EAST WEST UNIVERSITY

Effect of Lightly Doped Drain on the Electrical Characteristics of CMOS Compatible Vertical MOSFETs

By

Md. Delowar Hossain

In partial fulfillment of the requirements for

The degree

Of

Bachelor of Science in Electrical and Electronic Engineering

(B.Sc. in EEE)

Summer, 2013

The Department of Electrical and Electronic Engineering

Faculty of Sciences and Engineering

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Thesis Supervisor	Chairperson
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APPROVAL

The thesis titled "Effect of Lightly Doped Drain on the Electrical Characteristics of CMOS Compatible Vertical MOSFETs" submitted by Md.Delowar Hossain (SID: 2008-1-80-047) has been accepted as satisfactory in partial fulfillment of the requirements for the degree of Bachelor of Science in Electrical and Electronic Engineering on summer 2013.

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ABSTRACT

CMOS compatible ion implanted vertical MOSFET has been recently demonstrated as a viable route for improving RF performance of matured CMOS technology. Unlike planar MOSFETs, in this type of devices heavily doped and lightly doped drain is provided by single implantation and anneal. For this reason depending on anneal time the depth of LDD and doping is determined which could have unavoidable effects on vertical MOSFET's electrical characteristics. In this thesis I investigate effect of LDD doping on the CMOS compatible vertical MOSFETs structure. Electrical characteristics of 100nm vertical MOSFET is investigated for different values of LDD and body doping values. It is found that with the increase of LDD doping drive current of vertical MOSFET increases whereas sub-threshold performance is degraded. The degradation of sub-threshold performance is found to be more prominent at low body doping values. In addition to this threshold voltage of vertical MOSFETs are found to decrease with the increase of LDD doping. These effects are explained by the reduction of the effective channel lengths and decrease in the source/ drain series resistances with the increase of LDD doping values. These results are very significant for choosing appropriate body doping and LDD doping values for fabricating 100nm CMOS compatible vertical MOSFETs.

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CHAPTER 1

INRODUCTION

1.1 Motivation

In modern CMOS technology the MOSFETs has been scaled down in size. Small MOSFETs are desirable for several reasons. The main reason of making transistors small is to pack more devices in a smaller chip area. This results in a chip with more functionality in same area. It is expected that smaller transistors will provides faster operation.

Scaling of the MOSFETs require all devices dimension to be reduced proportionally. The main devices dimensions are channel length, channel width and oxide thickness. Due to scale down of the MOSFETs size when the channel length of MOSFETs is below than 100nm some operational problems occur which is known as short channel effect (SCE) including hot carrier effects, drain induce barrier lowering effect (DIBL), punch-through effect, velocity saturation effect etc. Moreover, the fabrication cost of conventional planar MOSFETs below 100nm channel lengths is extremely expensive due to expensive lithography requirement to define the channel region.

Many types of alternative architectures are investigated to eliminate the short channel effect and to reduce the MOS fabrication cost in conventional silicon based technology. Such as,

- FINFET,
- Planner double gate MOSFETs and
- Vertical MOSFETs etc.

Among these different device structures investigated vertical MOSFETs are potentially attractive due to following reasons.

1. Easier realization of surround gate structures.
2. Flexibility of designing short channel devices using relaxed lithography node.
3. Decoupling of the gate length from the packing density.
4. Less silicon area requirement to fabricate a vertical MOSFET.

When, MOSFETs is scaled beyond 100nm, lightly doped drain (LDD) is used to reduce hot carrier effect. This LDD is given in planner MOSFET by double implantation and spacer

technology. At first a low energy implant is used to create LDD (n^-) region and then source/drain is formed by a heavy dose of (n^+) implant, while protecting the LDD region by spacers. In contrast in vertical MOSFETs, LDD is not provided elaborately by double implantation due to its specific architecture. Here, LDD is provided by annealing time with one implant. For this reason depending on annealing time the depth of LDD and doping is determined. The LDD doping could have unavoidable effects on vertical MOSFETs devices performance which has not been exclusively studied.

1.2 Thesis Objective

In this thesis work I study the effect of LDD in vertical MOSFETs architecture. Device performance of a 100nm ion implanted vertical MOSFETs has been studied at various LDD and body doping to see the effect of LDD on different device parameters like, drive current, sub-threshold slope, DIBL and threshold voltage etc. This study would provide insight into choosing appropriate body and LDD doping for vertical MOSFETs fabrication.

1.3 Organization

This thesis report is segmented into seven different chapters. The first chapter describes the introduction of this thesis includes the motivation, objective and organization. This chapter discussed about the road map of modern CMOS technology. It also describes about the LDD forming process at the conventional planar MOSFETs.

The second chapter introduced with the various type of vertical MOSFETs structure so far available in the literature.

Chapter three discusses about the basic theory of the MOSFETs devices.

In chapter four, the simulation methodology is described elaborately. Here, I discuss the basic simulation technique of device simulation software ATLAS-SILVACO. It also recognizes the process of MOSFETs modeling at ATLAS software and the appropriate grid structure. Finally, it introduces with different method and model which are important for simulating any semiconductor devices.

Chapter five presents the results of the simulation in detail.

Finally, in chapter six and seven I describe the description and conclusion about my thesis.

CHAPTER 2

LITERATURE REVIEW

There have been several approaches investigated for designing and fabrication of vertical MOSFETs. These approaches are separated as three different types of vertical MOSFETs such as,

Type 1 - Vertical MOSFETs based on epitaxy.

Type 2 - Vertical replacement gate MOSFETs.

Type 3 - Vertical MOSFETs based on ion implantation.

A MOSFETs transistor of type 1, vertical MOSFETs based on epitaxy [1-5] is manufactured by accurately growing epitaxial layers for the heavily doped (n^+) drain and source and p type channel illustrated in figure 2.1. For good control of channel length accurate epitaxy is needed. That can be achieving by using controlled low pressure chemical vapor deposition (LPCVD), to grow single crystal material on substrate. After epitaxy process a vertical MOSFETs transistor is manufactured by a pillar etch, gate oxide growth and finally a polysilicon gate is deposited and patterned. The main disadvantage of this technique is the integration of epitaxial layer into a standard CMOS process. In addition, as both source and drain extend across the full width of the pillar, this configuration gives very high parasitic bipolar transistor action. Another major disadvantage is the source/ drain overlap capacitance as polisilicon gate passes over the pillar top and bottom respectively for lithographic alignment tolerance and gate track to contact.

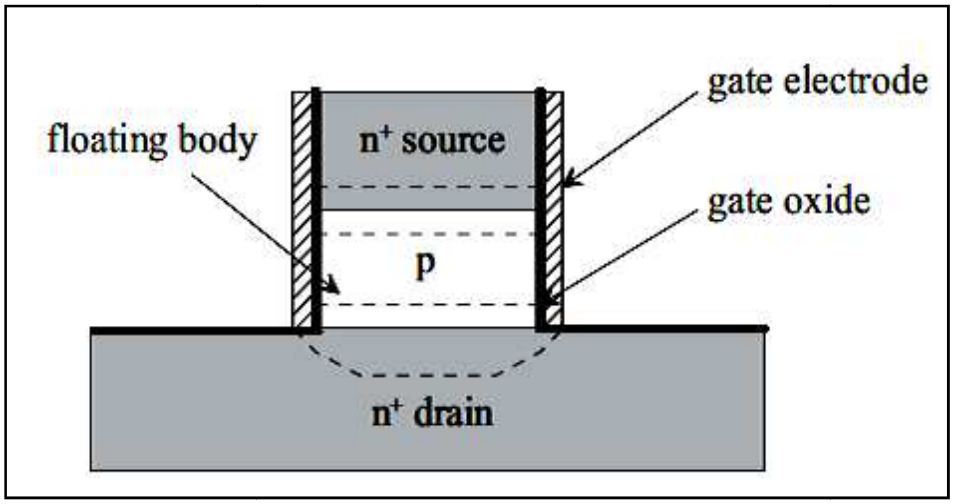

Figure 2.1: Vertical MOSFET based on epitaxy.

A variant of epitaxy approach has also been developed, which uses selective epitaxy [6-10] as illustrated in figure 2.2. In this approach, an oxide/ polysilicon/ oxide stock is created before the epitaxy. Then a trench is created by dry etches and gate oxide is grown. By using selective epitaxy the heavily doped (n^+), drain, source and p-type channel is created. This selective epitaxy removes overlap capacitance but high parasitic bipolar gain remains problem. Moreover, other problems are creation of the high quality gate oxide on polysilicon and the controlling facets during selective capacity.

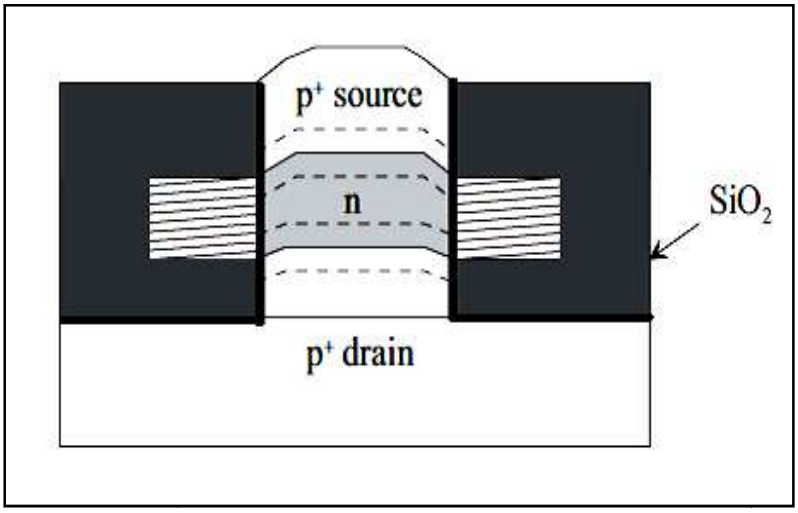

Figure 2.2: Vertical MOSFET based on selective epitaxy with reduced overlap capacitance.

The type 2 vertical MOSFETs is shown the figure 2.3 that is the vertical replacement gate MOSFETs (VRG). The VRG MOSFETs [11-14] can be made with competitive parasitic capacitances and packing density as compare to planar MOSFETs. Here, the layer deposition method is used to create a channel length which defined by the layer thickness. The gate length is precisely defined by a blanket film deposition. At first, arsenic ion is implanted into silicon wafer to form heavily doped (n^+) drain regions. Then multi-layer stack of phosphosilicate glass (PSG)/ nitride/ undoped oxide/ nitride/ PSG is deposited on the drain layer. After the multilayer stack is deposited, a rectangular vertical trench is etched through the entire stack. Then boron-doped crystalline silicon is grown by selective epitaxy to form P-type single-crystal device channel. The silicon channel is planarized using chemical mechanical polishing (CMP). After this the process is followed by forming source region by arsenic ion implantation, forming source-drain extension (SDEs) by solid source diffusion (SSD), depositing and etching nitride spacer and removing sacrificial gate layer. Finally gate oxide is grown, gate deposition and patterning is done.

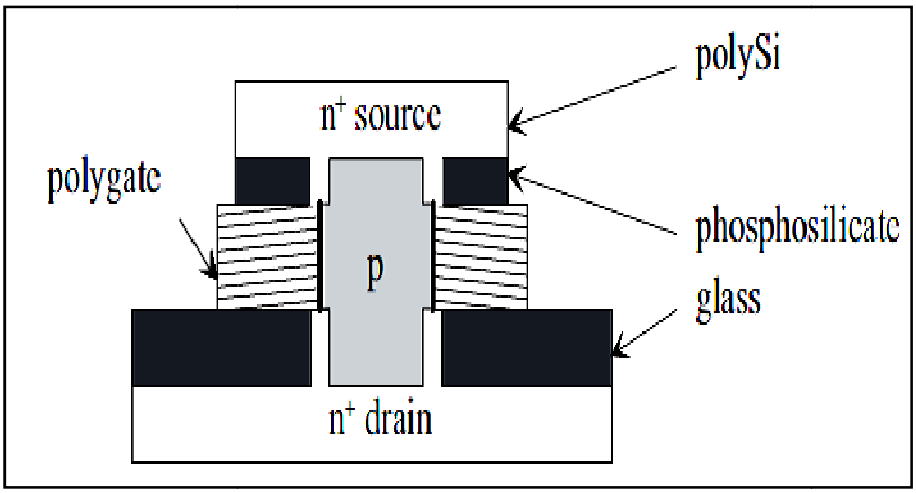

Figure 2.3: Vertical replacement gate MOSFET.

In this type of vertical MOSFETs, the overlap capacitances are much lower than the device, vertical MOSFETs based on epitaxy as it is determined by the thickness of the insulators between the PSG layers and the gate layer of this device. Because of source and drain extension across the entire width of the pillar, the parasitic bipolar transistor is found a problem. A partial solution is proposed by using a shallow polysilicon source pad to manufacture a leaky body contact [15]. Main disadvantage of this architecture is that it is not at all CMOS compatible due to the use of epitaxy.

Finally, the third type of vertical MOSFETs is the vertical MOSFETs based on ion-implantation [16-24] as illustrated in figure 2.4. The source and drain regions of this type of MOSFETs is formed by ion-implantation. The silicon pillar height and the implant energy determine the channel length of this type of MOSFETs.

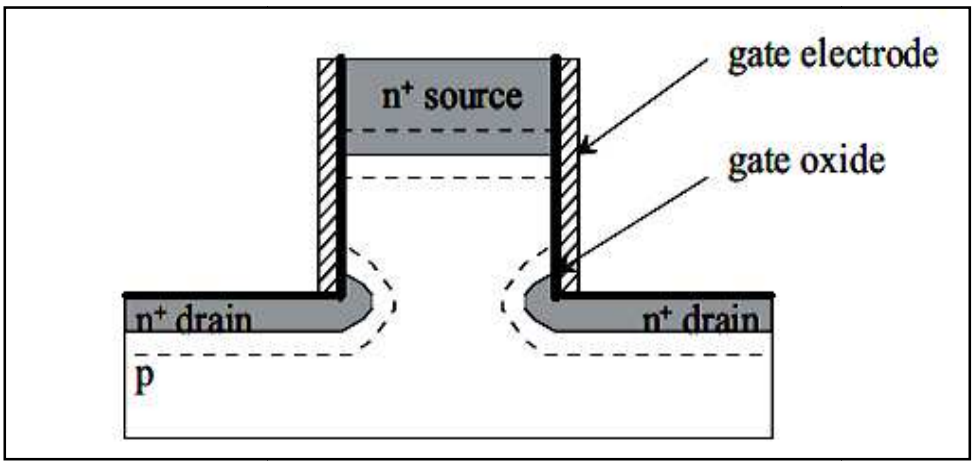

Figure 2.4: Vertical MOSFET based on ion implantation.

In this type of MOS device it is possible to give a narrow shape pillar with the gate surrounding the entire pillar and the channel is completely lithography independent. In this type of device the parasitic bipolar gain is lower than the device, vertical MOSFETs base on epitaxy. The main reason of that is the drain never penetrates across the width of the pillar. Another major advantage of this type device is CMOS compatibility while parasitic source/ drain overlap capacitance has been eliminated in this type of vertical MOSFETs devices using FILOX process [25] which made this type of devices most promising for industrial application. Extensive investigations have been done on this type of vertical MOSFETs [26, 27, 28] and recently this type of vertical MOSFET has been demonstrated as viable route for improving RF performance of matured CMOS technologies [26]. Due to potential CMOS compatibility and industrial application in this work I study effect of LDD on ion-implanted vertical MOSFETs architecture.

CHAPTER 3

THEORY OF MOSFETs

In this chapter I have discussed the fundamental theory of MOS devices. For a uniformly doped p-type semiconductor substrate the following considerations are made.

3.1 Two-terminal MOS Structure

A two-terminal metal oxide semiconductor (MOS) structure, also known as a MOS capacitor, consists of three layers namely a semiconductor layer, an embedded insulator layer and a conducting layer. Figure 3.1 shows the energy band diagram of an ideal two-terminal MOS structure.

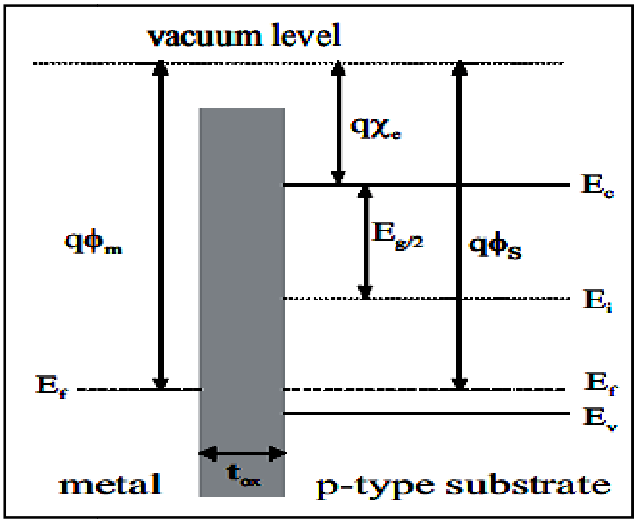

Figure 3.1: Band diagram of an idealized two-terminal MOS structure in flat band condition.

In an idealized MOSFETs structure the flat band voltage V_{FB} defined as the energy band difference between the metal work function ϕ_m and the silicon work function ϕ_s is zero so that,

$$qV_{FB} = q\phi_{ms} = q\phi_m - q\phi_s = q\phi_m - \left(q\,\chi_e + \frac{E_g}{2} + q\phi_f\right) = 0 \qquad (3.1)$$

Where, ϕ_{ms} is the work function difference, q is the elementary charge, χ_e is the electron affinity, E_g the band gap between the conduction and valence band, E_v the energy level of the valence band, E_c the energy level of the conduction band, ϕ_f is named the Fermi potential and is the difference between the Fermi level E_f and the intrinsic energy level E_i divided by the electron charge q. The Fermi potential of a p-type substrate can be calculated using the substrate doping concentration N_A and the intrinsic carrier concentration n_i as,

$$\phi_f = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) \tag{3.2}$$

Where, k is the Boltzmann constant and T the temperature in Kelvin.

Applying a voltage to the semiconductor changes the charge in the substrate. Three modes of operation can be differentiated between namely accumulations, depletion and inversion, as shown in figure 3.2. In the case of a p-type substrate and a voltage $V_G < 0V$ applied to the gate contact, whilst the substrate is connected to ground, free charge carriers (holes) are accumulated under the insulation layer (oxide). Since free holes are moving towards the silicon surface layer, the surface charge is of the same type as in the substrate, but of higher concentration. This layer is called accumulation layer (figure 3.2(a)). The applied voltage causes a voltage drop over the oxide as well as bending the energy bands in the substrate. At the oxide/ semiconductor interface the surface potential ψ_s can be found. If $V_G > 0V$, free positive charge carriers are pushed away from the surface layer and thereby a depletion region of the width x_d is formed. This process is termed depletion (figure 3.2(b)). In figure 3.2(c) a large voltage is applied to the gate. The surface layer inverts from p-type to n-type as nearly all free holes are pushed away from the surface layer and at the same time free electrons accumulate underneath the oxide. As soon as the intrinsic level E_i increases beyond the Fermi level E_f to obtain a negative charged surface layer, the surface is in weak inversion mode ($\psi_s \geq \phi_f$). At the onset of strong inversion the surface potential barrier ψ_s is defined by $\psi_s = 2|\phi_f|$ as shown in figure 3.3.

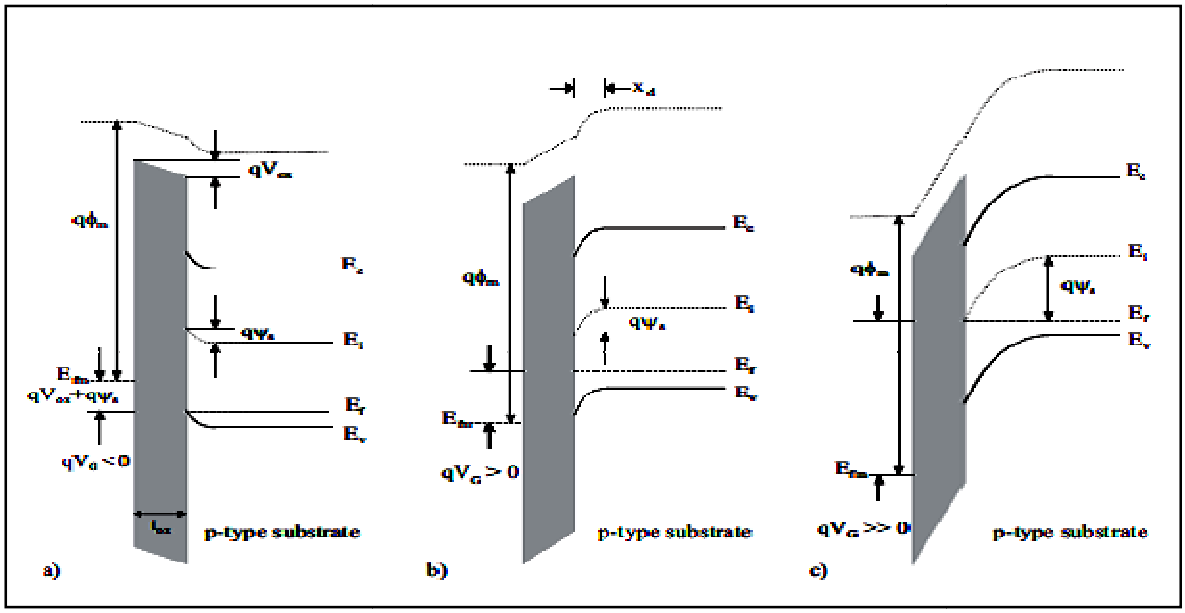

Figure 3.2: One-dimensional MOS structure (a) accumulation ($\psi_s < 0$) (b) depletion ($0 < \psi_s < \phi_f$) (c) Onset of weak inversion ($\psi_s = \phi_f$).

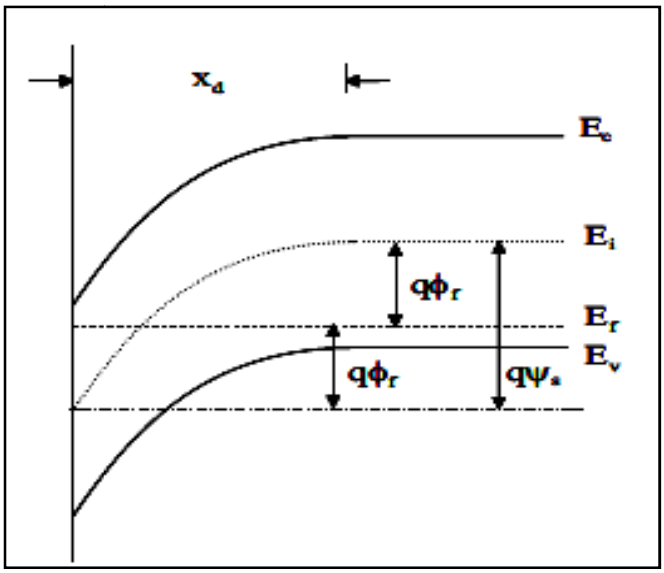

Figure 3.3: Energy band diagram showing the onset of strong inversion ($\psi_s = 2\phi_f$).

The gate voltage to bring the surface layer into strong inversion is termed the threshold voltage V_T. In order to calculate the threshold voltage, first the depletion width x_d of a doped semiconductor needs to be calculated. This can be achieved by solving the one-dimensional Poisson's equation which relates the electric field E(x) to the charge density ρ(x) as follows,

$$\frac{dE(x)}{dx} = \frac{\rho(x)}{\epsilon_{S_i}\epsilon_0} \quad \text{for } 0 < x < x_d \tag{3.3}$$

Where, ϵ_0 is the dielectric constant in vacuum and ϵ_{S_i} is the dielectric constant of silicon[29]. The charge density equals the number of acceptors in the substrate $\rho(x) = -qN_A$ for an abrupt junction. The maximum field can now be calculated by integrating over the depletion region,

$$E_{max} = \int_0^{x_d} \frac{-qN_A}{\epsilon_{S_i}\epsilon_0} dx = \frac{-qN_A x_d}{\epsilon_{S_i}\epsilon_0} \tag{3.4}$$

Further, the differential relation between the surface electric field E at x = 0 and the voltage ψ_s applied to the silicon over a small width at strong inversion is,

$$E = -\frac{d\psi_s}{dx} \tag{3.5}$$

The surface potential across the region is,

$$\psi_s = -\int_0^{x_d} E dx = -\int_0^{x_d} \frac{-qN_A x_d}{\epsilon_{S_i}\epsilon_0} dx = \frac{qN_A {x_d}^2}{2\epsilon_{S_i}\epsilon_0} \tag{3.6}$$

The depletion layer width for a p-type semiconductor can hence be calculated as,

$$x_d = \sqrt{\frac{2\epsilon_{S_i}\epsilon_0|\psi_s|}{qN_A}} \tag{3.7}$$

The substrate depletion charge Q_B density at the onset of strong inversion ($\psi_s = 2|\phi_f|$) can be written as,

$$Q_B = -qN_A x_d = -qN_A\sqrt{\frac{2\epsilon_{S_i}\epsilon_0 2|\phi_f|qN_A}{q^2{N_A}^2}} = -\sqrt{4qN_A\epsilon_{S_i}\epsilon_0|\phi_f|} \tag{3.8}$$

The applied gate-substrate voltage drops over the oxide as well as over the depletion region. The threshold voltage V_T is therefore,

$$V_T = V_{ox} + |\psi_s| = -\frac{Q_B}{C_{ox}} + 2|\phi_f| = \frac{\sqrt{4qN_A\epsilon_{S_i}\epsilon_0|\phi_f|}}{C_{ox}} + 2|\phi_f| \tag{3.9}$$

Where, V_{OX} is the oxide voltage.

Equation (3.9) shows that varying the substrate doping concentration changes the threshold voltage. This knowledge can be used to explicitly influence the threshold voltage in order to change the on/off voltage of the transistor. The desired threshold voltage is typically ±0.3V for n-channel and p-channel MOSFETs respectively.

3.1.1 Work Function Difference

In practice, the work function in the silicon is different than the work function in the gate. This is certainly true for polysilicon, which is commonly used as a gate material in CMOS, as shown in figure 3.4. In this case the Fermi potential ϕ_{poly}, assuming non-degeneration, of the n-type poly silicon can be written as,

$$\phi_{poly} = \frac{kT}{q}\ln\left(\frac{n_i}{N_D}\right) \tag{3.10}$$

Where, N_D is the doping concentration of the poly silicon gate.

However, if the doping concentration of the polysilicon gate is higher than 10^{18}-10^{19} cm^{-3} the Fermi level is equal to the energy level of the conduction band so that, $E_f \simeq E_c$ [30].

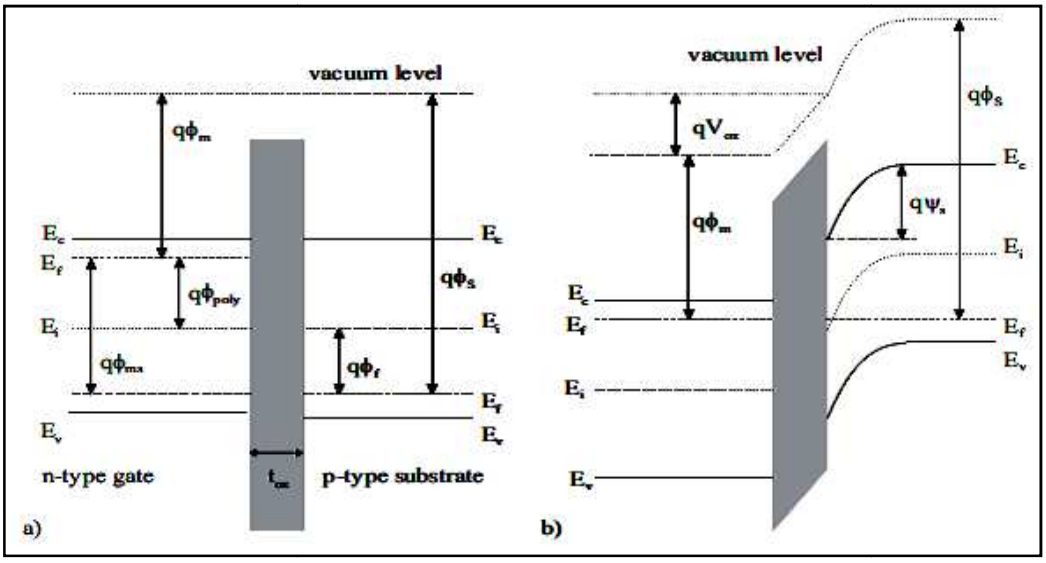

Figure 3.4: Energy band diagram of a MOS structure with degenerated polysilicon.

Figure 3.4(a) illustrates the semiconductor/ oxide semiconductor stack in flat band.

The work function difference in this case is,

$$q\phi_{ms} = -(q\phi_{poly} + q\phi_f) \tag{3.11}$$

If the gate and the substrate are under zero bias condition the semiconductor is depleted as shown in figure 3.4(b). Here, the Fermi energy levels E_f of the gate and the substrate are aligned and the MOSFETs structure is in weak inversion.

The threshold voltage can now be written as,

$$V_T = \frac{\sqrt{4qN_A\epsilon_{S_i}\epsilon_0|\phi_f|}}{C_{ox}} + 2|\phi_f| + V_{FB} \tag{3.12}$$

3.1.2 Oxide Interface Traps

The oxide charge Q_{ox} is the inherent charge embedded between the gate and semiconductor and is strongly affected by the gate oxidation conditions as well as the crystal orientation. In the previous section the voltage to achieve flat band V_{FB} was only dependent on the work function difference ϕ_{ms} so that $V_{FB} = \phi_{ms}$.

The flat band voltage needs to be modified to take care of charges in the silicon/gate oxide interface. These charges are namely interface-trapped charges, fixed-oxide charges, oxide-trapped charges and mobile ionic charge carriers as shown in figure 3.5.

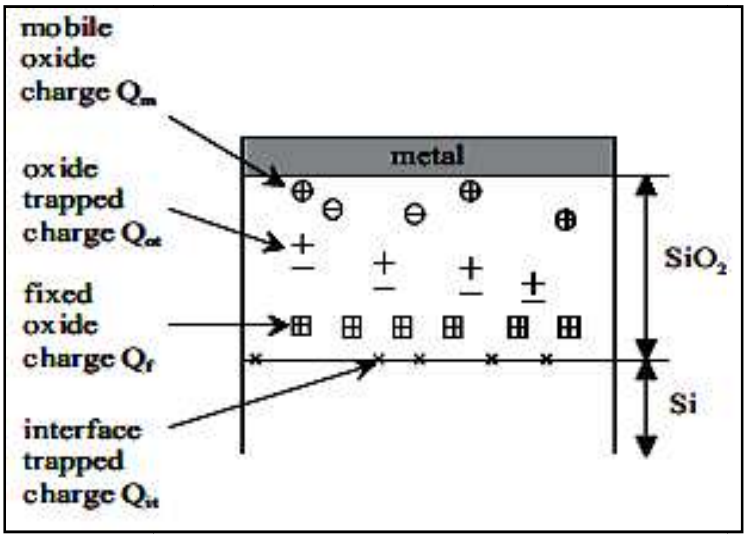

Figure 3.5: Oxide traps in the gate oxide.

Interface-trapped charges Q_{it}, with energy states in the silicon forbidden band gap are located at the Si-SiO_2 interface. The interface trap density is orientation dependent. A variation in the order of one magnitude can be found in <100> orientation compared with silicon in <111> orientation. S_{ZE} reports values of Q_{it} in the region of $10^{10}cm^{-2}$ [31].

Fixed-oxide charges Q_f are also depending on the oxidation and annealing conditions. Typical densities for a <100> surface are $10^{10}cm^{-2}$ and for a <111> surface $5 \times 10^{10}cm^{-2}$. Oxide-trapped charges Q_{ot} are caused by defects in the SiO_2 layer due to X-ray radiation or high energy electrons.

Contamination during the oxidation process can leave alkali ions as mobile carriers in the silicon oxide causing mobile ionic charges Q_m. Assuming that all charges are very close to the oxide/ silicon interface, the flat band voltage including the above discussed oxide charges can be written as,

$$V_{FB} = \phi_{ms} - \frac{Q_{it}+Q_f+Q_m+Q_{ot}}{C_{ox}} \tag{3.13}$$

3.1.3 Small-signal Capacitance

So far the two terminal MOSFETs structure has been evaluated under static conditions. In this section the ac signal behavior will be investigated. The capacitance C_{ox} between two plates of a parallel plate capacitor is given by,

$$C_{ox} = \frac{\epsilon_{ox}\epsilon_0 A_{ox}}{t_{ox}} \tag{3.14}$$

Where, t_{ox} is the thickness of the oxide and A_{ox} the area.

Equation (3.14) is valid to calculate the capacitance in accumulation as shown in figure 3.6. If the two-terminal MOS structure is in depletion condition, the oxide capacitance and the capacitance of the depletion region are in series. The overall capacitance under this condition is,

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_d} = \frac{C_{ox}+C_d}{C_{ox}C_d} \tag{3.15}$$

Where, C_d is the depletion capacitance.

At high measurement frequencies, as the gate voltage is increased the capacitance drops to its minimum value so that the capacitance is given by equation (3.15). This is because the inversion layer charge (minority charge carriers) cannot keep up with the fast changing voltage applied to the device and only the depletion charge can respond to the applied ac-signal. The inversion layer charge can only be changed by the mechanism of thermal generation and recombination which is a relatively slow process.

At low measurement frequencies a different behavior is observed because the inversion layer charge can follow the variation of the applied signal. In this case the depletion charge is constant. All of the applied voltage drops across the oxide so that $C=C_{ox}$ as in accumulation.

Thus, if the capacitance is plotted as a function of V_G, a graph similar to figure 3.6 is obtained.

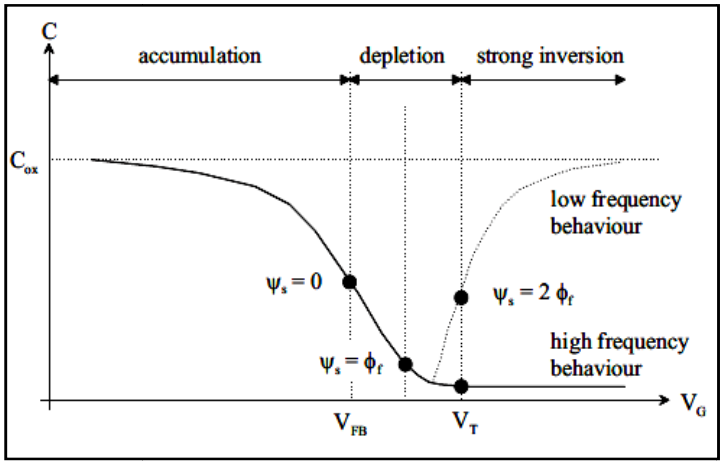

Figure 3.6: Capacitance of a two-terminal MOS structure as function of gate voltage.

3.2 Four-terminal MOS Structure

The four-terminal MOS structure or MOSFET is similar to a two-terminal MOS structure with the addition of source and drain regions. Two types of MOS transistors can be distinguished, namely enhancement mode and depletion mode devices. In this section the enhancement mode MOSFETs will be discussed. For the following description of the device, it is assumed that the source is tied to ground.

Figure 3.7(a) shows a zero biased gate, source, drain and substrate. Around the n+ − p junctions, there is a small depletion region. The resistance between source and drain is very high, as the two pn-junctions are of opposite polarity.

Applying a gate voltage V_G of $V_{FB} < V_G < V_T$ depletes the p-type semiconductor underneath the gate oxide. The space charge region around source and drain now extends under the gate. Increasing the gate voltage so that $V_G > V_T$ adds to the already existing depletion region an inversion layer connecting the source and drain regions. However, since there is no voltage difference between the source and drain, no current can flow and $I_D = 0$.

3.2.1 Linear Operation

A positive gate voltage V_G of $V_{FB} < V_G < V_T$ as well as a positive voltage connected to the drain ($V_{DS} > 0$) forms a depletion layer underneath the gate oxide. Since the gate voltage is not sufficient to create an inversion layer, no channel exists to connect the source and drain regions. Without taking leakage currents into account it can be said that $I_D=0$. This mode of

operation is called the cutoff mode. For the condition of $V_G > V_T$ and $V_{DS} < (V_G - V_T)$, a channel is formed, connecting source and drain as shown in figure 3.7(b). The MOSFETs is said to be non-saturated. Due to the inversion layer, free electrons lower the drain/ source resistance, which is now much less than in depletion mode and, furthermore, can be controlled by the positive gate voltage. This mode of operation is called linear mode. The maximum channel voltage (V_c, max (y = L) = V_{DS}) can be found at the drain and drops to Vc, min (y=0)=0V at the source.

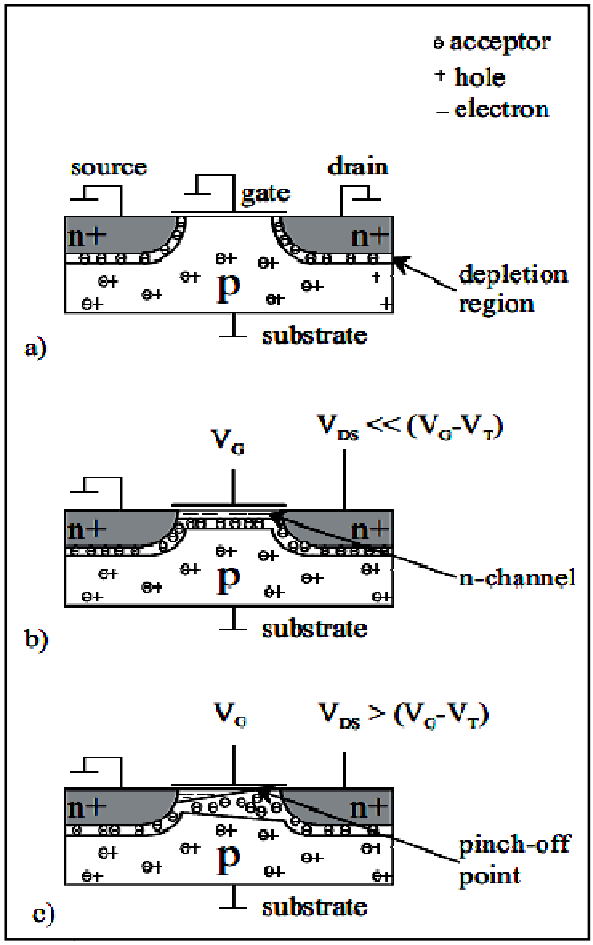

Figure 3.7: Four terminal MOSFET structure (a) with zero biased gate (b) in cutoff.

It is assumed that the channel is of constant length L, and of constant width W and its thickness changes between source and drain. In the following, the drain current for the linear region will be derived. The differential voltage drop in the inversion channel, parallel to the surface is defined as,

$$dV_c = I_D dR = I_D \frac{\rho}{A_c(y)} dy = I_D \frac{\rho}{x_c(y)W} dy \qquad (3.16)$$

Where, $A_c(y)$ is the cross-section area of the channel, $X_c(y)$ is the channel thickness and ρ the channel charge density.

Since the channel resistivity can be expressed as $\rho = 1/ (q\ \mu_n\ n)$, the differential voltage is,

$$dV_c = I_D \frac{1}{q\mu_n x_c(y) W} dy \tag{3.17}$$

Where, μ_n is the channel mobility and n the number of negative charge carriers.

The inversion layer charge in the channel is defined by $Q_I(y) = -q\ n\ x_c(y)$. Therefore the equation of the differential voltage can be solved for the drain current to,

$$I_D\ dy = -Q_I(y)\mu_n W\ dV_c \tag{3.18}$$

The inversion layer charge is dependent on the effective voltage across the MOSFETs capacitor so that,

$$Q_I(y) = -C_{ox}(V_G - V_T - V_c(y)) \tag{3.19}$$

The drain current becomes,

$$I_D\ dy = C_{ox}\big(V_G - V_T - V_c(y)\big)\mu_n W\ dV_c \tag{3.20}$$

Integrating the left term of the equation over the given channel length L, whilst integrating the right term of equation (3.20) over the voltage drop across the channel gives,

$$I_D \int_0^L dy\ = C_{ox}\,\mu_n W \int_0^{V_{DS}} (V_G - V_T - V_c(y))\ dV_c$$

$$\text{Or,}\quad I_D L = C_{ox}\,\mu_n W \left((V_G - V_T)V_{DS} - \frac{1}{2}{V_{DS}}^2\right) \tag{3.21}$$

With,

$$\beta = C_{ox}\,\mu_n \frac{W}{L} \tag{3.22}$$

The process transconductance parameter, equation (3.21) becomes the equation for the drain current in linear mode.

$$I_D = \beta\left((V_G - V_T)V_{DS} - \frac{1}{2}{V_{DS}}^2\right) \tag{3.23}$$

3.2.2 Saturation Operation

The drain current cannot be continuously increased. At some point ($V_{DS} = V_G - V_T$) the channel pinches off as illustrated in figure 3.7(c). The MOSFETs is now in saturation mode. The onset of saturation can be approximated by finding the maximum current using,

$$\frac{dI_D}{dV_{DS}} = 0 = \beta(V_G - V_T - V_{DS}) \tag{3.24}$$

At this point the drain voltage is,

$$V_{DS,sat} = V_G - V_T \tag{3.25}$$

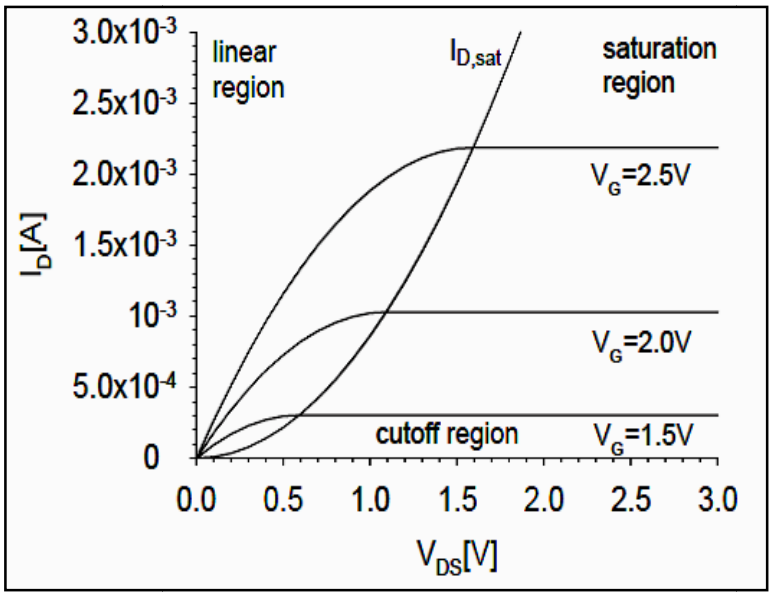

Figure 3.8: Idealized output characteristic of a 100nm channel length (W=1μm) MOSFETs.

The current previously calculated for the linear region in equation (3.23) now changes, after substituting the drain voltage by its saturation value to,

$$I_D = \frac{1}{2}\beta(V_G - V_T)^2 \tag{3.26}$$

Equation (3.26) is valid for long channel devices and does not take velocity saturation found in short channel devices into account.

Figure 3.8 illustrates the output characteristic of a MOSFET based on equation (3.23) and (3.26). Furthermore, figure 3.8 shows the locus of $V_{DS,sat}$ where the current reaches its maximum value.

3.2.3 Body Bias Effect

Biasing the substrate, changes the voltage across the depletion layer and therefore its thickness and hence the threshold voltage. The depletion layer charge (see equation (3.8)) changes to,

$$Q_B = -\sqrt{4qN_A\epsilon_{S_i}\epsilon_0(|\phi_f| + V_B)} \tag{3.27}$$

Where, V_B is the substrate bias voltage.

The change in threshold voltage can now be determined as,

$$\Delta V_{Tbias} = \frac{\sqrt{4qN_A\epsilon_{S_i}\epsilon_0(|\phi_f|+V_B)}}{C_{ox}} - \frac{\sqrt{4qN_A\epsilon_{S_i}\epsilon_0|\phi_f|}}{C_{ox}} \tag{3.28}$$

3.2.4 Detailed MOSFETs Analysis

For the previous analysis it was assumed that the threshold voltage V_T was constant along the channel. However, in reality the channel voltage $V_c(y)$ changes the substrate depletion charge density Q_B. Assuming ($V_S = V_B = 0$) the threshold voltage can be written as,

$$V_T(V_c) = \frac{1}{C_{ox}}\sqrt{2q\epsilon_{S_i}\epsilon_0 N_A(2|\phi_f| + V_c)} + 2|\phi_f| + V_{FB} \tag{3.29}$$

The non-saturated drain current can be written as,

$$I_D = \beta\int_0^{V_{DS}}\{(V_G - V_{FB} - 2|\phi_f|) - V_c - \frac{1}{C_{ox}}\sqrt{2q\epsilon_{S_i}\epsilon_0 N_A(2|\phi_f| + V_c)}\}dV_c \tag{3.30}$$

Integrating the above equation leads to the following equation

$$I_D = \beta((V_G - V_{FB} - 2|\phi_f|)V_{Ds} - \frac{1}{2}{V_{DS}}^2 - \frac{2}{3C_{ox}}\sqrt{2q\epsilon_{S_i}\epsilon_0 N_A}\{(2|\phi_f| + V_{DS})^{\frac{3}{2}} - (2|\phi_f|)^{\frac{3}{2}}\}) \tag{3.31}$$

At the peak value of the non-saturation current ($\frac{dI_D}{dV_{DS}} = 0$) the saturation voltage is,

$$V_{DS,sat} = V_G - V_{FB} - 2|\phi_f| - \frac{q\epsilon_{S_i}\epsilon_0 N_A}{{C_{ox}}^2}\left(\sqrt{1 + \frac{2{C_{ox}}^2}{q\epsilon_{S_i}\epsilon_0 N_A}(V_G - V_{FB})} - 1\right) \tag{3.32}$$

Substituting equation (3.32) into equation (3.31) allows a more accurate calculation of the drain current in the non-saturated region. In comparison with equation (3.23), the values of I_D in the detailed analysis tend to be lower than in the simple equations.

3.2.5 Sub Threshold Region

When $\phi_f < \psi_s < 2\psi_f$ the semiconductor surface is in weak inversion. At this point the minority carrier concentration is still lower than the substrate doping concentration N_A. The corresponding drain current I_D is termed sub-threshold current. The sub-threshold current is of particular importance for low-power applications as it determines the off-current.

In weak inversion the sub-threshold current is dominated by diffusion instead of drift. Due to the arrangement of the MOSFETs, $I_{D\,sub}$ be approximated in the same way as the collector current of an npn-bipolar transistor with homogeneous base doping to,

$$I_{D_{sub}} = -qA_{sub}D_n\frac{d_n}{d_y} = qA_{sub}D_n\frac{n(0)-n(L)}{L} \tag{3.33}$$

Where, A_{sub} is the cross-section of current flow, $D_n = \mu_n kT/q$ the electron diffusion coefficient and n(0) and n(L) the electron densities in the channel at the source and the drain. The area A_{sub} of current flow is given by the width W of the device and the effective channel thickness X_{ceff}. The effective channel thickness can be calculated as,

$$x_{ceff} = \frac{kT}{q} E_s \tag{3.34}$$

Where, E_s is the electric field at the silicon surface in weak-inversion.

E_s is given by,

$$E_s = \frac{-Q_B}{\epsilon_{S_i}\epsilon_0} = \sqrt{\frac{2qN_A\phi_{ss}}{\epsilon_{S_i}\epsilon_0}} \tag{3.35}$$

Where, ϕ_{ss} is the surface potential at the source.

The electron densities are given by,

$$n(0) = n_i \exp\left(\frac{q(\phi_{ss}-\phi_f)}{kT}\right)$$
$$n(L) = n_i \exp\left(\frac{q(\phi_{ss}-\phi_f-V_{DS})}{kT}\right) \tag{3.36}$$

Substituting equation (3.36) into equation (3.33) gives,

$$I_{D_{sub}} = \frac{qA_{sub}D_n n_i \exp\left(\frac{-q\phi_f}{kT}\right)}{L}\left(1 - \exp\left(\left(\frac{-qV_{DS})}{kT}\right)\right)\right) \exp\left(\frac{q\phi_{ss}}{kT}\right) \tag{3.37}$$

The sub-threshold swing is defined as,

$$S = \left(\frac{d(\log_{10} I_D)}{dV_G}\right)^{-1} \tag{3.38}$$

For the simulation it was assumed that the surface potential at the source is equal to the surface potential given by $V_G - V_{FB}$. The extracted sub-threshold slope S was 60mV/dec. Equation (3.37) shows the linear relation between the channel length L and the drain current $I_{D\,sub}$.

3.2.6 Short Channel and Narrow-width Effects

The equations discussed in the previous section are fairly accurate for describing large devices; they cannot be applied to small-geometry MOSFETs devices.

Charge Sharing Effects:

A significant fraction of total substrate depletion charge underneath the gate originates from the pn-junctions. This charge must be subtracted from the threshold voltage expression since it is independent from the applied gate voltage. For low V_{DS} the depletion region thickness can be considered constant throughout the channel. The depletion charge controlled by the

gate can be modeled as a trapezoidal volume. For this case the ratio $-Q_B/C_{ox}$ changes due to the geometry dependence to,

$$-\frac{Q_B L_{eff}}{C_{ox} L} \tag{3.39}$$

Where, L_{eff} is the effective channel length.

The bottom of the trapezoid has the same length L as the channel, whilst the top of the trapezoid has a length of L_1 such that,

$$L = L_1 + 2\Delta L \tag{3.40}$$

Where, ΔL is the lateral extent of the depletion width at the source and drain as shown in figure 3.9(a).

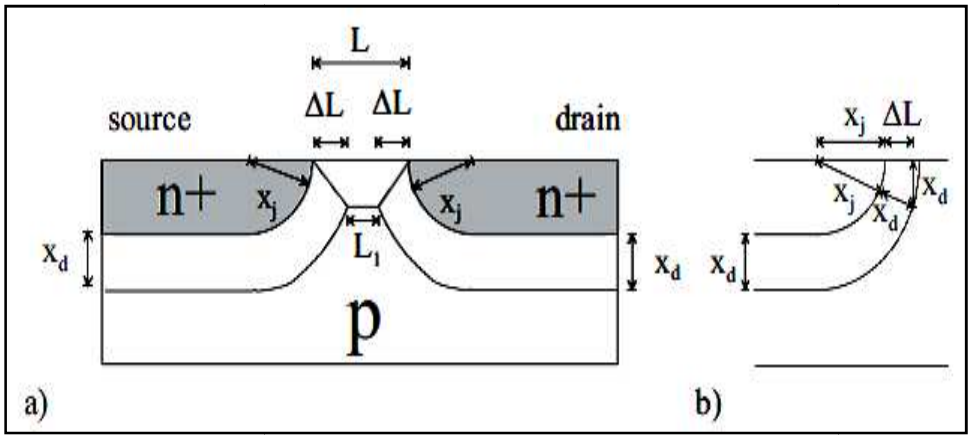

Figure 3.9: Schematic diagram of a charge sharing model showing the depletion.

The effective channel length can be written as,

$$L_{eff} = \frac{L+L_1}{2} = L - \Delta L \tag{3.41}$$

Substituting equation (3.41) into equation (3.39) gives,

$$-\frac{Q_B}{C_{ox}}\left(\frac{L-\Delta L}{L}\right) = -\frac{Q_B}{C_{ox}}\left(1 - \frac{\Delta L}{L}\right) \tag{3.42}$$

Assuming that the pn-junctions are shaped like quarter-circular arcs and extend a distance X_d into the p-substrate the depletion depth for the source and drain, respectively, can be expressed as,

$$x_d = \sqrt{\frac{4\epsilon_{S_i}\epsilon_0}{qN_A}|\phi_f|} \tag{3.43}$$

In order to calculate ΔL of the triangle shown in figure 3.9(b), we can say,

$$(x_j + \Delta L)^2 + {x_d}^2 = (x_j + x_d)^2 \tag{3.44}$$

Where, X_j is the junction depth of the n+ implant.

The solution of this quadratic is,

$$\Delta L = -x_j + \sqrt{x_j{}^2 + 2x_j x_d} \tag{3.45}$$

The short-channel threshold voltage V_{TSCE} V_{TSCE} can now be calculated as,

$$V_{TSCE} = V_{FB} + \frac{\sqrt{4qN_A\epsilon_{S_i}\epsilon_0|\phi_f|}}{C_{ox}}\left(1 - \frac{\Delta L}{L}\right) + 2|\phi_f|$$

$$= V_{FB} + \frac{\sqrt{4qN_A\epsilon_{S_i}\epsilon_0|\phi_f|}}{C_{ox}}\left(1 - \frac{x_j}{L}\left(\sqrt{1 + \frac{2x_d}{x_j}} - 1\right)\right) + 2|\phi_f| \tag{3.46}$$

The threshold voltage reduction induced by the short-channel effect ΔV_{TSCE} can be computed by using the above assumptions as,

$$\Delta V_{TSCE} = \frac{Q_B}{C_{ox}}\left(-\frac{\Delta L}{L}\right) = -\frac{\sqrt{4qN_A\epsilon_{S_i}\epsilon_0|\phi_f|}}{C_{ox}}\frac{x_j}{L}\left(\sqrt{1 + \frac{2x_d}{x_j}} - 1\right) \tag{3.47}$$

Channel Length Modulation:

Increasing the drain voltage beyond the onset of saturation ($V_{DS} > V_{DS,sat}$) moves the pinch-off point away from the drain towards the source. This movement of the pinch-off point is called channel length modulation. It should be noted, that the termination of the channel at the pinch-off point does not shut off the current. It rather injects carriers travelling from the source towards the drain into the drain depletion region. Since the voltage drop from the pinch-off point to the source is still $V_{DS,sat}$, the portion of the applied drain voltage beyond ($V_{DS} - V_{DS,sat}$) is dropped across the depletion layer at the drain. Compared to the onset of pinch-off, the same voltage is now dropped across a smaller channel length L´ so that L´<L as illustrated in figure 3.10.

The resulting drain current will increase slightly. This effect can be analytically modelled by approximating the inversion layer charge $Q_I(L\_) = 0$, which implies that,

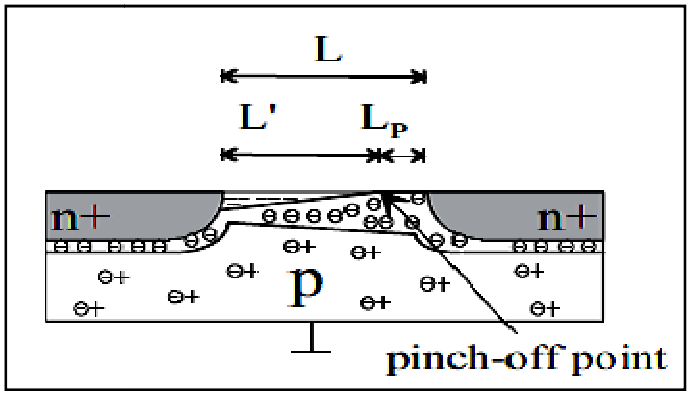

Figure 3.10: Channel under pinch-off condition.

The channel voltage at L is $V_{DS,sat}$ the pinch-off length L_P can be calculated using the approximation of a depletion region, whereby the voltage drop across this region is $(V_{DS}-V_{DS,sat})$ to,

$$L_P \simeq \sqrt{\frac{2\epsilon_{S_i}\epsilon_0}{qN_A}(V_{DS}-V_{DS,sat})} \tag{3.48}$$

The relation of the saturation current and the channel length modulation can now be approximated as,

$$I_D \simeq \frac{I_{D,sat}L}{L-L_P} = \frac{I_{D,sat}}{\left(1-\frac{L_P}{L}\right)} \tag{3.49}$$

Figure 3.11 illustrates the effect of channel length modulation. Simulating the effect of channel length modulation using equation (3.49) shows that the drain current does not saturate. Increasing the drain/ source voltage V_{DS} above $V_{DS,sat}$ increases the drain current I_D in the saturation region.

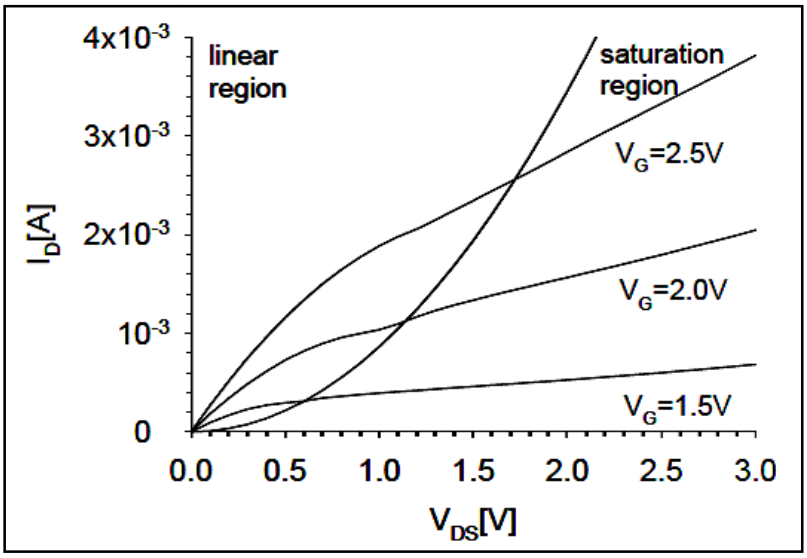

Figure 3.11: Output characteristic of a 100nm channel length (W=1μm) MOSFET.

Drain Induced Barrier Lowering:

As V_{DS} increases the channel length L is reduced because the drain depletion region moves closer to the source depletion region. This results in a significant field penetration from the drain to the source which lowers the potential barrier at the source. An increased injection of electrons by the source can now conduct more current than one would expect. This effect is termed drain-induced barrier lowering (DIBL) [32]. Furthermore, the depletion charge density Q_B of short channel devices, where the geometry of the depletion region is approximated as a trapezoid as shown in figure 3.9 is lower than for long channel devices,

where, a rectangular depletion region was assumed. This lowers the threshold voltage V_{TSCE} for increasing drain voltages V_{DS}.

Punch-through Effect:

Punch through occurs when, due to the drain applied voltage V_{DS}, both depletion regions merge and $V_G < V_T$. In this case, where L=2ΔL, the gate loses control over the drain current I_D [33]. To overcome the effect of punch-through, higher doping of the substrate is required to minimize the depletion region.

Narrow-width Effects:

The definition of the active area and the resulting depletion region beneath the silicon/ oxide/ polysilicon layer interface leads to a higher threshold voltage caused by an increase of the substrate charge per unit area Q_B. Two different approximations are shown in figure 3.12.

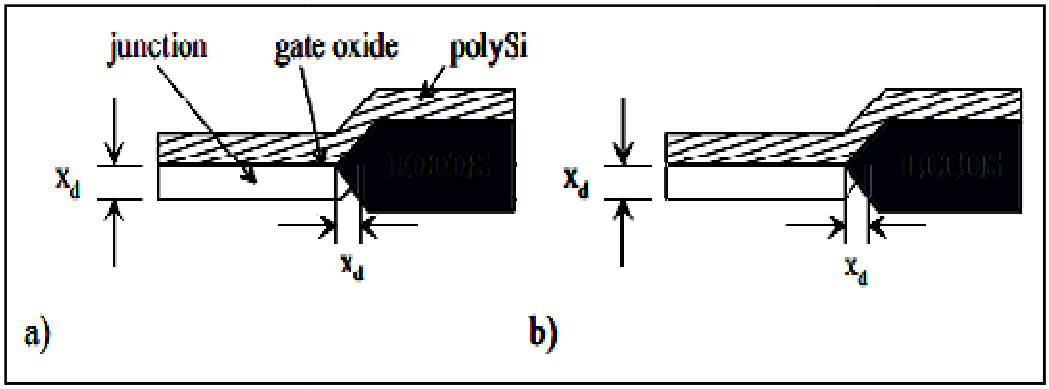

Figure 3.12: Narrow width effect of lateral MOSFETs (a) circle approximation (b) triangular.

The narrow-width threshold voltage V_{TNWE} can be calculated as,

$$V_{TNWE} = V_{FB} + \frac{\sqrt{4qN_A\epsilon_{S_i}\epsilon_0|\phi_f|}}{C_{ox}}\left(1 + \frac{Kx_d}{W}\right) + 2|\phi_f| \qquad (3.50)$$

Where, K is the form factor depending on the chosen model shown in figure 3.13 for both sides of the non-uniformly shaped depletion regions.

Table 3.1: Shows different values for the form factor K.

Type	Circle	Triangular
Shape	X_d 	X_d 
Form-factor K	$\frac{\pi}{4}$	$X_d/2$

The term of the threshold voltage V_T can be modified by adding the narrow-width effect voltage ΔV_{TNWE},

$$\Delta V_{TNWE} = \frac{1}{C_{ox}} \sqrt{2qN_A \epsilon_{S_i} \epsilon_0 (2|\phi_f|)} \left(\frac{Kx_d}{W}\right) \tag{3.51}$$

3.2.7 Parasitic Bipolar Effects

Reducing, the channel length L whilst keeping the drain/ source voltage V_{DS} constant increases the maximum electric field experienced by the charge carriers (electrons) near the drain region. Energetic charge carriers can create new electron-hole pairs by impact ionization as illustrated in figure 3.13.

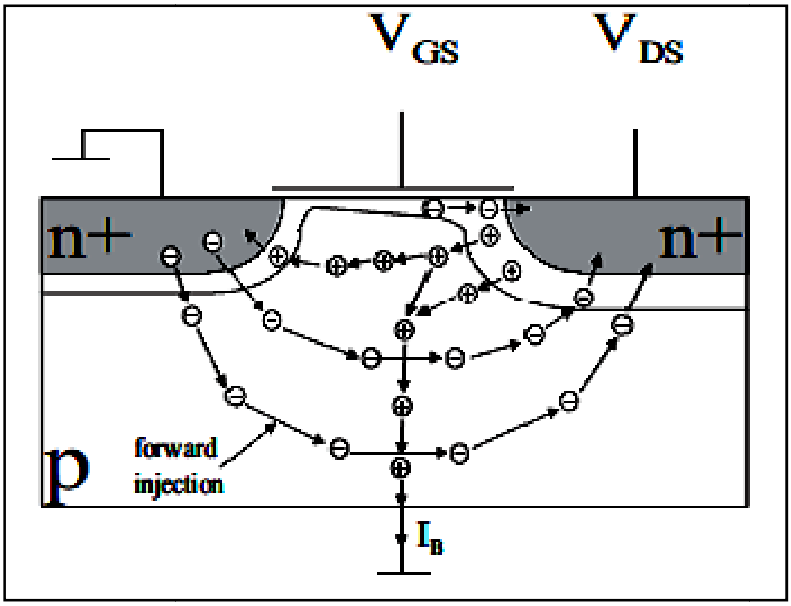

Figure 3.13: Parasitic bipolar transistor action.

Holes injected into the substrate will flow to the substrate contact where they will give rise to a substrate current. This substrate current flow will give rise to voltage drops in the substrate that can cause the forward biasing of the substrate/ source junction. In this case, electrons are injected into the substrate which will be collected by the drain. This effect is known as parasitic bipolar transistor action.

Parasitic bipolar transistor action can have significant effects when the substrate contact is remote from the drain or when the substrate is floating. In the latter case, floating body effects occur that seriously influence the behavior of the device.

The severity of the parasitic transistor action is determined by the gain of the bipolar transistor. The gain of a bipolar transistor is given by the ratio of the collector current I_C and the base current I_B as follows,

$$\beta = \frac{I_C}{I_B} \tag{3.52}$$

The base current I_B of the bipolar npn-transistor shown in figure 3.13 is given by, [34]

$$I_B = \frac{q\, A\, D_{pe}\, {n_i}^2}{W_E\, N_{Deff}} \exp\left(\frac{qV_{be}}{kT}\right) \tag{3.53}$$

Where, D_{pe} is the hole diffusion coefficient in the emitter (source), W_E is the emitter depth, N_{Deff} is the effective donor concentration in the emitter and V_{be} the base emitter voltage which is caused by the potential shift in the substrate.

The collector current I_C is given by,

$$I_C = \frac{q\, A\, D_{nb}\, {n_i}^2}{W_B\, N_{Abeff}} \exp\left(\frac{qV_{be}}{kT}\right) \tag{3.54}$$

Where, D_{nb} is the electron diffusion coefficient in the base, W_B the width of the base and N_{Abeff} the effective acceptor concentration in the base.

Substituting equation (3.53) and (3.54) into equation (3.52) gives the gain of the parasitic npn-bipolar transistor as follows,

$$\beta = \frac{D_{nb} W_E\, N_{Deff}}{D_{pe} W_B\, N_{Abeff}} \tag{3.55}$$

CHAPTER 4

SIMULATION METHODOLOGY

4.1 Simulation Overview

The device simulation is done using the commercial device simulator ATLAS-SILVACO. A vertical MOSFETs structure has been simulated with channel length of 100nm, heavily doped drain depth 20nm, lightly doped drain depth 20nm, and with a gate oxide thickness of 2nm. The heavily doped drain and source region were formed using uniform doping concentration of 1×10^{21} / cm^3. The various LDD doping of 5×10^{18} / cm^3, 1×10^{19}/cm^3, 5×10^{19} / cm^3 and 1×10^{20} / cm^3 were used for analysis this device structure. Here the body was p-type and source drain and gate were n-type with uniform concentration. Several body doping concentrations were investigated with values of 1×10^{16} / cm^3, 2×10^{16} / cm^3, 4×10^{16} / cm^3, 6×10^{16} / cm^3, 8×10^{16} / cm^3, 1×10^{17} / cm^3, 2×10^{17} / cm^3, 4×10^{17} / cm^3, 6×10^{17} / cm^3, 8×10^{17} / cm^3 and 1×10^{18} / cm^3.

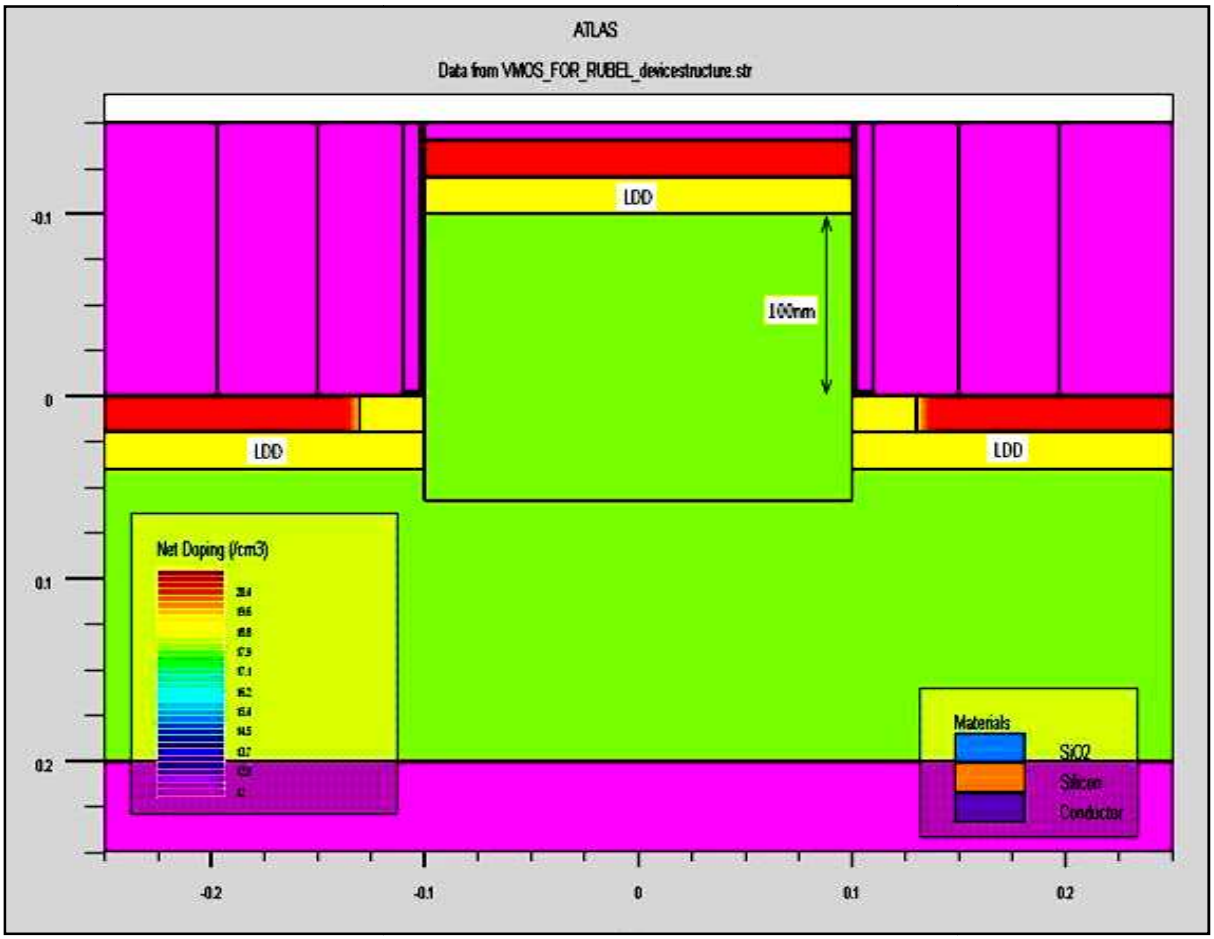

Figure 4.1: Schematic structure of vertical MOSFET.

The created device grid structure is shown below,

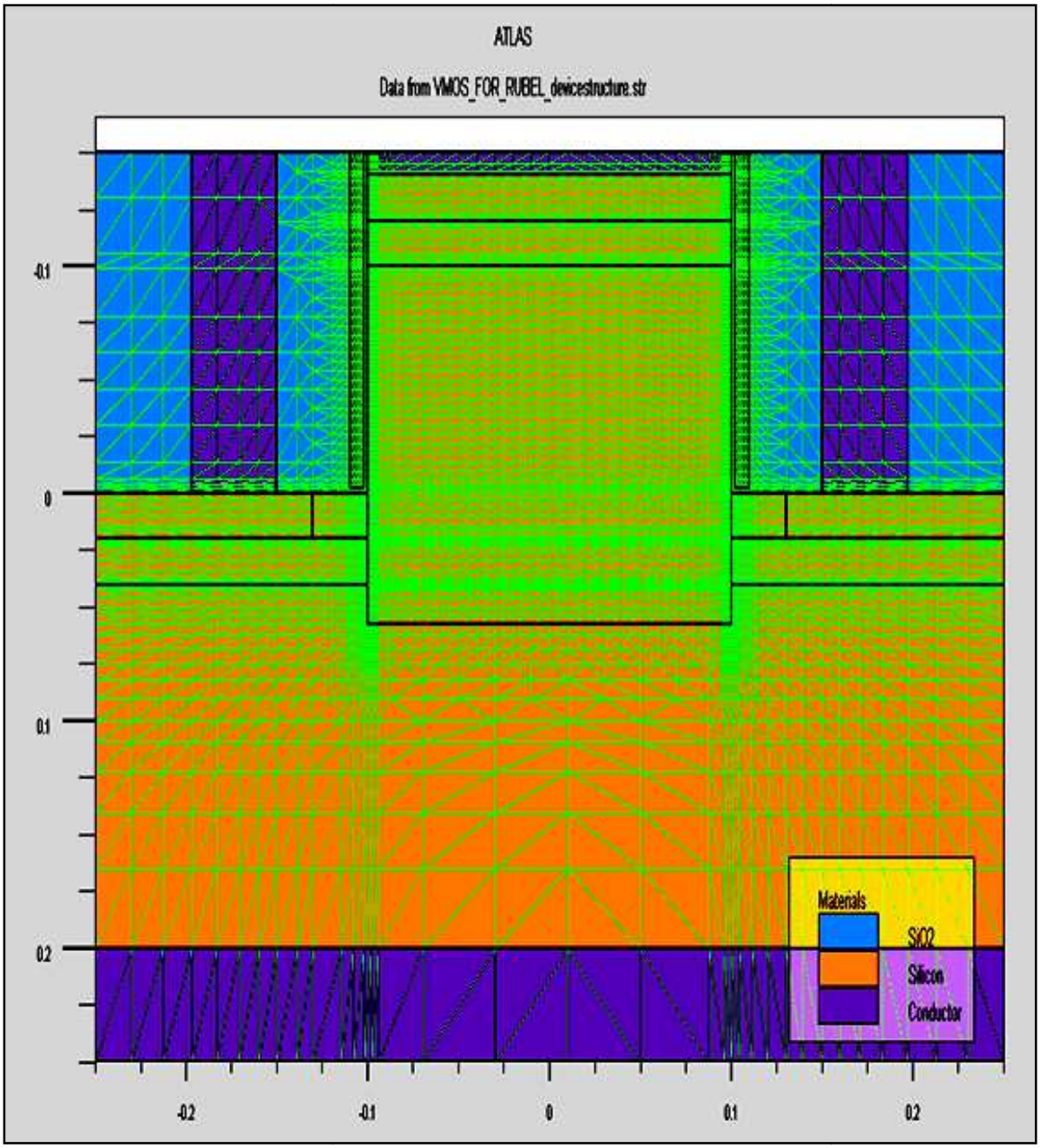

Figure 4.2: Cross-sectional view of vertical MOSFET for 100nm channel length showing the grid density.

To accuratly create the device structure, I ensured adequate mesh density in high field area such as channel region, source, drain and gate junction region. I have taken finer mesh at the interface of heavy doping and the light doping interface. I have removed grid lines from a specified device region where I expect a coarser grid using the ELIMINATE statement. A coarser grid is used at the substrate region in order to reduce simulation run time and achieve more accuracy. Asimple drift-diffution model has been used for simulation.

For this Simulation, I used Fermi-Dirac statistics, giving the probability $f_F(E)$. Mathematically,

$$f_F(E)=\frac{1}{1+\exp(\frac{E-E_F}{kT_L})} \quad (4.1)$$

Where, $f_F(E)$ is called Fermi-Dirac probability function, E_F is Fermi energy level that spatially independent of reference energy and k is the Boltzmann's constant.

It is known that the mobility degradation occurs inside the inversion layers of a MOSFET. This degradation is occurred due to subsequently higher surface scattering near the semiconductor to insulator interface. The effects are acoustic phonon effect, longitudinal electric field effect etc. To handle these effects I have used the most advance model, Lombardi CVT Model [35]. I can select this mode by write down the CVT in input text file at model statement. In the CVT model, the transverse field, doping dependent and temperature dependent parts of the mobility are given by three components that are combined using Mathiessen's rule. These components are surface mobility limited by scattering with acoustic phonons(μ_{AC}), the mobility limited by surface roughness (μ_{sr}), factor and the mobility limited by scattering with optical intervalley phonons (μ_b), are combined using Mathiessen's rule,

$$\mu_T^{-1} = \mu_{AC}^{-1} + \mu_b^{-1} + \mu_{sr}^{-1} \quad (4.2)$$

Where, the first component, acoustic phonons (μ_{AC}) is surface mobility limited by scattering,

$$\mu_{AC.n} = \frac{BN.CVT}{E_\perp} + \frac{CN.CVT\ N^{TAU.CVT}}{T_L E_\perp^{\frac{1}{3}}} \quad (4.3)$$

$$\mu_{AC.p} = \frac{BP.CVT}{E_\perp} + \frac{CP.CVT\ N^{TAUP.CVT}}{T_L E_\perp^{\frac{1}{3}}} \quad (4.4)$$

Where, T_L is the temperature, $E_\perp$ is the perpendicular electric field and N is the total doping concentration. The equation parameters BN.CVT, BP.CVT, CN.CVT, CP.CVT, TAUN.CVT, and TAUP.CVT are specified shown in table 4.1.

Table 4.1: Specified parameters for equation (4.3) to (4.4).

Statement	Parameter	Default	Units
MOBILITY	BN.CVT	4.75×10^{7}	cm/ (s)
MOBILITY	BP.CVT	9.925×10^{4}	cm/ (s)
MOBILITY	CN.CVT	1.74×10^{5}	
MOBILITY	CP.CVT	8.842×10^{5}	
MOBILITY	TAUN.CVT	0.125	
MOBILITY	TAUP.CVT	0.0317	
MOBILITY	GAMN.CVT	2.5	
MOBILITY	GAMP.CVT	2.2	
MOBILITY	MUON.CVT	52.2	cm^2/ (v-s)
MOBILITY	MUOP.CVT	44.9	cm^2/ (v-s)
MOBILITY	MU1N.CVT	43.4	cm^2/ (v-s)
MOBILITY	MU1P.CVT	29.0	cm^2/ (v-s)
MOBILITY	MUMAXN.CVT	1417.0	cm^2/ (v-s)
MOBILITY	MUMAXP.CVT	470.5	cm^2/ (v-s)
MOBILITY	CRN.CVT	9.68×10^{16}	cm^{-3}
MOBILITY	CRP.CVT	2.23×10^{17}	cm^{-3}
MOBILITY	CSN.CVT	3.43×10^{20}	cm^{-3}
MOBILITY	CSP.CVT	6.10×10^{20}	cm^{-3}
MOBILITY	ALPHN.CVT	0.680	
MOBILITY	ALPHP.CVT	0.71	
MOBILITY	BETAN.CVT	2.00	
MOBILITY	BETAP.CVT	2.00	
MOBILITY	PCN.CVT	0.0	cm^{-3}
MOBILITY	PCP.CVT	0.23×10^{16}	cm^{-3}
MOBILITY	DELN.CVT	5.82×10^{14}	V/s
MOBILITY	DELP.CVT	2.054×10^{14}	V^2/s

The second component, surface roughness factor is given by,

$$\mu_{sr} = \frac{\text{DELN.CVT}}{E_{\perp}^{2}} \tag{4.5}$$

$$\mu_{sr} = \frac{\text{DELP.CVT}}{E_{\perp}^{2}} \tag{4.6}$$

Here, the equation parameters DELN.CVT and DELP.CVT had also the defaults shown in table 4.1.

And finally, the third mobility component, is mobility limited by scattering with optical intervalley phonons is given by,

$$\mu_{b.n} = \mathrm{MU0N.CVT}\exp\left(\frac{-\mathrm{PCN.CVT}}{N}\right) + \frac{\left[\mathrm{MUMAXN.CVT}\left(\frac{T_L}{300}\right)^{-\mathrm{GAMN.CVT}} - \mathrm{MU0N.CVT}\right]}{1+\left(\frac{N}{\mathrm{CRN.CVT}}\right)^{\mathrm{ALPHN.CVT}}} - \frac{\mathrm{MU1N.CVT}}{1+\left(\frac{\mathrm{CSN.CVT}}{N}\right)^{\mathrm{BETAN.CVT}}} \quad (4.7)$$

$$\mu_{b.p} = \mathrm{MU0P.CVT}\exp\left(\frac{-\mathrm{PCP.CVT}}{N}\right) + \frac{\left[\mathrm{MUMAXP.CVT}\left(\frac{T_L}{300}\right)^{-\mathrm{GAMP.CVT}} - \mathrm{MU0P.CVT}\right]}{1+\left(\frac{N}{\mathrm{CRP.CVT}}\right)^{\mathrm{ALPHP.CVT}}} - \frac{\mathrm{MU1N.CVT}}{1+\left(\frac{\mathrm{CSP.CVT}}{N}\right)^{\mathrm{BETAP.CVT}}} \quad (4.8)$$

It is known that the band gap of Si gets changed when doping concentration is greater than 1e18/cc. The conduction band is lowered by approximately the same quantity as the valence band is raised.

ATLAS allows such a band gap narrowing effects by specifying the BGN parameter of the MODELS statement. An analytic expression of band gap narrowing effect is as follows.

$$\Delta Eg = \mathrm{BGN.E}\left\{\ln\frac{N}{\mathrm{BGN.N}} + \left[\left(\ln\frac{N}{\mathrm{BGN.N}}\right)^2 + \mathrm{BGN.C}\right]^{\frac{1}{2}}\right\} \quad (4.10)$$

Which has been taken from Slotboom and de Graaf's analytical expression of band gap narrowing effect.[36].

The parameters BGN.E, BGN.N and BGN.C were default values shown in table 4.2.

Table 4.2: Specified parameters of Band gap Narrowing Model for equation (4.10).

Statement	Parameter	Default	Units
MATERIAL	BGM.E	9.0×10^{-3}	V
MATERIAL	BGN.N	1.0×10^{17}	cm^{-3}
MATERIAL	BGN.C	0.5	-

For carrier generation and recombination, I used Shockley-Read-Hall (SHR) recombination model in my device simulation. The mathematical model of Shockley-Read-Hall recombination is as follows,

$$R_{SRH} = \frac{pn - n_{ie}^2}{TAUPO\left[n + n_{ie}\exp\left(\frac{ETRAP}{kT_L}\right)\right] + TAUNO\left[p + n_{ie}\exp\left(\frac{-ETRAP}{kT_L}\right)\right]} \quad (4.11)$$

Where, ETRAP is the difference between the trap energy level and the intrinsic Fermi level.

TAUNO is the electron lifetime and TAUPO is the hole life time. This model is activated in ATLAS software by write down SHR at MODEL statement. As TAUPO and TAUNO parameters are user definable on the material statement although I used default values of carrier lifetimes are given table 4.3.

Table 4.3: Specified parameter for equation (4.11).

Statement	Parameter	Default	Units
METERIAL	ETRAP	0	eV
METERIAL	TAUNO	1.0×10^{-7}	S
METERIAL	TAUPO	1.0×10^{-7}	S

The electron and hole lifetimes τ_n and τ_p respectively are concentration dependent. The constant carrier lifetimes are applied to make a function of impurity concentration using the equation,

$$R_{SRH} = \frac{pn - n_{ie}^2}{\tau_p\left[n + n_{ie}\exp\left(\frac{ETRAP}{kT_L}\right)\right] + \tau_n\left[p + n_{ie}\exp\left(\frac{-ETRAP}{kT_L}\right)\right]} \quad (4.12)$$

$$\tau_n = \frac{TAUN0}{1 + \frac{N}{(NSRHN)}} \quad (4.13)$$

$$\tau_p = \frac{TAUP0}{1 + \frac{N}{(NSRHP)}} \quad (4.14)$$

Where, N is the local (total) impurity concentration. The parameters TAUN0, TAUP0, NSRHN and NSRHP having default values shown in table 4.4.

Table 4.4: Default parameters for equations (4.10) to (4.12).

Statement	Parameter	Default	Units
METERIAL	TAUNO	1.0×10^{-7}	S
METERIAL	NSRHN	5.0×10^{16}	cm^{-3}
METERIAL	TAUPO	1.0×10^{-7}	S
METERIAL	NSRHP	5.0×10^{16}	cm^{-3}

CHAPTER 5

ELECTRICAL RESULTS

This chapter describes the effect of LDD on some key parameters of vertical MOSFETs. I extract device drive current, sub-threshold slope, drain induced barrier lowering (DIBL) and threshold voltage from output characteristics and transfer characteristics respectively for various LDD and body doping for a 100nm vertical MOSFETs. I observe that due to increase of the LDD doping the drive current of the device is increased but sub-threshold slope and DIBL are degraded. Moreover, it is also observed that the threshold voltage decreases at a minimum rate with the increase of LDD doping. These results are summarized below.

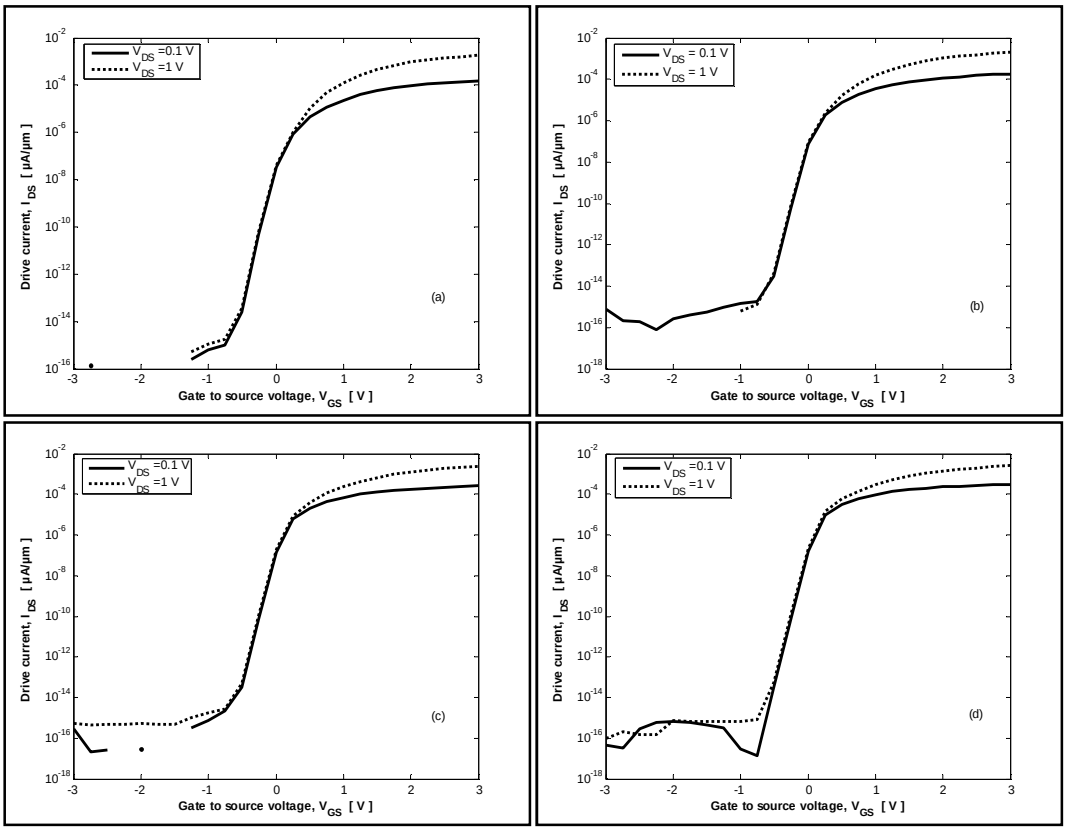

Figure 5.1: Transfer characteristics of 100nm vertical MOSFETs for body doping of 1×10^{18} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) 1×10^{20}/cm^3.

Figure 5.1 shows the transfer characteristics of the vertical MOSFETs for a body doping of 1×10^{18}/cm^3 at various LDD doping of 5×10^{18} / cm^3,1×10^{19}/cm^3 ,5×10^{19}/cm^3 and 1×10^{20} / cm^3. I found that for LDD doping 5×10^{18} / cm^3(Figure 5.1 (a)), the sub-threshold slope of the device is 82.28 [mV/dec], DIBL is 6.11 [mV/V] and threshold voltage

is 1.153 V. For the highest value of LDD doping of 1×10^{20} / cm^3, the sub-threshold slope of the device is 86.77 [mV/dec], DIBL is 15.78 [mV/V] and threshold voltage is 0.8545V. These extracted values are shown in table 5.1.

Table 5.1: Device parameters for body doping 1×10^{18} / cm^3 at different LDD.

BODY Doping [cm^{-3}]	**LDD Doping** [cm^{-3}]	$\mathbf{V_G}$ [V]	$\mathbf{V_T}$ [V] ($\mathbf{V_{DS}}$=1V) ($\mathbf{I_{DS}}$=0.13mA)	**S** [mV/dec] When ($\mathbf{V_{DS}}$=0.1V&1V)	**DIBL** [mV/V] ($\mathbf{I_D}$=10^{-8}A) ($\mathbf{V_{DS}}$=0.1V&1V)
1×10^{18}	1×10^{20}	-3 to 3	0.8545	86.77	15.78
1×10^{18}	5×10^{19}	-3 to 3	0.95	85.51	15
1×10^{18}	1×10^{19}	-3 to 3	1.093	83.35	9.78
1×10^{18}	5×10^{18}	-3 to 3	1.153	82.28	6.11

As can be seen from the table 5.1 with the increase of LDD doping devices sub-threshold performance is slightly degraded. In addition to this a slight reduction in threshold voltage can also be observed with the increase of the LDD doping.

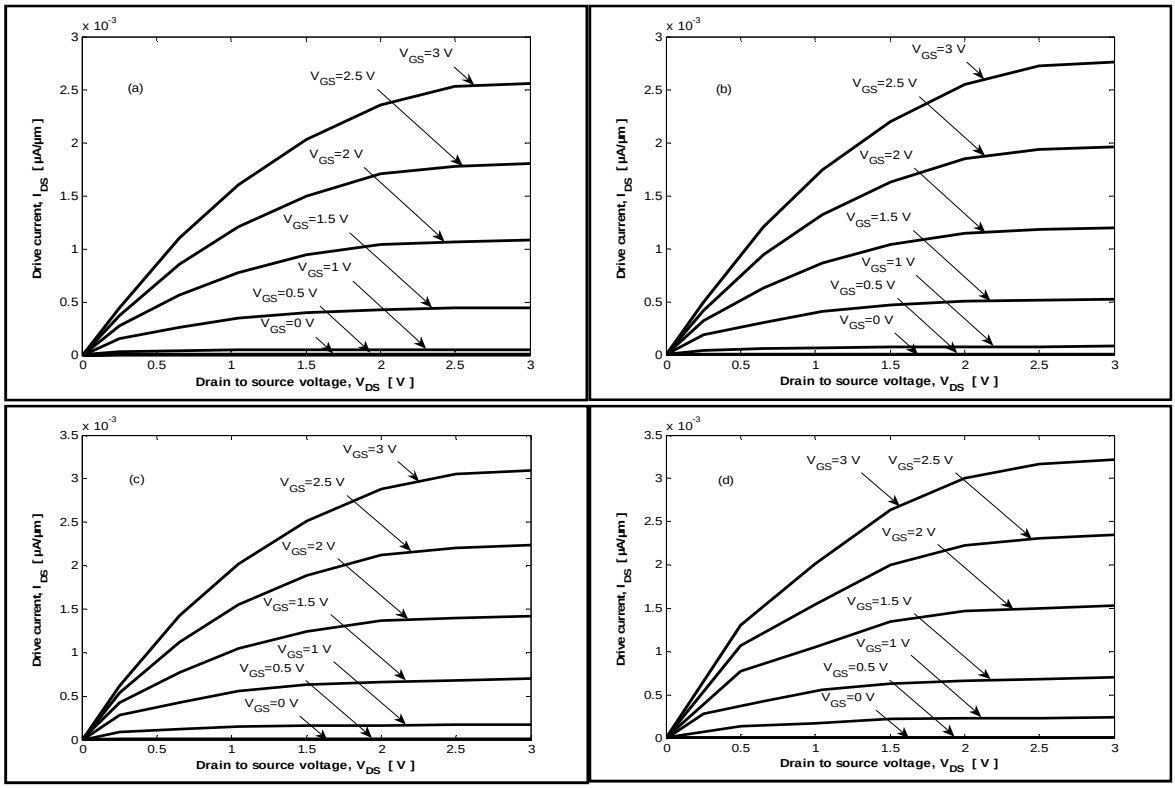

Figure 5.2: Output characteristics of 100nm vertical MOSFETs for body doping of 1×10^{18} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) 1×10^{20}/cm^3.

Figure 5.2 shows the output characteristics for the vertical MOSFETs for 100nm channel length. These output characteristics is obtained of highest body doping (1×10^{18} / cm^3) and for all LDD doping of 5×10^{18} / cm^3, 1×10^{19}/cm^3 , 5×10^{19}/cm^3 and 1×10^{20} / cm^3. From these curves the drive currents are extracted for V_{GS}=3V and V_{DS}=3V. I observed that for the LDD doping of 5×10^{18} / cm^3, the drive current of the device is 2.56 [mA/µm], for the LDD doping of 1×10^{19}/cm^3, the drive current of the device is 2.76 [mA/µm], for the LDD doping of 5×10^{19}/cm^3, the drive current of the device is 3.1[mA/µm], and for the LDD doping of 1×10^{20}/cm^3, the drive current of the device is 3.22 [mA/µm]. It is found that with the increase of the LDD doping the drain current I_D increases.

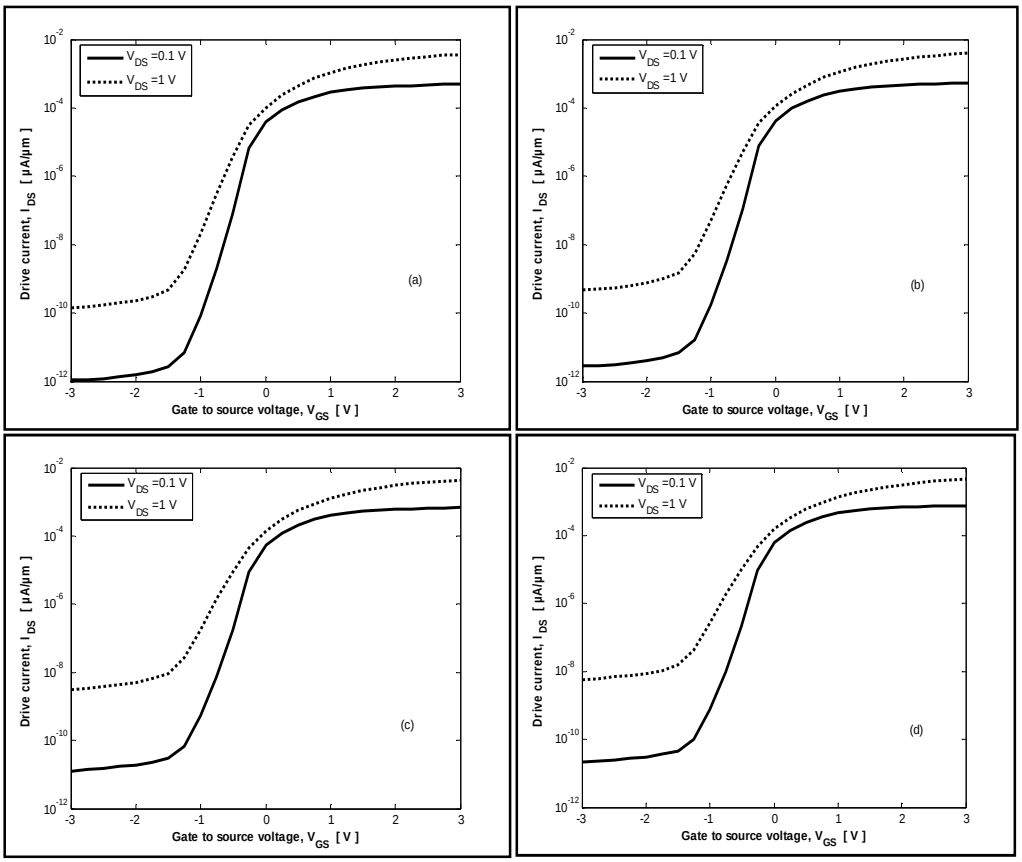

Figure 5.3: Transfer characteristics of 100nm vertical MOSFETs for body doping of 1×10^{16} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) 1×10^{20}/cm^3.

Figure 5.3 shows the transfer characteristics of the vertical MOSFETs for 100nm channel length. These curves are shown for the lowest body doping (1×10^{16} / cm^3) on for LDD doping of 5×10^{18} / cm^3, 1×10^{19}/cm^3 , 5×10^{19} / cm^3 and 1×10^{20} / cm^3. I found that for the LDD doping of 5×10^{18} / cm^3, the sub-threshold slope of the device is 232.22 [mV/dec], DIBL is 451.99 [mV/V] and threshold voltage is 0.2401 [V]. For the LDD doping

of 1×10^{20} / cm^3, the sub-threshold slope of device is 305.29 [mV/dec], DIBL is 700 [mV/V] and threshold voltage is 0.1459 [V]. These extracted values are shown in the following table 5.2.

Table 5.2: Device parameters for body doping 1×10^{16} / cm^3 at different LDD.

BODY Doping [cm^{-3}]	**LDD Doping** [cm^{-3}]	$\mathbf{V_G}$ [V]	$\mathbf{V_T}$ [V] ($\mathbf{V_{DS}}$=1V) ($\mathbf{I_{DS}}$=0.13mA)	**S** [mV/dec] When ($\mathbf{V_{DS}}$=0.1V&1V)	**DIBL** [mV/V] ($\mathbf{I_D}$=10^{-8}A) ($\mathbf{V_{DS}}$=0.1V&1V)
1×10^{16}	1×10^{20}	-3 to 3	0.1459	305.29	700
1×10^{16}	5×10^{19}	-3 to 3	0.1598	294.18	638.78
1×10^{16}	1×10^{19}	-3 to 3	0.2064	256.65	518.56
1×10^{16}	5×10^{18}	-3 to 3	0.2401	232.22	451.99

These results again indicate that with the increase of the LDD doping the sub-threshold slope (S) and DIBL of the device is increased, but the thresholds voltages (V_T) of the device is slightly decreased. It is worth noting that sub-threshold slope (S) and DIBL values are significantly worse at the body doping of 1×10^{16} / cm^3 in comparison to the body doping of 1×10^{18} / cm^3.

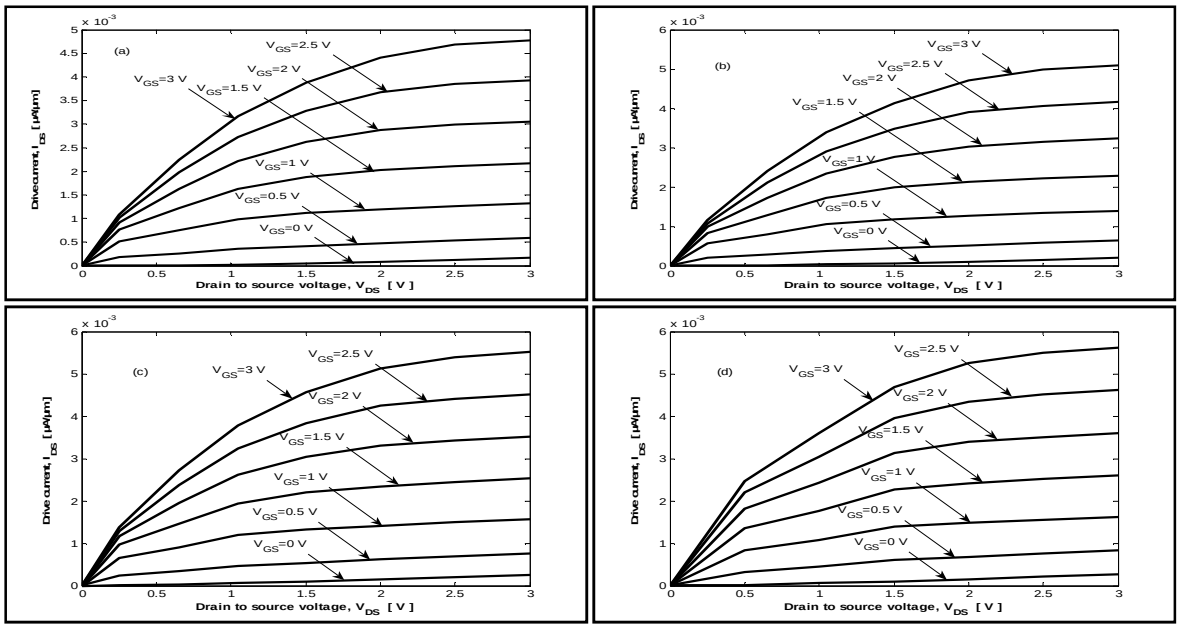

Figure 5.4: Output characteristics of 100nm vertical MOSFETs for body doping of 1×10^{16} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) 1×10^{20}/cm^3.

Figure 5.4 shows the output characteristics for the vertical MOSFETs for 100nm channel length. These output characteristics are presented for the lowest body doping (1×10^{16} / cm^3) and for LDD doping of 5×10^{18} / cm^3, 1×10^{19}/cm^3 , 5×10^{19} /

cm^3 and $1 \times 10^{20} / cm^3$. I found that for the LDD doping of $5 \times 10^{18} / cm^3$ the drive current of the device is 4.69 [mA/µm], for the LDD doping of $1 \times 10^{19} / cm^3$ the drive current of the device is 4.99 [mA/µm], for the LDD doping of $5 \times 10^{19} / cm^3$ the drive current of the device is 5.40 [mA/µm], and for the LDD doping of $1 \times 10^{20} / cm^3$ the drive current of the device is 5.63 [mA/µm]. These results again indicate that with the increase of the LDD doping the drain current I_D is also increases.

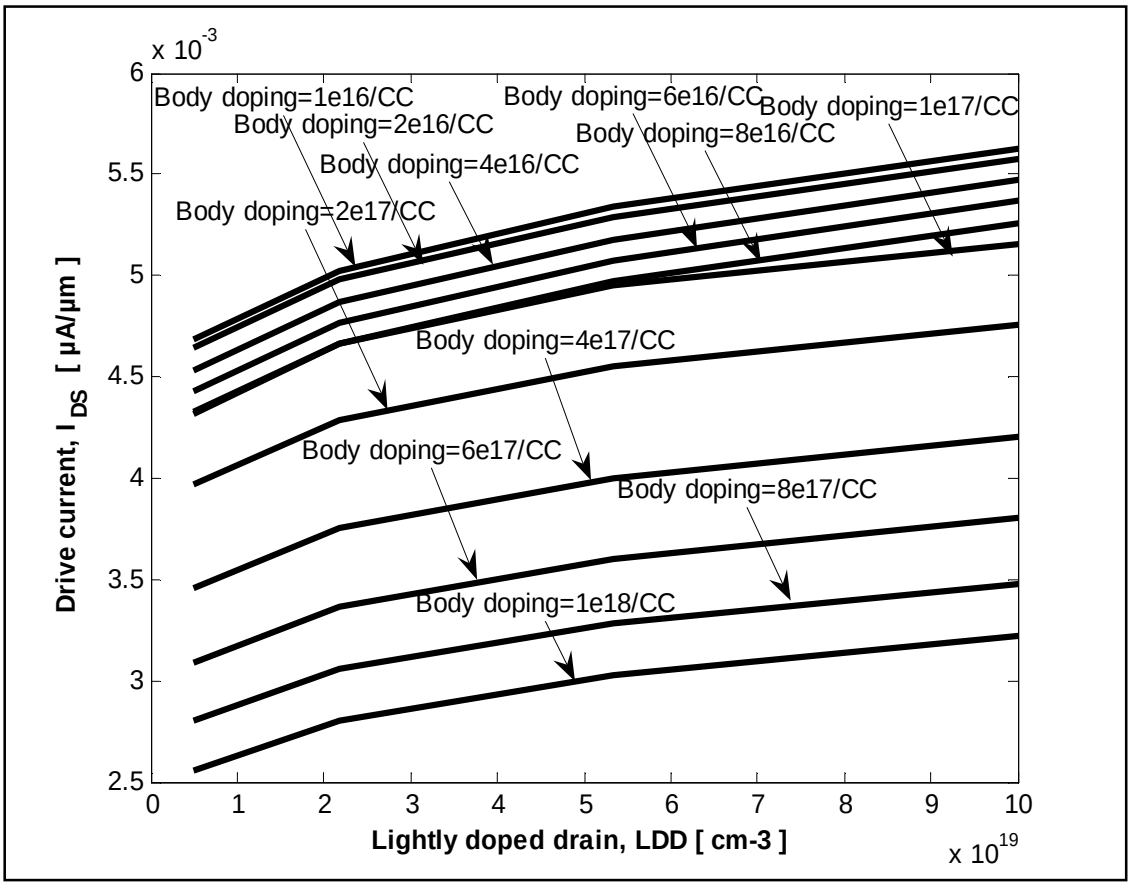

Figure 5.5: Drive current as a function of lightly doped drain (LDD) for different body doping, $1 \times 10^{16} / cm^3$,$2 \times 10^{16} / cm^3$, $4 \times 10^{16} / cm^3$, $6 \times 10^{16} / cm^3$, $8 \times 10^{16} / cm^3$, $1 \times 10^{17} / cm^3$,$2 \times 10^{17} / cm^3$, $4 \times 10^{17} / cm^3$, $6 \times 10^{17} / cm^3$, $8 \times 10^{17} / cm^3$ and $1 \times 10^{18} / cm^3$.

Figure 5.5 shows Drive current as a function of lightly doped drain (LDD) for different body doping, $1 \times 10^{16} / cm^3$, $2 \times 10^{16} / cm^3$, $4 \times 10^{16} / cm^3$, $6 \times 10^{16} / cm^3$, $8 \times 10^{16} / cm^3$, $1 \times 10^{17} / cm^3$, $2 \times 10^{17} / cm^3$, $4 \times 10^{17} / cm^3$, $6 \times 10^{17} / cm^3$, $8 \times 10^{17} / cm^3$ and $1 \times 10^{18} / cm^3$. The drive current are shown for V_{GS}=3V and V_{DS}=3V. It is found that the drive current of the vertical MOSFETs device increases with increasing LDD doping at each body doping. It is also found that drive current of 100nm vertical MOSFETs device also increases with the decrease of body doping.

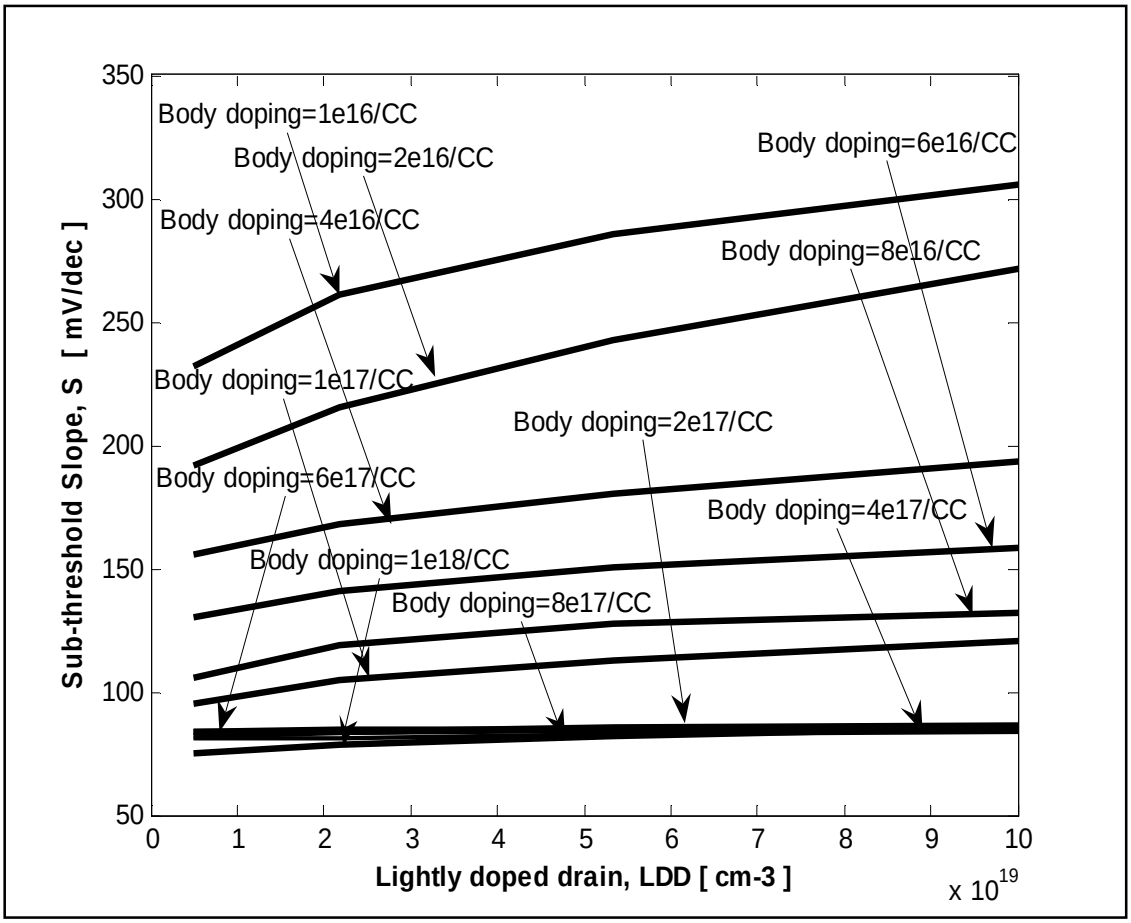

Figure 5.6: Sub-threshold slope as a function of lightly doped drain (LDD) for different body doping of 1×10^{16} / cm^3,2×10^{16} / cm^3, 4×10^{16} / cm^3, 6×10^{16} / cm^3, 8×10^{16} / cm^3, 1×10^{17} / cm^3,2×10^{17} / cm^3, 4×10^{17} / cm^3, 6×10^{17} / cm^3, 8×10^{17} / cm^3 and 1×10^{18} / cm^3.

Figure 5.6 shows sub-threshold slope as a function of lightly doped drain (LDD) for different body doping, 1×10^{16} / cm^3,2×10^{16} / cm^3, 4×10^{16} / cm^3, 6×10^{16} / cm^3, 8×10^{16} / cm^3, 1×10^{17} / cm^3,2×10^{17} / cm^3, 4×10^{17} / cm^3, 6×10^{17} / cm^3, 8×10^{17} / cm^3 and 1×10^{18} / cm^3. It is found that sub-threshold slope gradually degrades with the increase of LDD doping for any fixed body doping. For body doping 1×10^{18} / cm^3 sub-threshold slopes are 82.28 [mV/dec], 83.35 [mV/dec], 85.51 [mV/dec], 86.77 [mV/dec] for LDD doping of 5×10^{18} / cm^3, 1×10^{19}/cm^3 , 5×10^{19} / cm^3& 1×10^{20} / cm^3. For the lowest body doping 1×10^{16} / cm^3 sub-threshold slopes are 232.22 [mV/dec], 256.65 [mV/dec], 294.18 [mV/dec], 305.29 [mV/dec] for the LDD doping of 5×10^{18} / cm^3, 1×10^{19}/cm^3 , 5×10^{19} / cm^{3}and 1×10^{20} / cm^3 respectively. It is worth noting that sub-threshold slope degradation is more prominent at 1×10^{16} / cm^3 body doping in comparison to 1×10^{18} / cm^3 body doping.

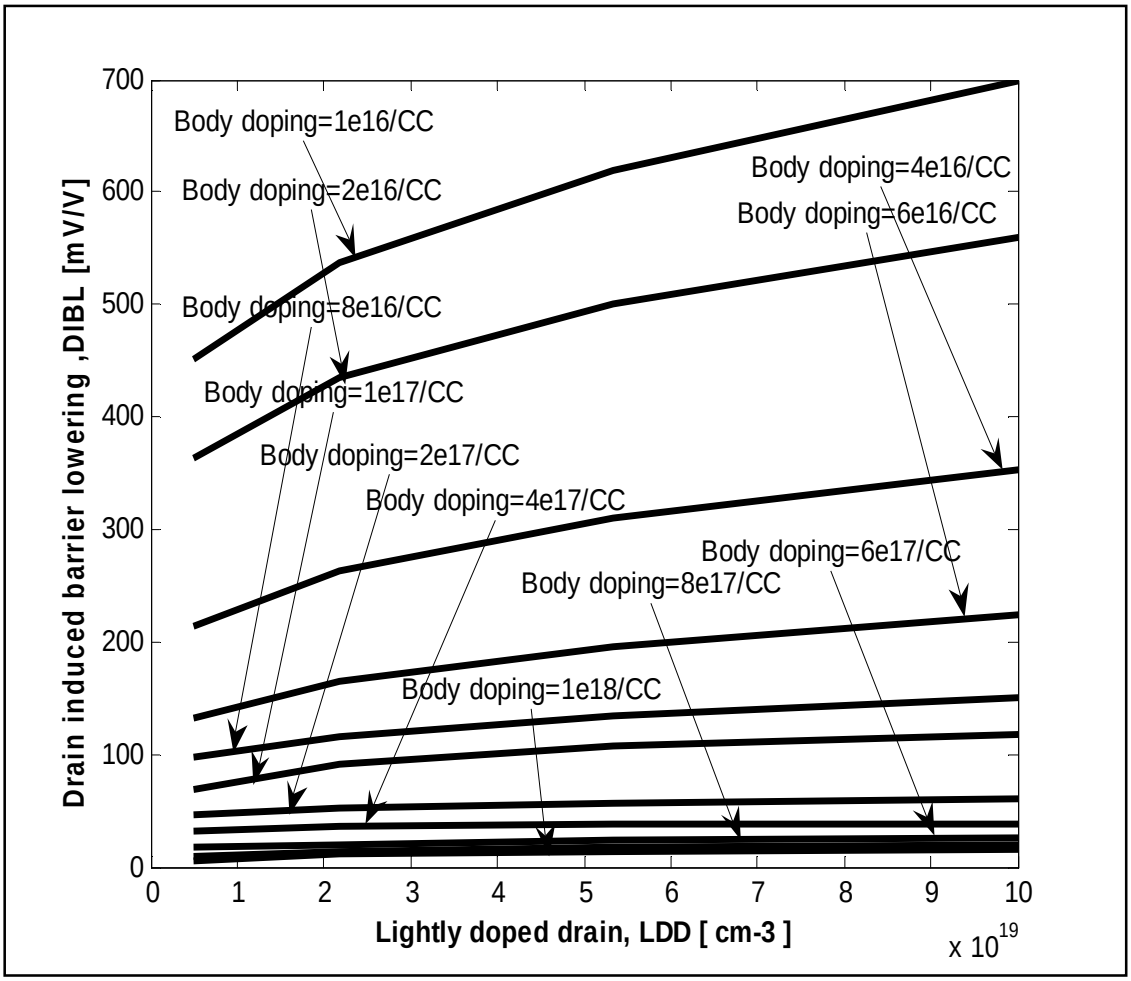

Figure 5.7: Drain induced barrier lowering (DIBL) as a function of lightly doped drain (LDD) for different body doping of 1×10^{16} / cm^3,2×10^{16} / cm^3, 4×10^{16} / cm^3, 6×10^{16} / cm^3, 8×10^{16} / cm^3, 1×10^{17} / cm^3,2×10^{17} / cm^3, 4×10^{17} / cm^3, 6×10^{17} / cm^3, 8×10^{17} / cm^3 and 1×10^{18} / cm^3.

Figure 5.7 shows Drain induced barrier lowering (DIBL) as a function of lightly doped drain (LDD) for different body doping of 1×10^{16} / cm^3,2×10^{16} / cm^3, 4×10^{16} / cm^3, 6×10^{16} / cm^3,8×10^{16} / cm^3,1×10^{17} / cm^3,2×10^{17} / cm^3,4×10^{17} / cm^3,6×10^{17} / cm^3, 8×10^{17} / cm^3 and 1×10^{18} / cm^3. DIBL trend of 100nm vertical MOSFETs device is similar to the sub-threshold slope at different LDD doping. For body doping of 1×10^{18} / cm^3 DIBL values are 6.11 [mV/V], 9.78 [mV/V], 15 [mV/V], and 15.78 [mV/V], for LDD doping of 5×10^{18} / cm^3,1×10^{19}/cm^3 , 5×10^{19} / cm^3 and 1×10^{20} / cm^3 respectively. For the lowest body doping of 1×10^{16} / cm^3 DIBL values are 451.99 [mV/V], 518.56 [mV/V], 638.78 [mV/V], and 700 [mV/V] for LDD doping of 5×10^{18} / cm^3, 1×10^{19}/cm^3 , 5×10^{19} / cm^3 and 1×10^{20} / cm^3 respectively. Again DIBL degradation is more prominent at the body doping 1×10^{16} / cm^3 in comparison to the body doping 1×10^{18} / cm^3.

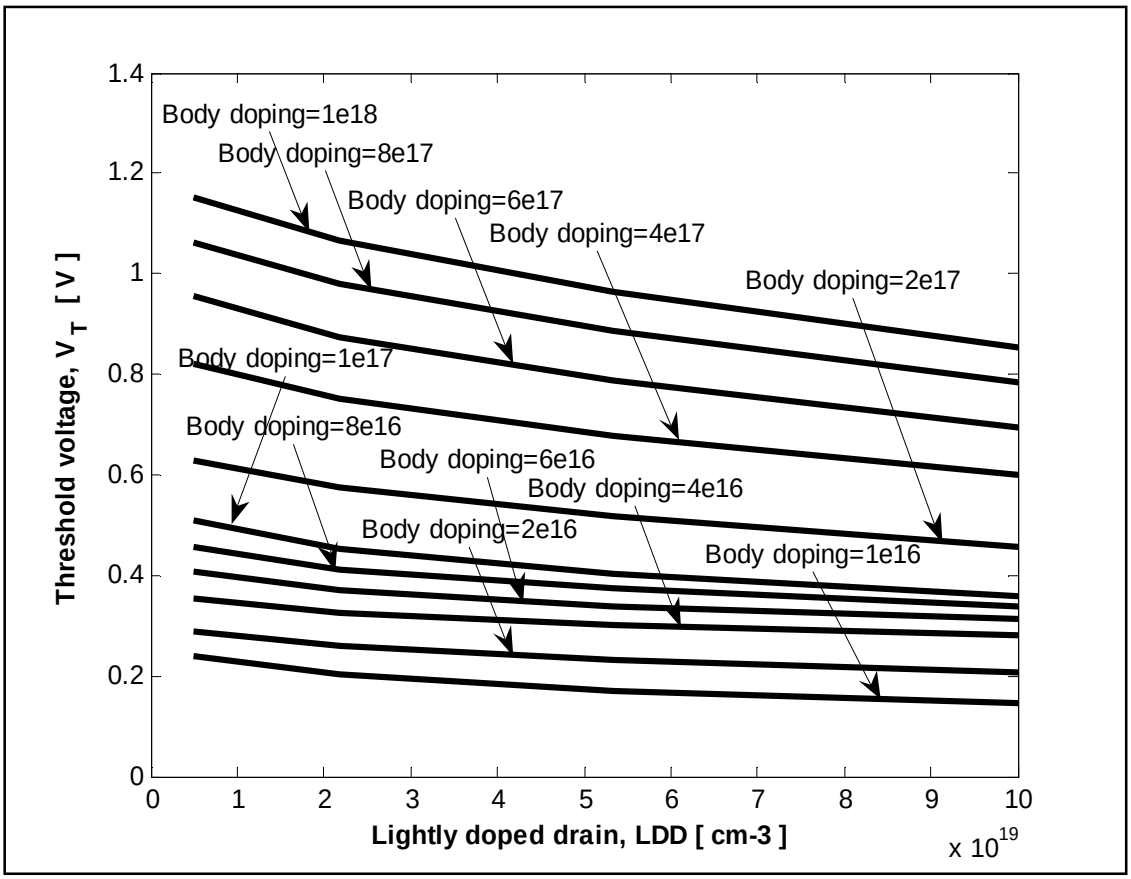

Figure 5.8: Threshold voltage (V_T) as a function of lightly doped drain (LDD) for different body doping of 1×10^{16} / cm^3,2×10^{16} / cm^3, 4×10^{16} / cm^3, 6×10^{16} / cm^3, 8×10^{16} / cm^3, 1×10^{17} / cm^3,2×10^{17} / cm^3, 4×10^{17} / cm^3, 6×10^{17} / cm^3, 8×10^{17} / cm^3 and 1×10^{18} / cm^3.

Finally, figure 5.8 shows Threshold voltage (V_T) as a function of lightly doped drain (LDD) for different body doping of 1×10^{16} / cm^3,2×10^{16} / cm^3, 4×10^{16} / cm^3, 6×10^{16} / cm^3, 8×10^{16} / cm^3, 1×10^{17} / cm^3, 2×10^{17} / cm^3, 4×10^{17} / cm^3, 6×10^{17} / cm^3, 8×10^{17} / cm^3 and 1×10^{18} / cm^3. In contrast to the sub-threshold slope and DIBL threshold voltages of 100nm vertical MOSFETs are found to decrease with the increase of LDD doping. For body doping of 1×10^{18} / cm^3 threshold voltages (V_T) values are 1.153V, 1.093V, 0.95V and 0.8545V, for the LDD doping of 5×10^{18} / cm^3, 1×10^{19}/cm^3 , 5×10^{19} / cm^{3}and 1×10^{20} / cm^3 respectively. For the lowest body doping of 1×10^{16} / cm^3 threshold voltages (V_T) values are 0.2401V, 0.2064V, 0.1598V and 0.1459V, for LDD doping of 5×10^{18} / cm^3, 1×10^{19}/cm^3 , 5×10^{19} / cm^3 and 1×10^{20} / cm^3 respectively. It is worth noting that threshold voltage (V_T) change with LDD doping is more prominent for body doping of 1×10^{18} / cm^3 in comparison to the body doping of 1×10^{16} / cm^3. Which is not similar to the trend observe for sub-threshold slope and DIBL observed in figure 5.6 and figure 5.7.

CHAPTER 6

DISCUSSION

The electrical results which I have elaborately described in chapter 5 exhibits some non-trivial effects of LDD doping on the electrical characteristics of CMOS compatible vertical MOFETs such as sub-threshold slope, drain induced barrier lowering (DIBL), threshold voltage, and drive current. I observed that the drive current I_D is increased due to increase of LDD doping for any fixed body doping. As the source to drain series resistance of the device is reduced due to increase of LDD doping, the drive current is increased at a noticeable amount. In addition to the source/ drain series resistance effective channel length of device also decreases with the increase of LDD doping which also increase the drive current for any fixed body doping. The increase in the drive current for any fixed drain and gate voltages with the decrease of the body doping can be explained by the onset of reduction of threshold voltages and significant reduction of the channel lengths with the decrease of body doping. The degradation of sub-threshold characteristics (sub-threshold slope and DIBL) with the increase of LDD doping is also due to the similar phenomenon of effective channel length reduction with the increase of LDD doping for any fixed body doping. However, this effect is more prominent at low body doping values as effective channel length reduction with the increase of LDD doping is expected to be high. Similar phenomenon can be attributed to the reduction of threshold voltages with the increase of LDD doping.

CHAPTER 7

CONCLUSION

7.1 Thesis Summary

In this thesis, I investigate the effect of the variation of LDD doping in CMOS compatible vertical MOSFETs architecture. It is found that with the increase of LDD doping drive current of vertical MOSFET increases whereas sub-threshold performance is degraded. The degradation of sub-threshold performance is found to be more prominent at low body doping values. In addition to this threshold voltage of vertical MOSFETs are found to decrease with the increase of LDD doping. These effects are explained by the reduction of the effective channel lengths and decrease in the source/ drain series resistances with the increase of LDD doping values. These results are very significant for choosing appropriate body doping and LDD doping values for fabricating 100nm CMOS compatible vertical MOSFETs.

7.2 Limitation of the Work and Possible Future Improvement

- The current simulation has been done using classical drift-diffusion isothermal model in 2D device frame work. More accurate results could be obtained if 3D simulation could be done as CMOS compatible vertical MOSFETs are mainly attractive for surround gate structure with possible corner effects. Current 2D simulation cannot take account of corner effects.
- During my simulation I have not taken any interface states in gate oxide. In fabricated vertical MOSFETs interface states might affect electrical characteristics.
- For HDD and LDD doping I have used constant doping concentrations whereas in real world the doping might have gradient in profile. Gaussian doping profile or creator of device structure in Athena process simulator should make the results more realistic.
- The results would be more accurate if lattice heating effects are taken into account through energy balance model.

APPENDICES

APPENDIX-A

A. Sub-threshold characteristics

A.1: Sub-threshold characteristics at different body doping and LDD doping values.

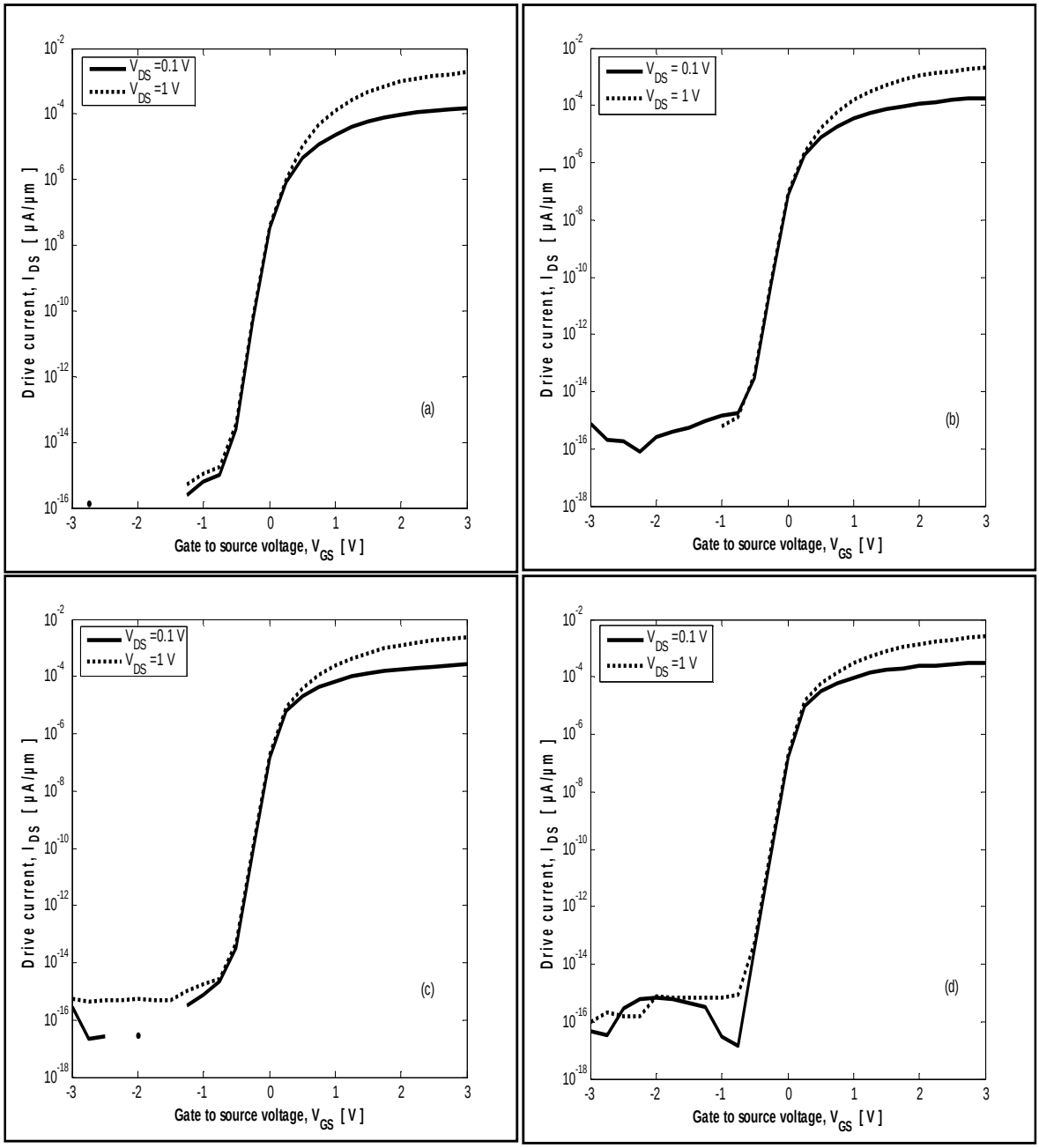

Fig.A$_1$: Transfer characteristics of 100nm vertical MOSFETs for body doping of 1×10^{18} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) $1 \times 10^{20}/cm^3$.

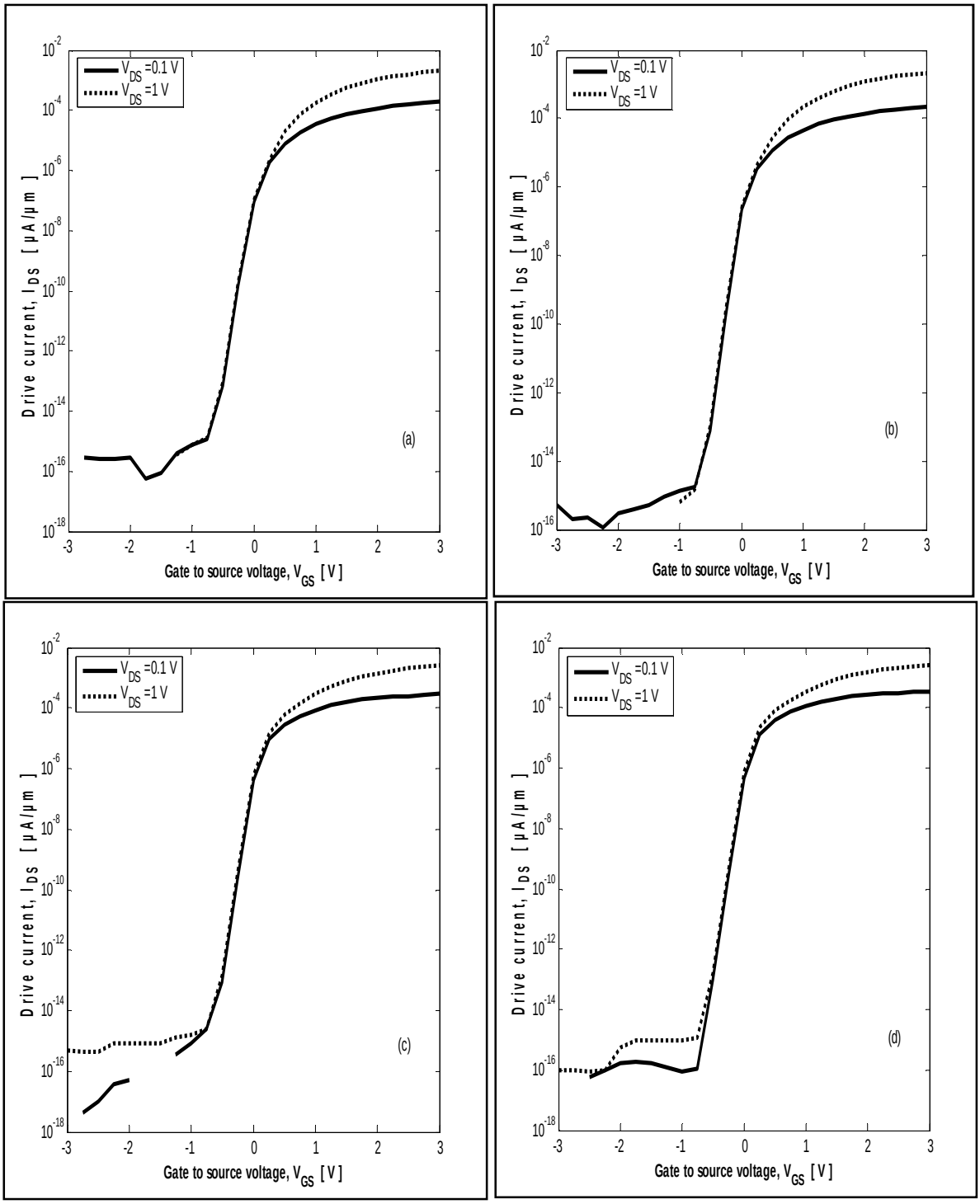

Fig.A$_2$: Transfer characteristics of 100nm vertical MOSFETs for body doping of 8×10^{17} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) $1 \times 10^{20}/cm^3$.

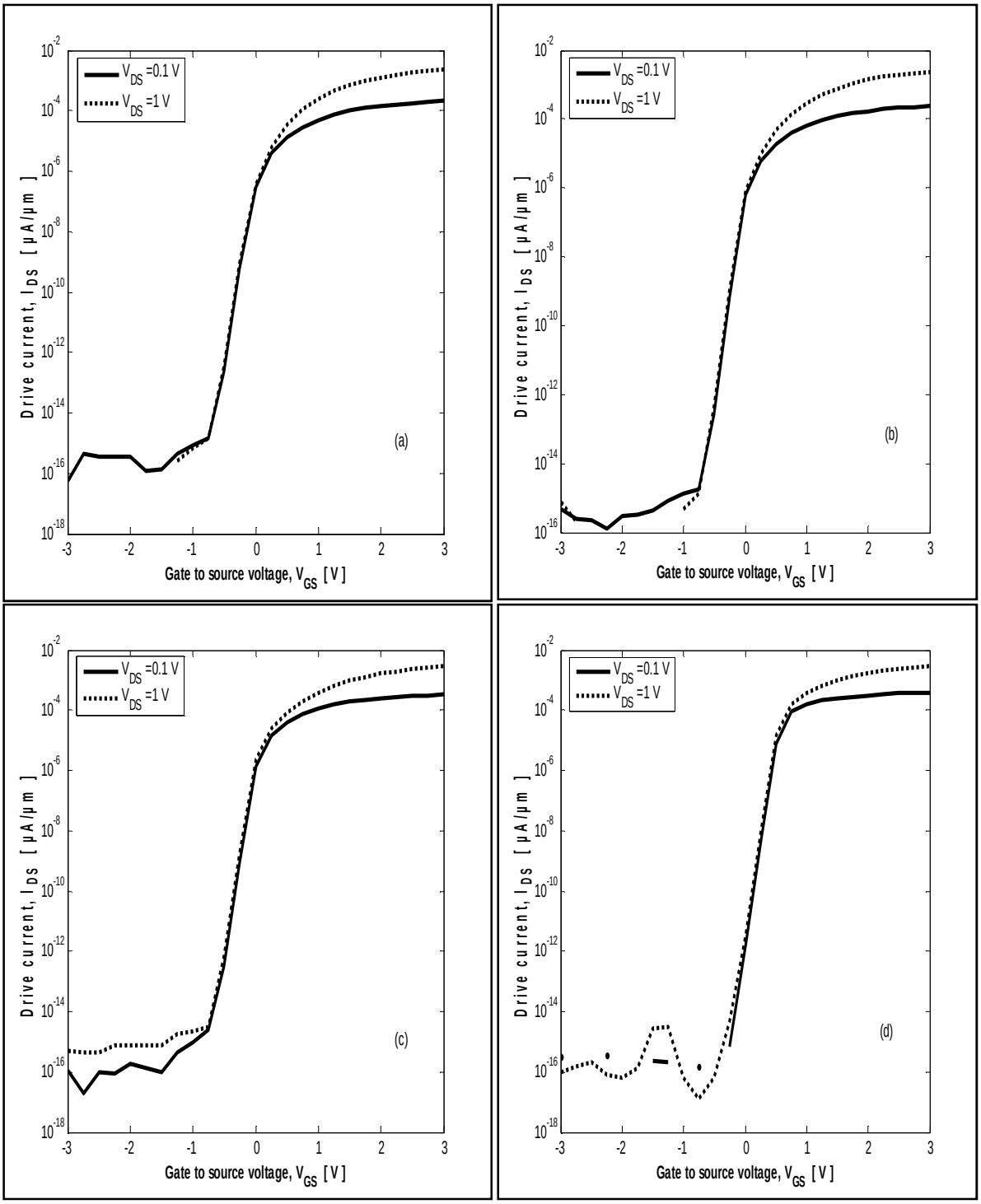

Fig.A$_3$: Transfer characteristics of 100nm vertical MOSFETs for body doping of 6×10^{17} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) $1 \times 10^{20}/cm^3$.

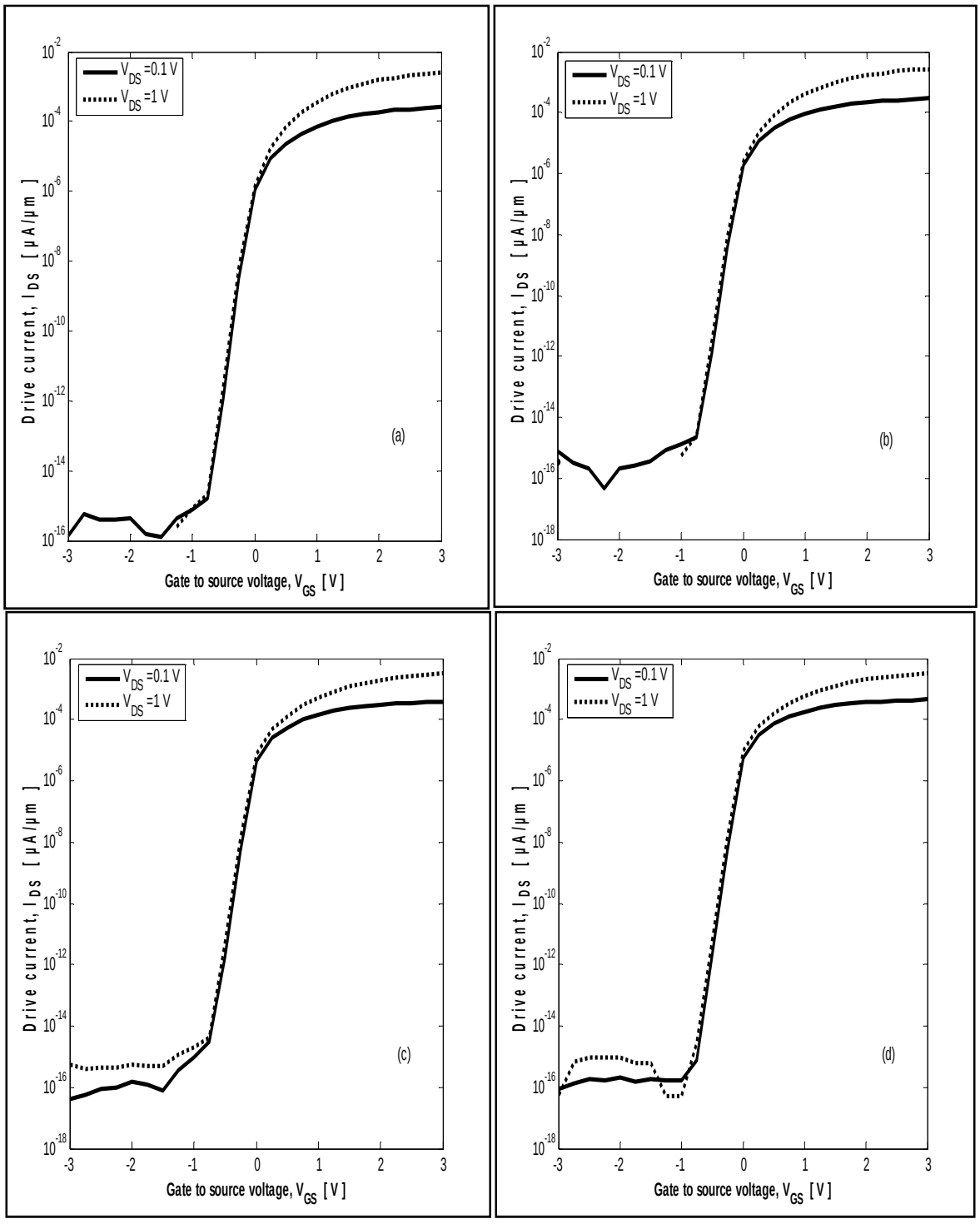

Fig.A$_4$: Transfer characteristics of 100nm vertical MOSFETs for body doping of 4×10^{17} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) $1 \times 10^{20}/cm^3$.

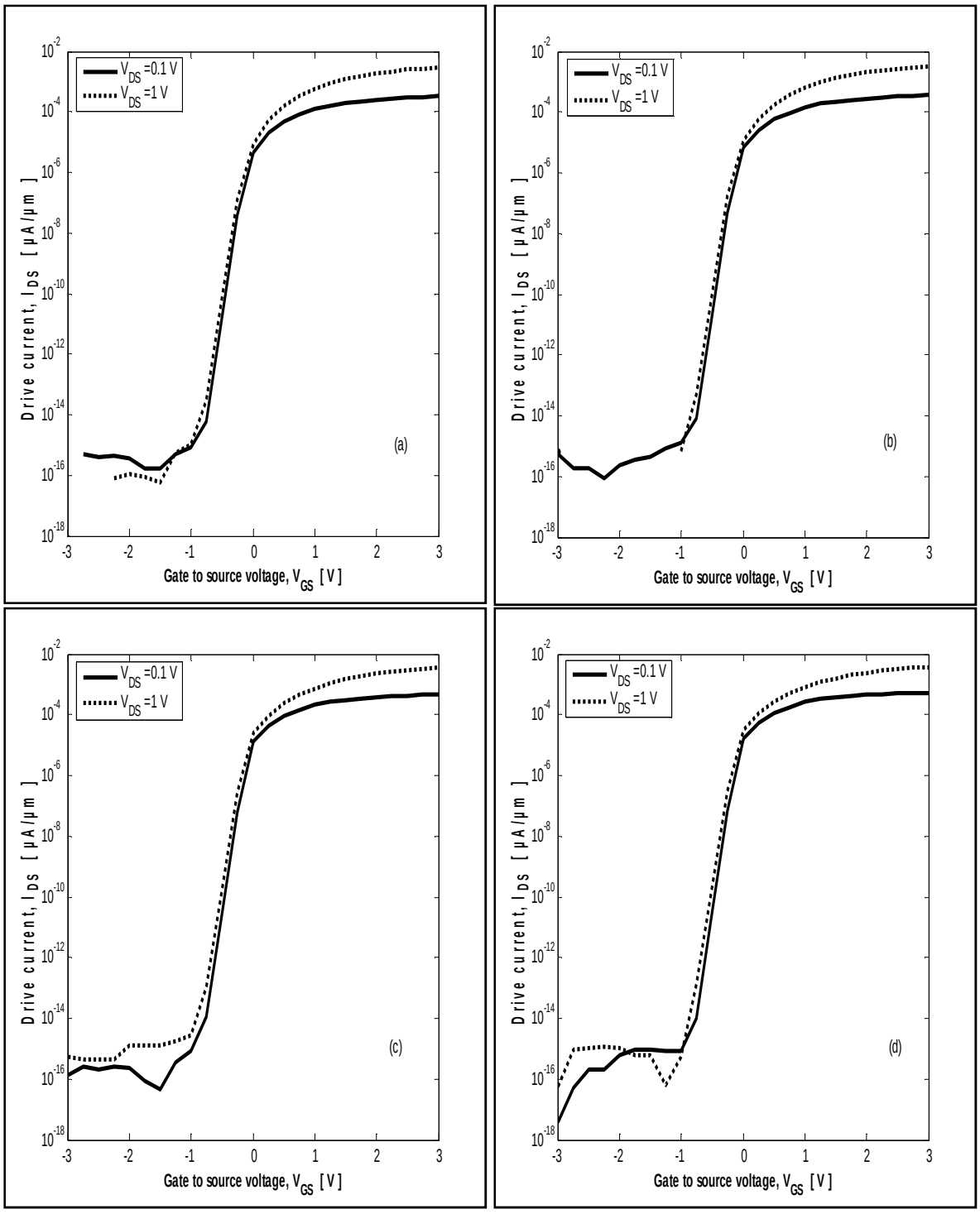

Fig.A$_5$: Transfer characteristics of 100nm vertical MOSFETs for body doping of 2×10^{17} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) $1 \times 10^{20}/cm^3$.

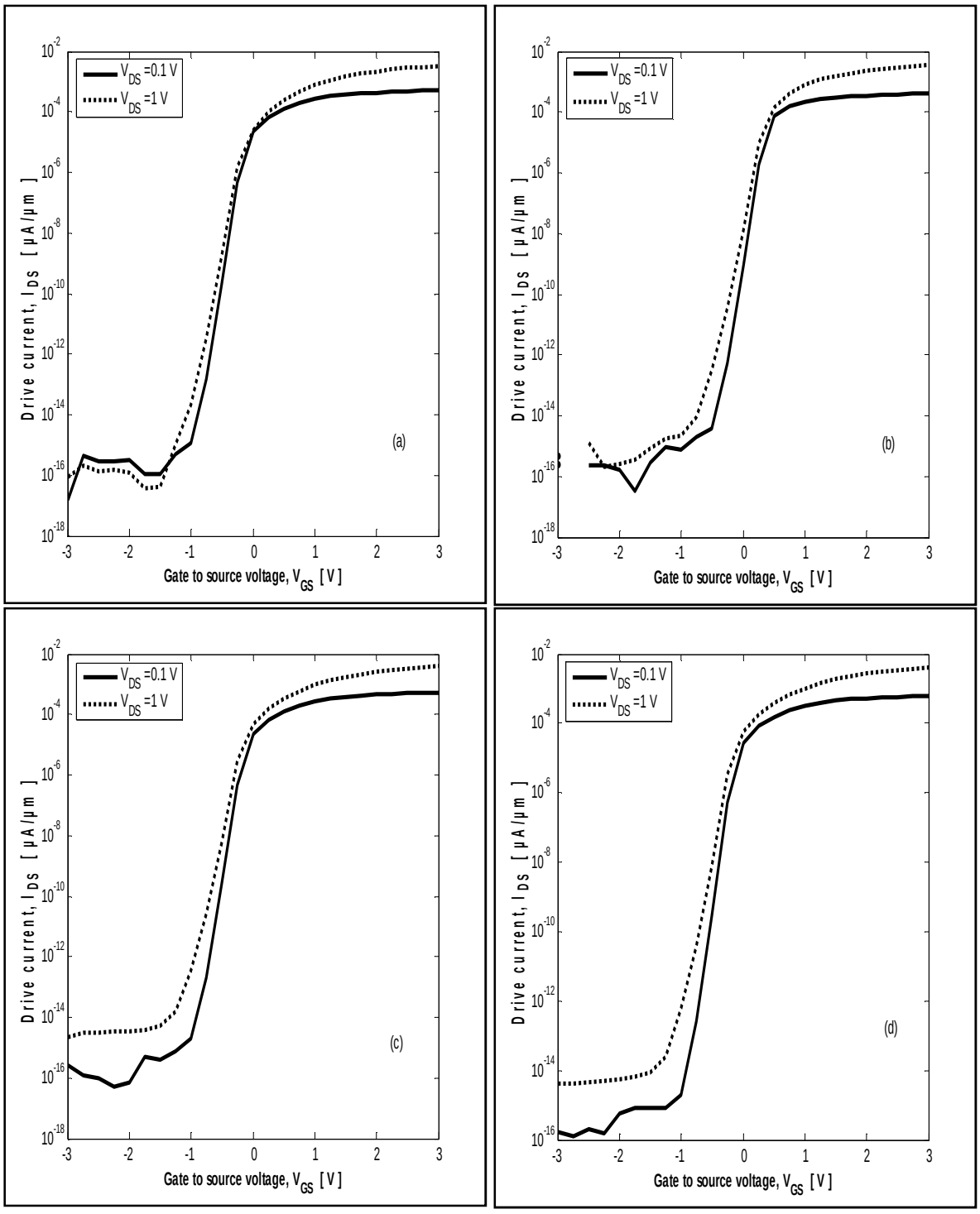

Fig.A$_6$: Transfer characteristics of 100nm vertical MOSFETs for body doping of 1×10^{17} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) $1 \times 10^{20}/cm^3$.

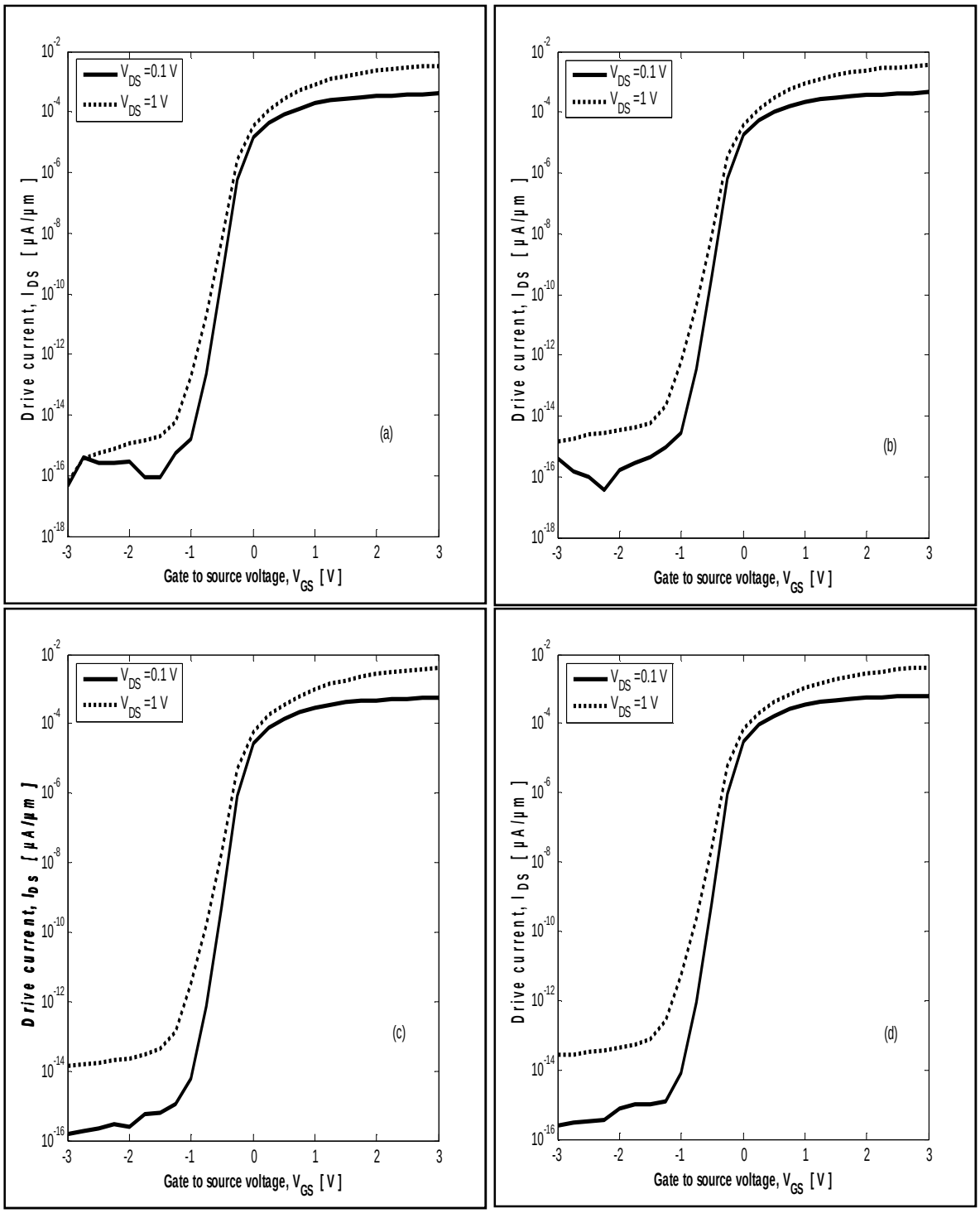

Fig.A$_7$: Transfer characteristics of 100nm vertical MOSFETs for body doping of 8×10^{16} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) $1 \times 10^{20}/cm^3$.

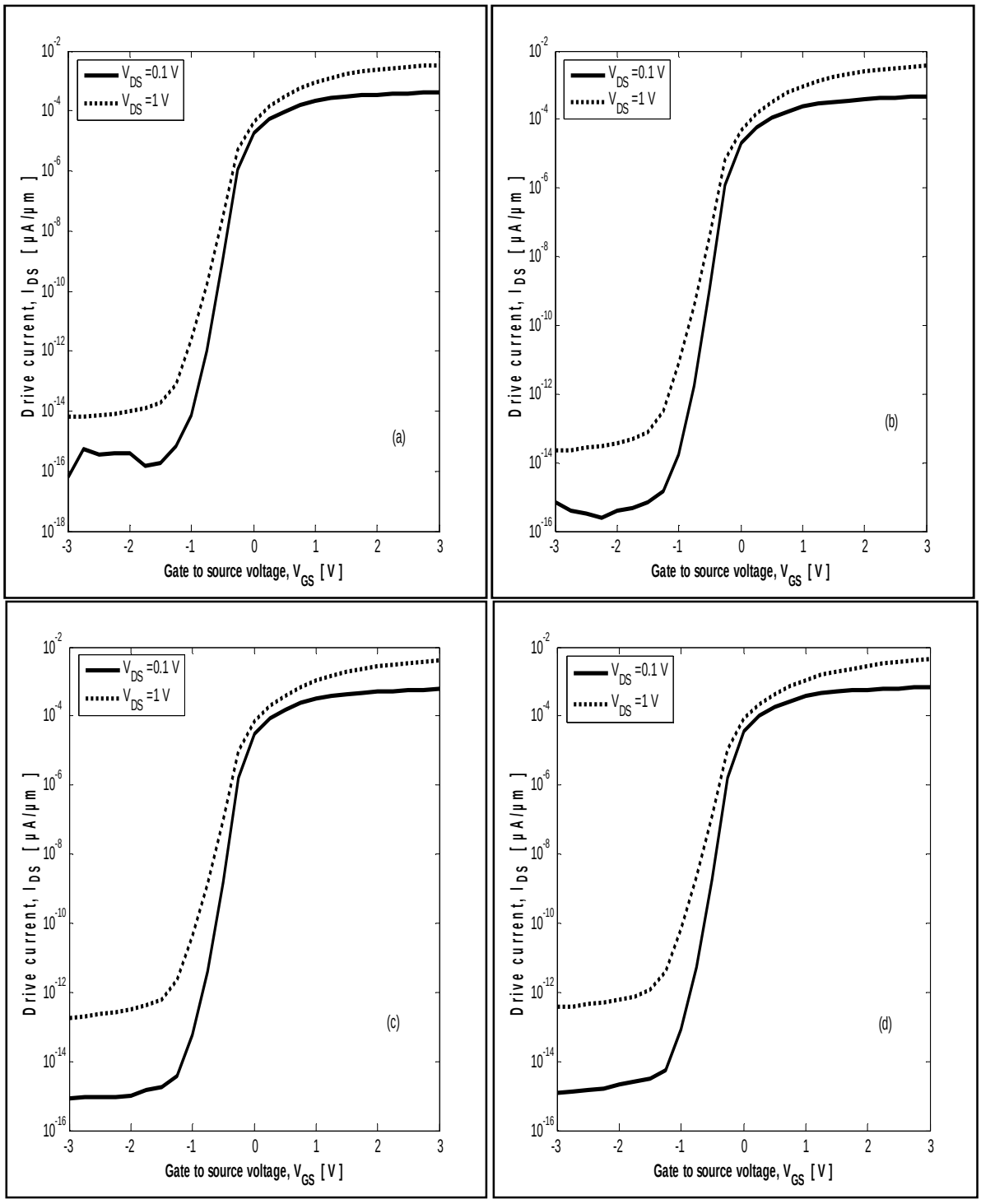

Fig.A$_8$: Transfer characteristics of 100nm vertical MOSFETs for body doping of6×10^{16} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) $1 \times 10^{20}/cm^3$.

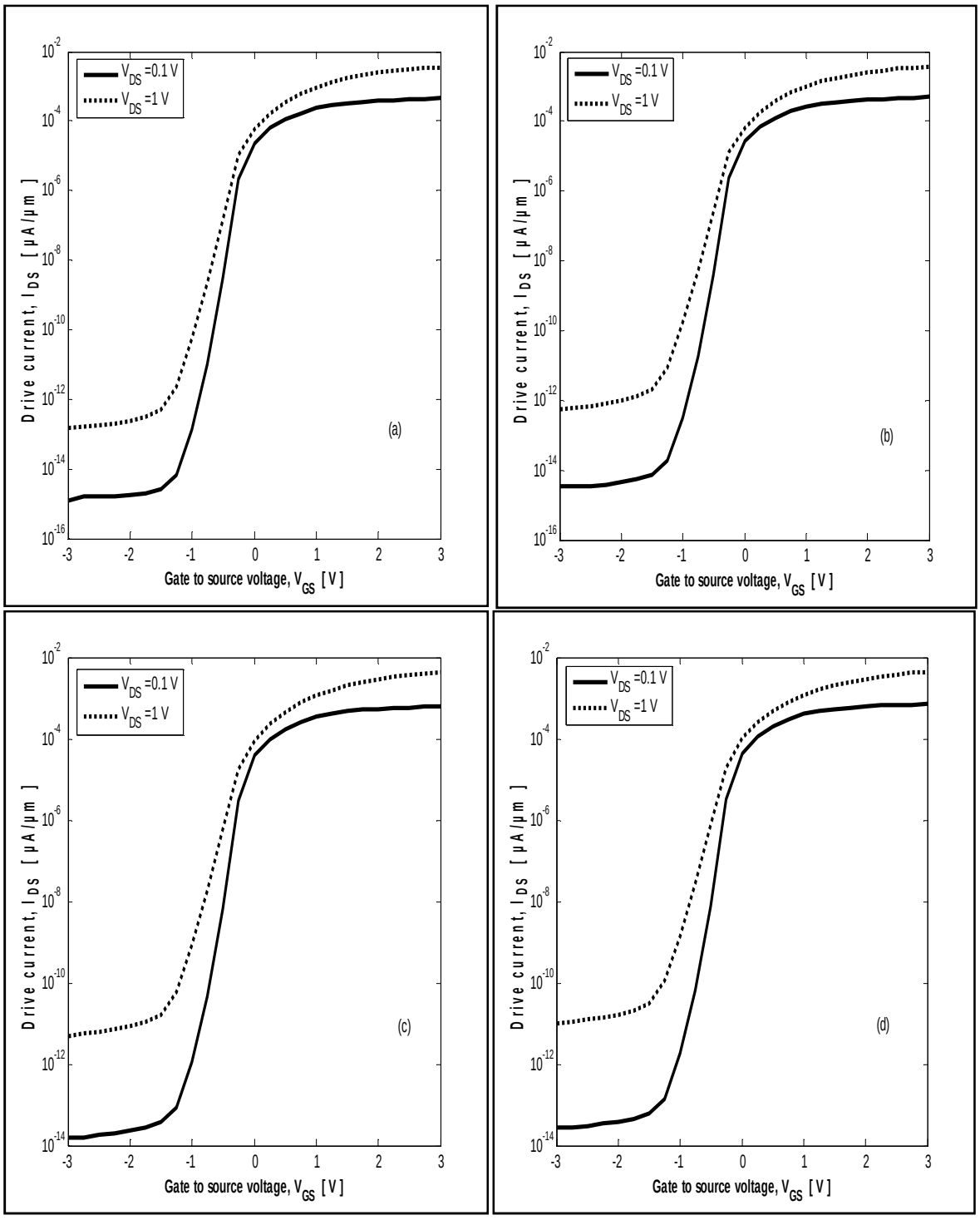

Fig.A$_9$: Transfer characteristics of 100nm vertical MOSFETs for body doping of 4×10^{16} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) $1 \times 10^{20}/cm^3$.

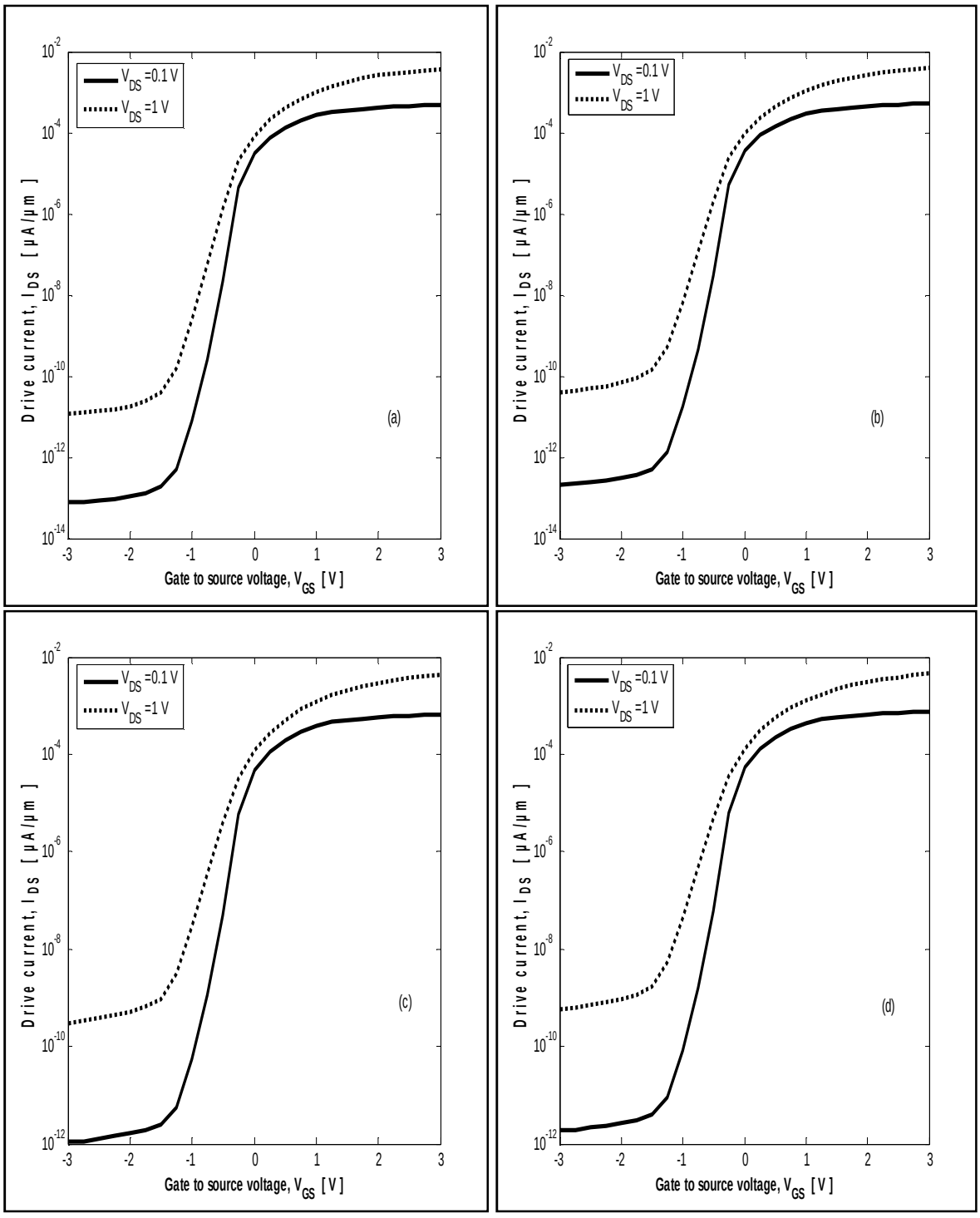

Fig.A$_{10}$: Transfer characteristics of 100nm vertical MOSFETs for body doping of 2×10^{16} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) 1×10^{20}/cm^3.

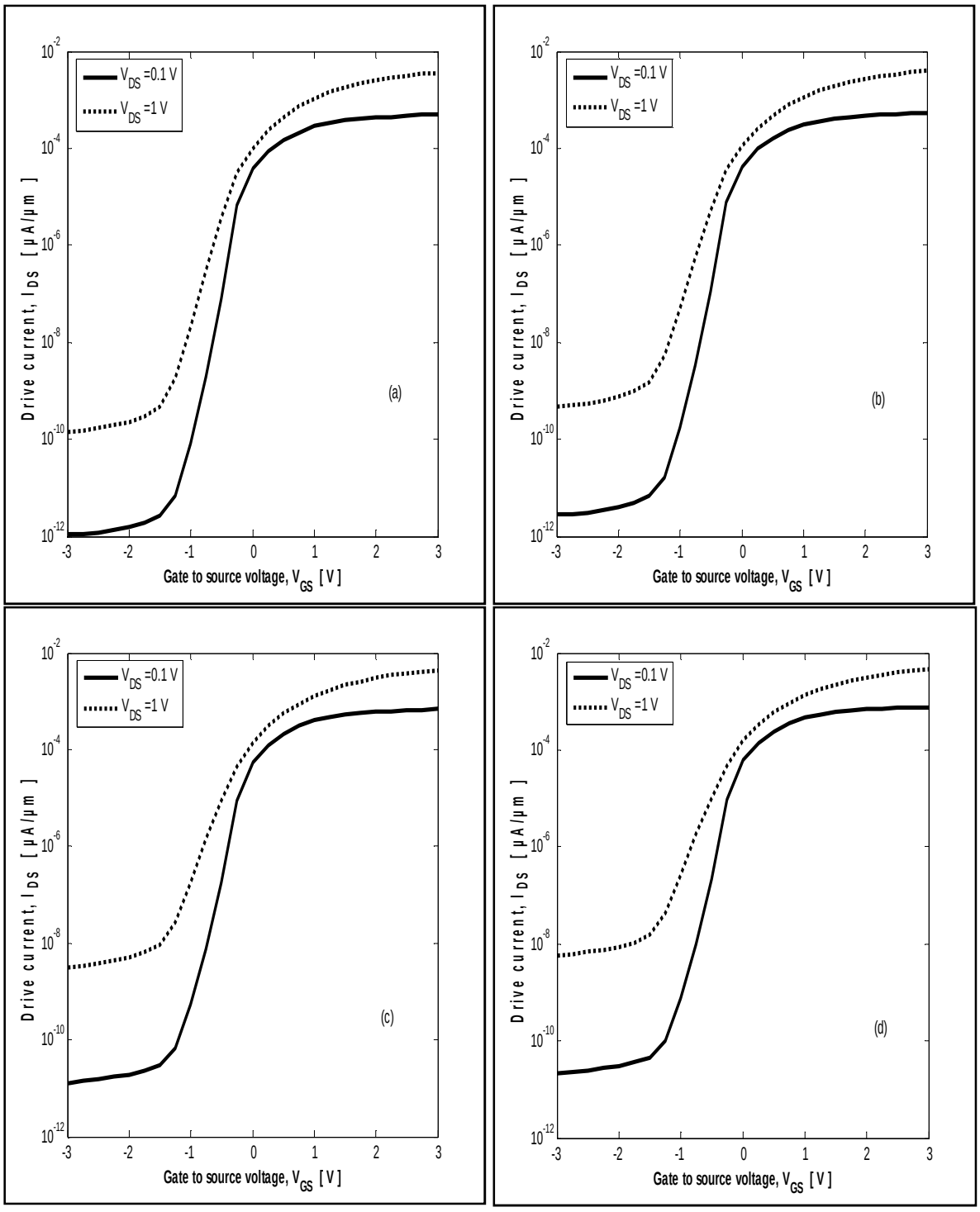

Fig.A$_{11}$: Transfer characteristics of 100nm vertical MOSFETs for body doping of 1×10^{16} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) 1×10^{20}/cm^3.

APPENDIX-B

B. Output characteristics

B.1: Output characteristics at different body doping and LDD doping values.

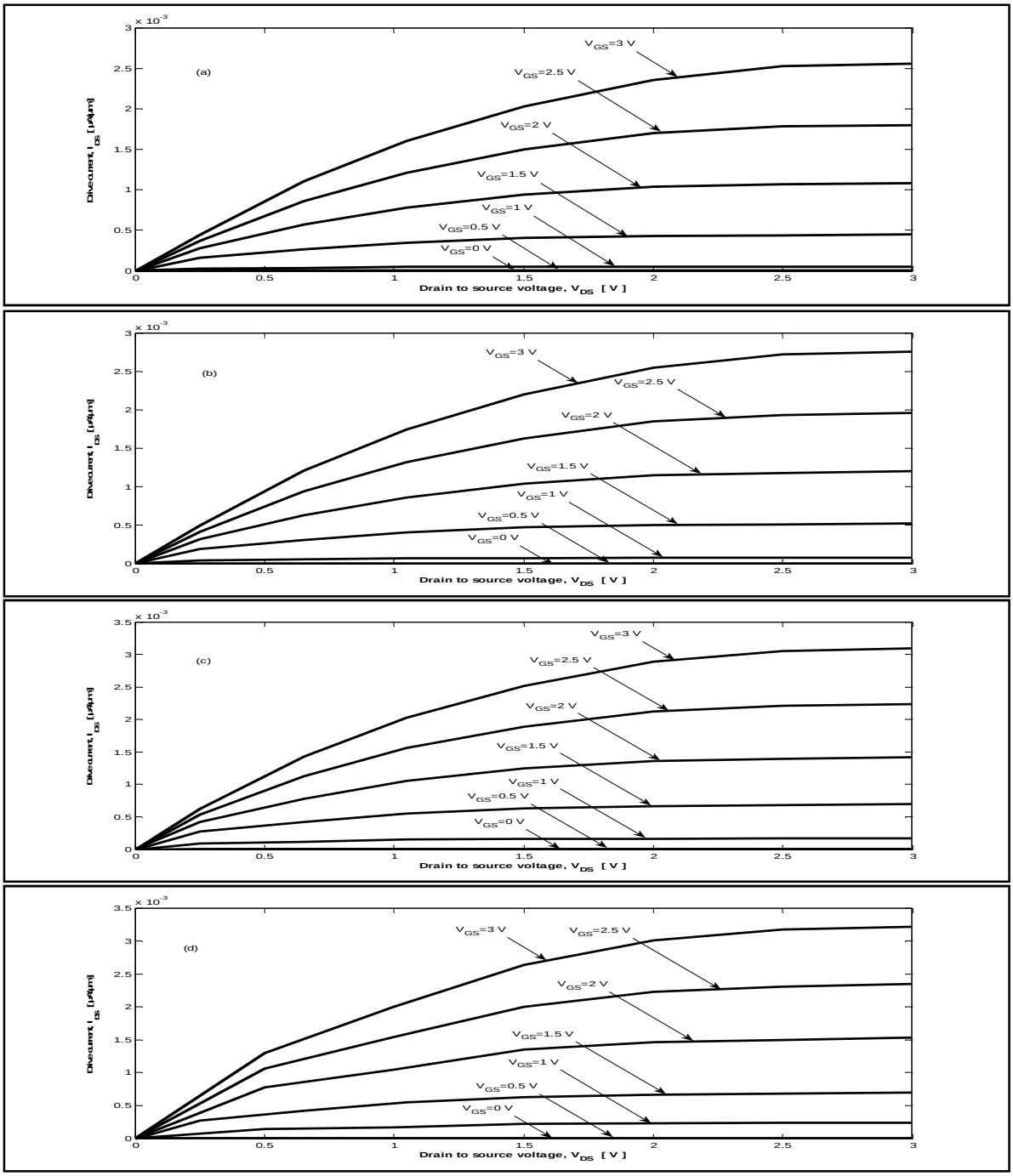

Fig.B_1: Output characteristics of 100nm vertical MOSFETs for body doping of 1×10^{18} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) $1 \times 10^{20}/cm^3$.

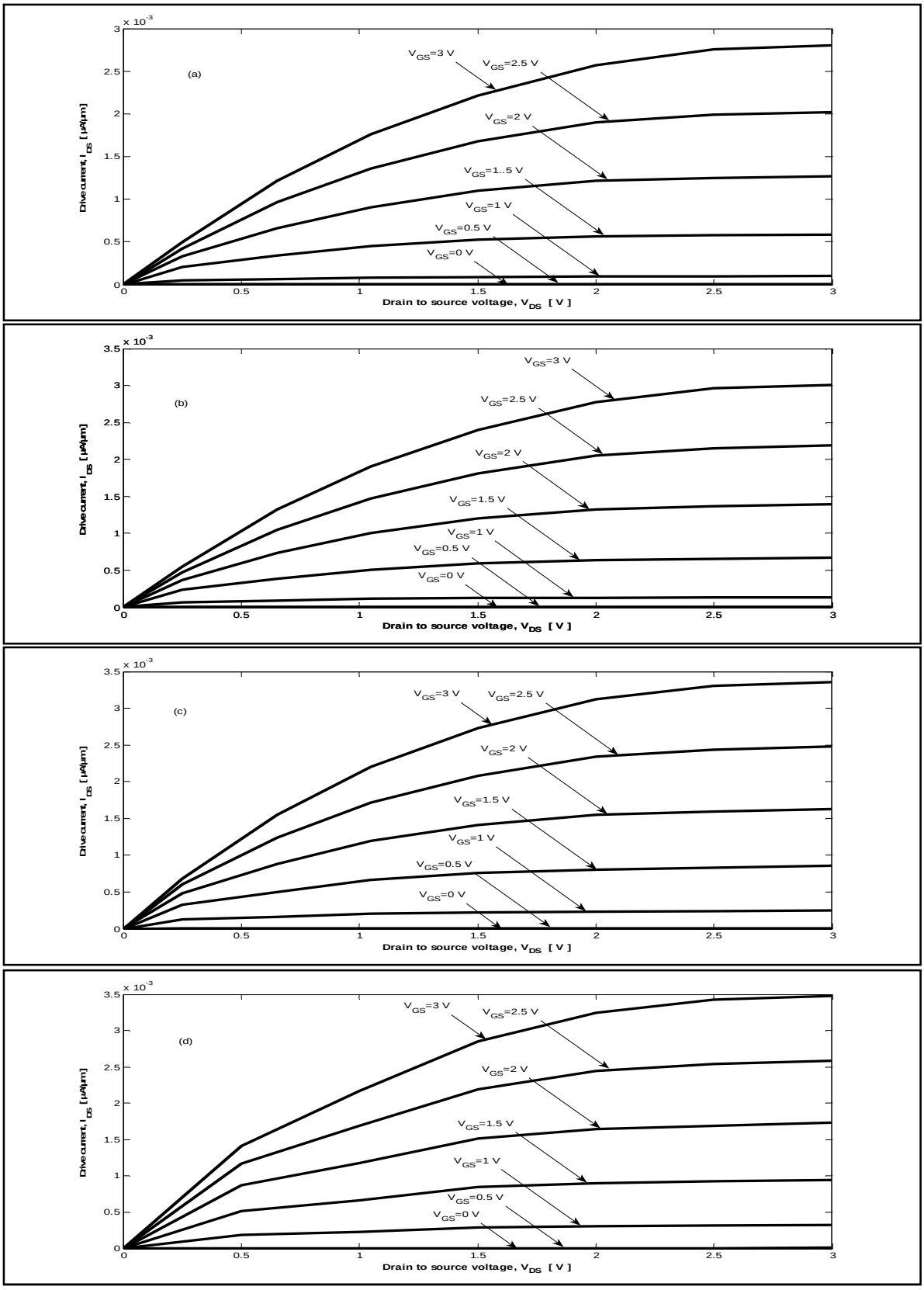

Fig.B$_2$: Output characteristics of 100nm vertical MOSFETs for body doping of 8×10^{17} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) 1×10^{20}/cm^3.

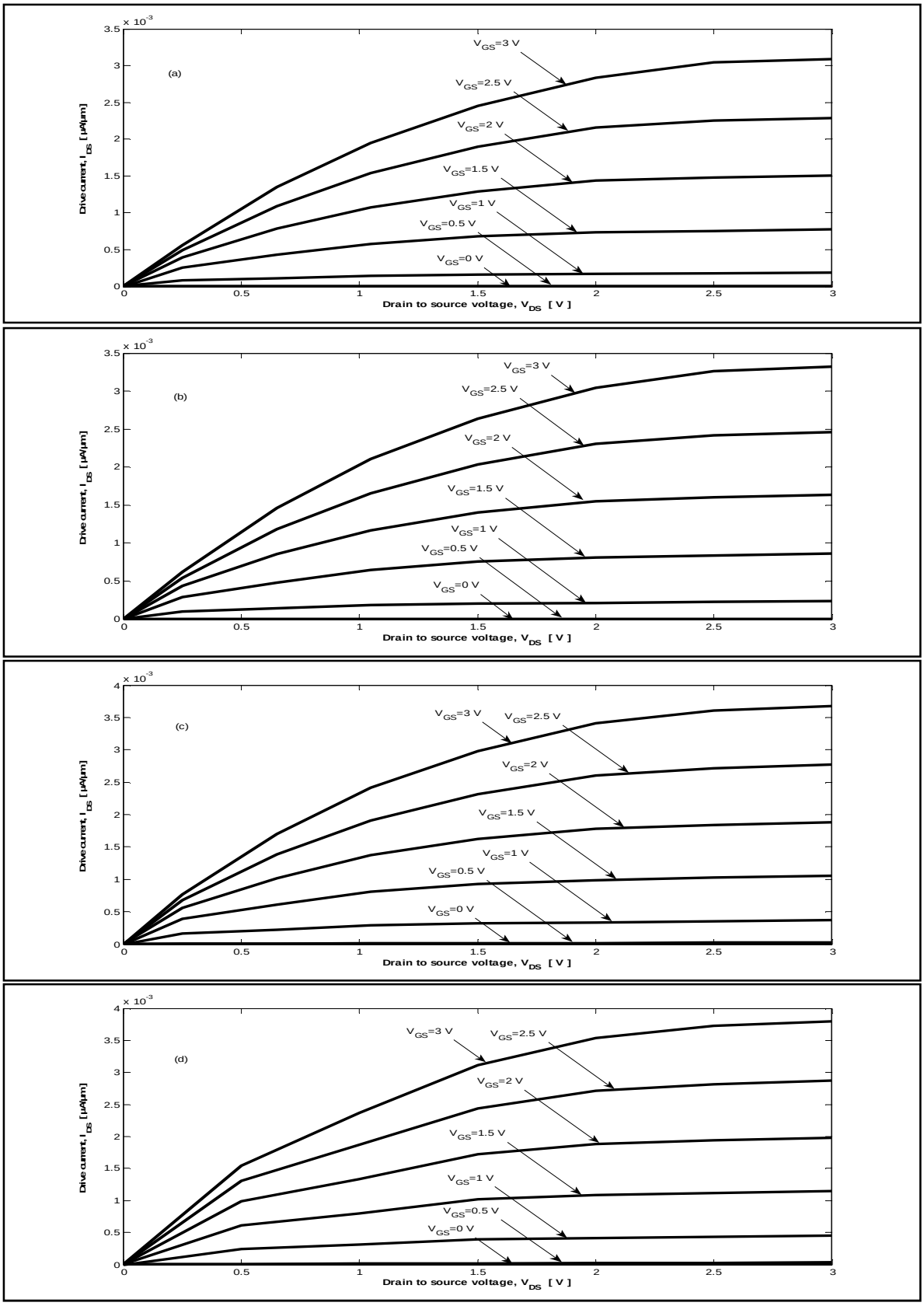

Fig.B$_3$: Output characteristics of 100nm vertical MOSFETs for body doping of 6×10^{17} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) $1 \times 10^{20}/cm^3$.

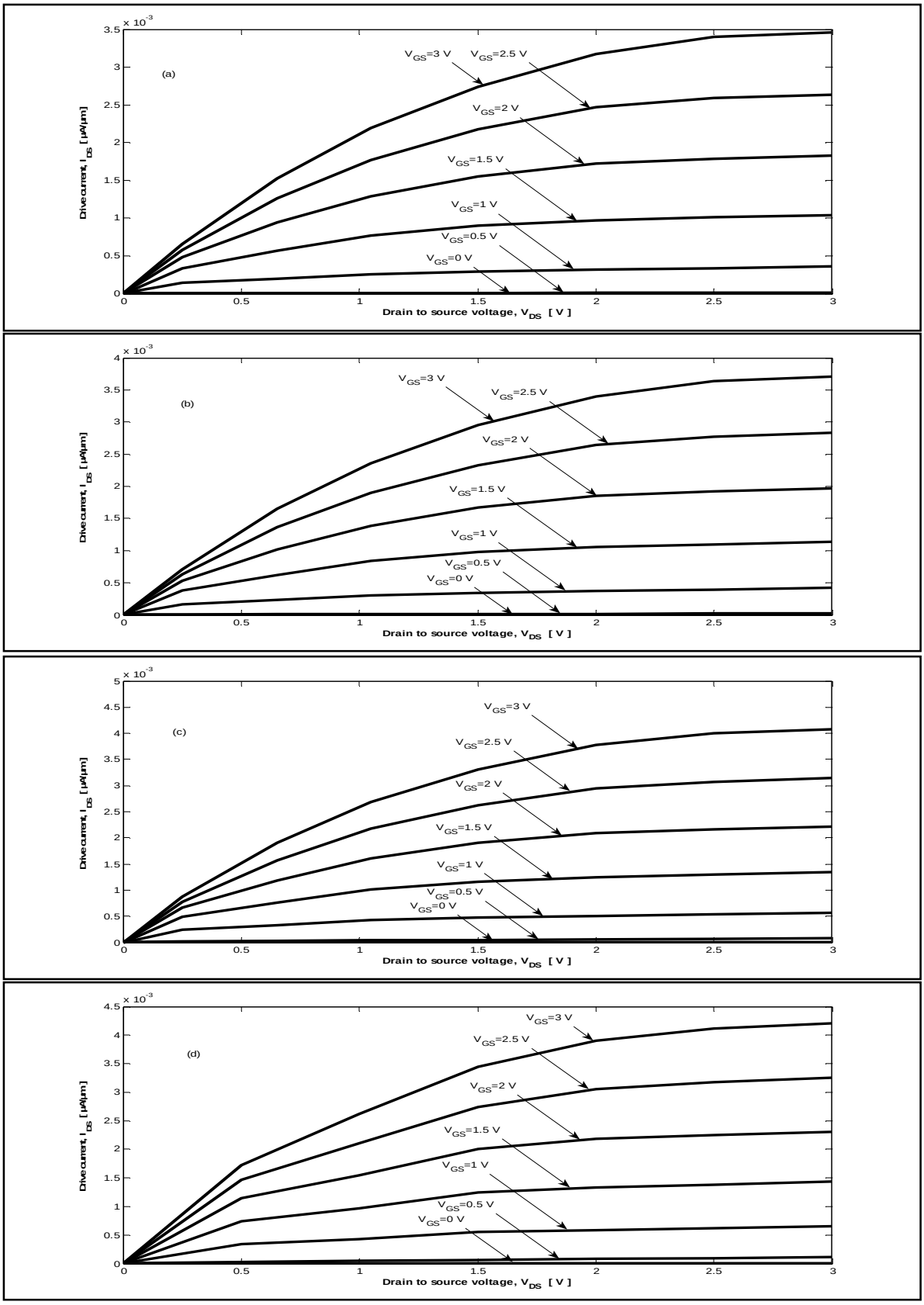

Fig.B$_4$: Output characteristics of 100nm vertical MOSFETs for body doping of 4×10^{17} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) $1 \times 10^{20}/cm^3$.

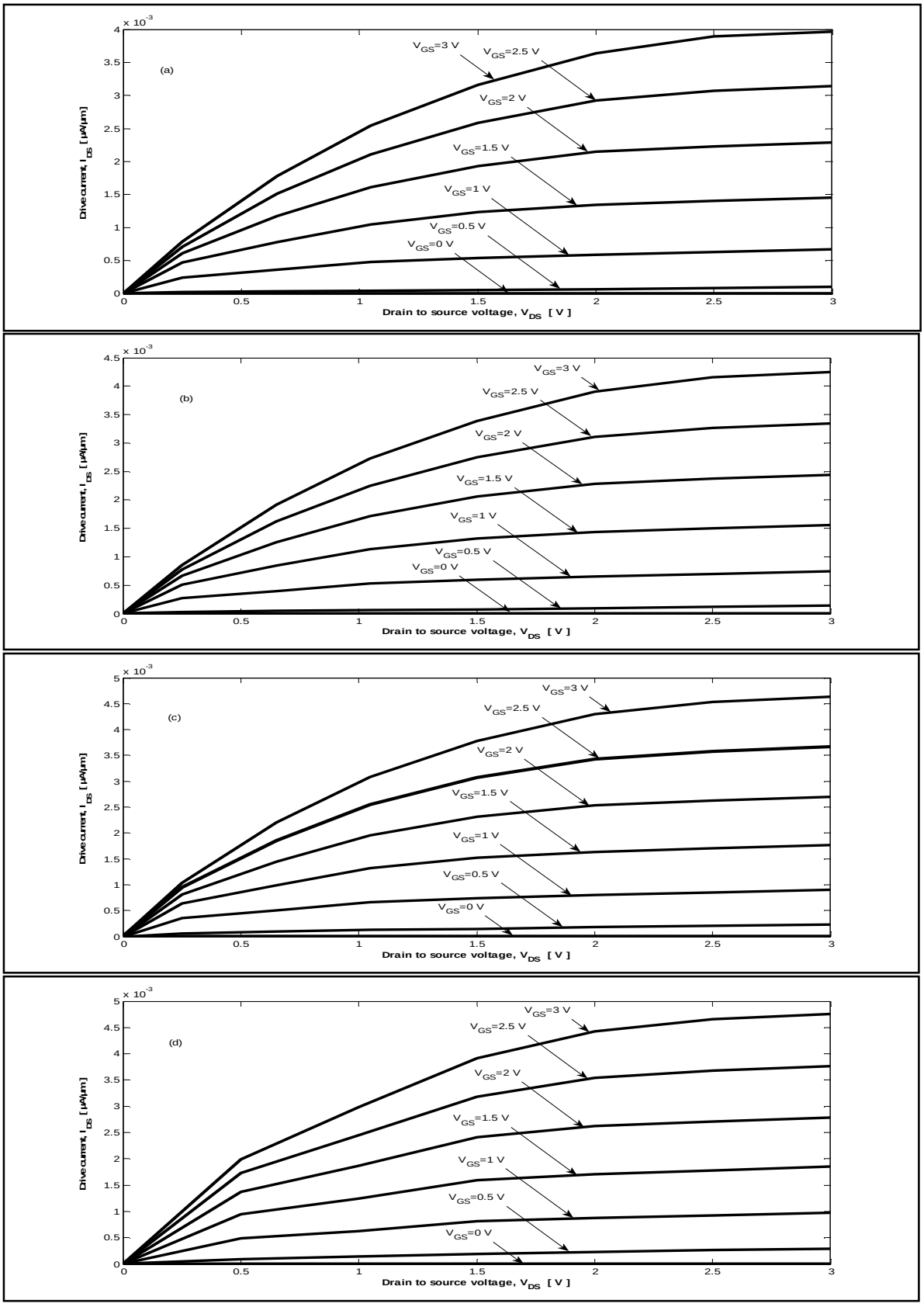

Fig.B$_5$: Output characteristics of 100nm vertical MOSFETs for body doping of 2×10^{17} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) $1 \times 10^{20}/cm^3$.

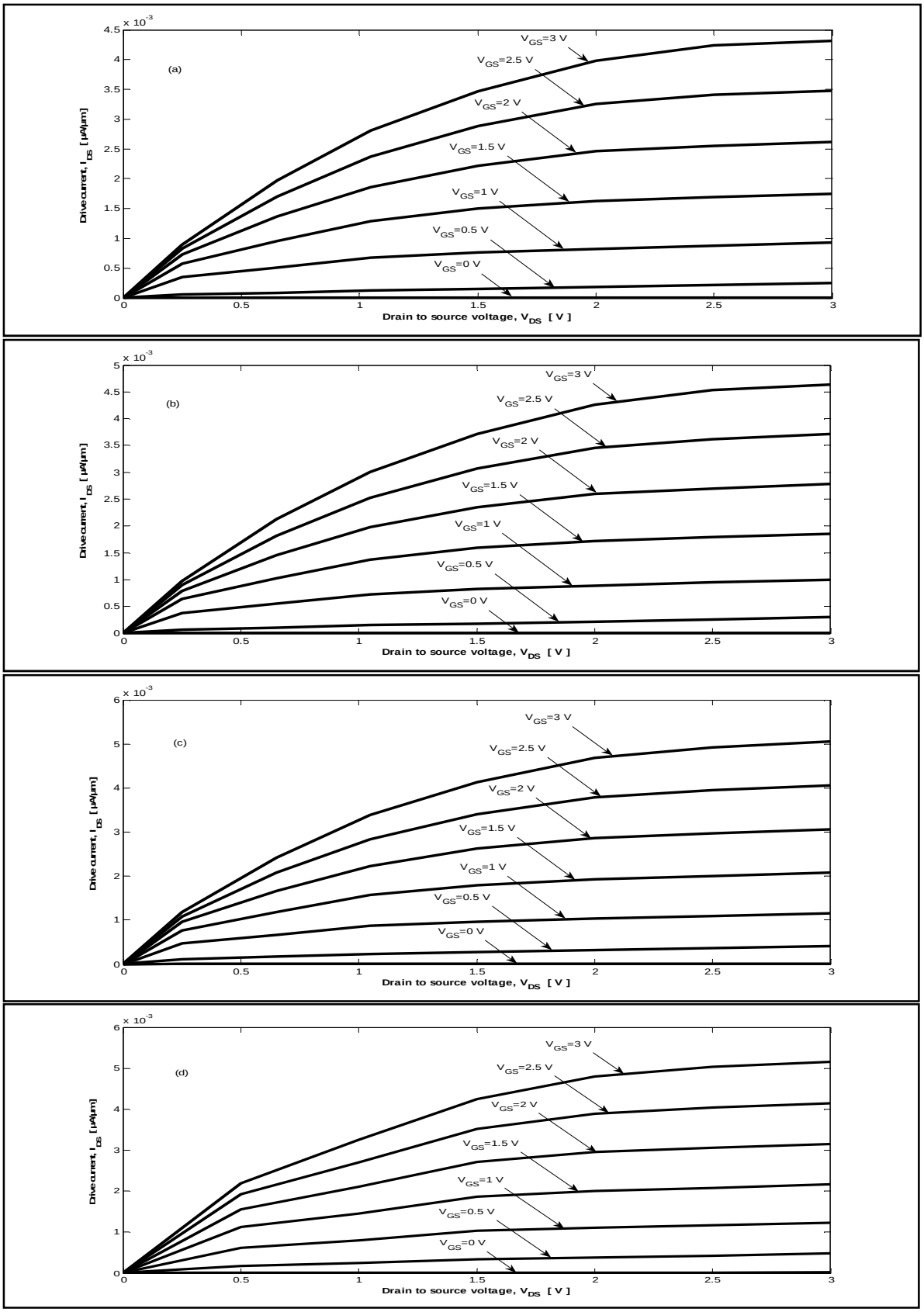

Fig.B$_6$: Output characteristics of 100nm vertical MOSFETs for body doping of 1×10^{17} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) $1 \times 10^{20}/cm^3$.

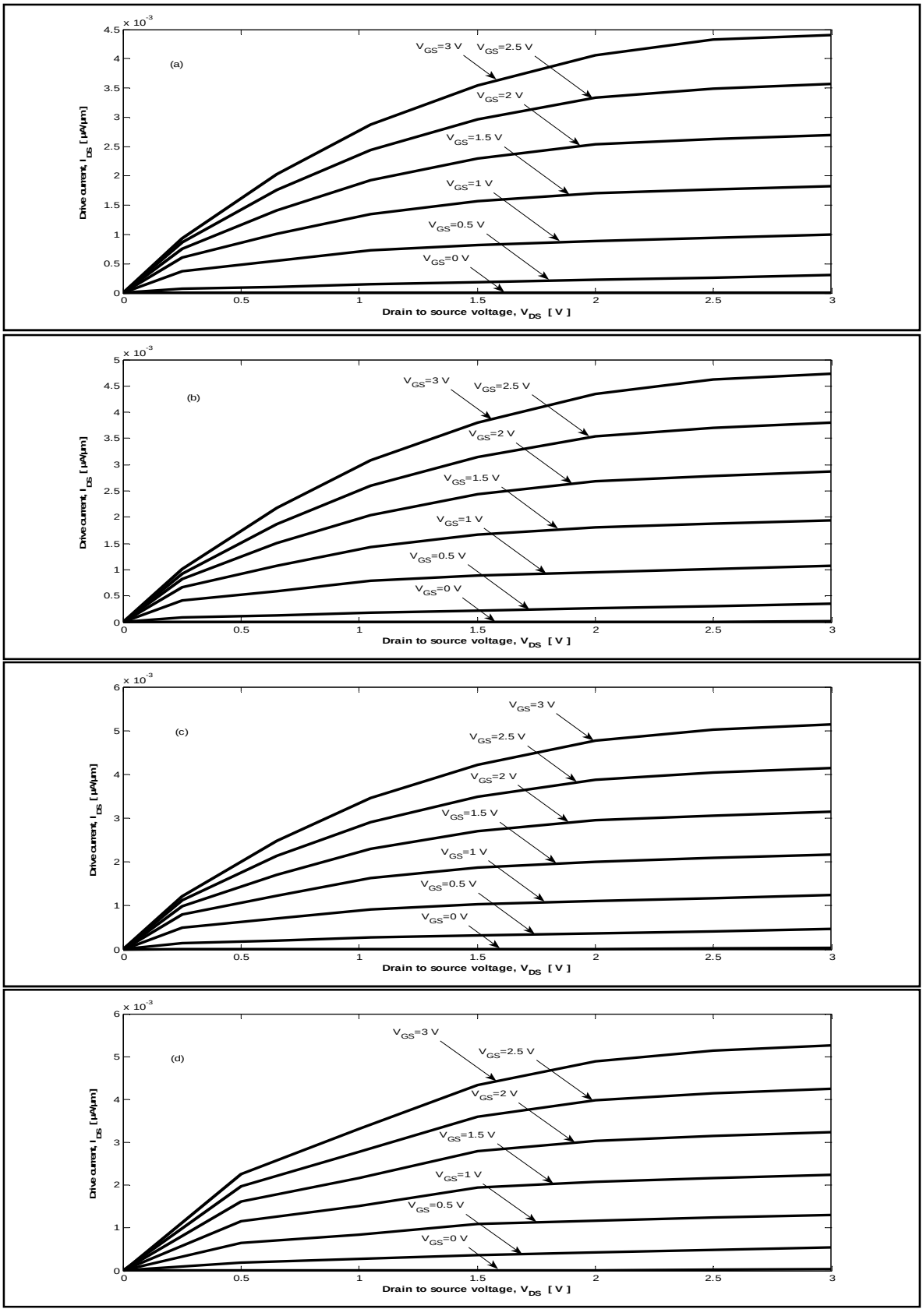

Fig.B$_7$: Output characteristics of 100nm vertical MOSFETs for body doping of 8×10^{16} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) $1 \times 10^{20}/cm^3$.

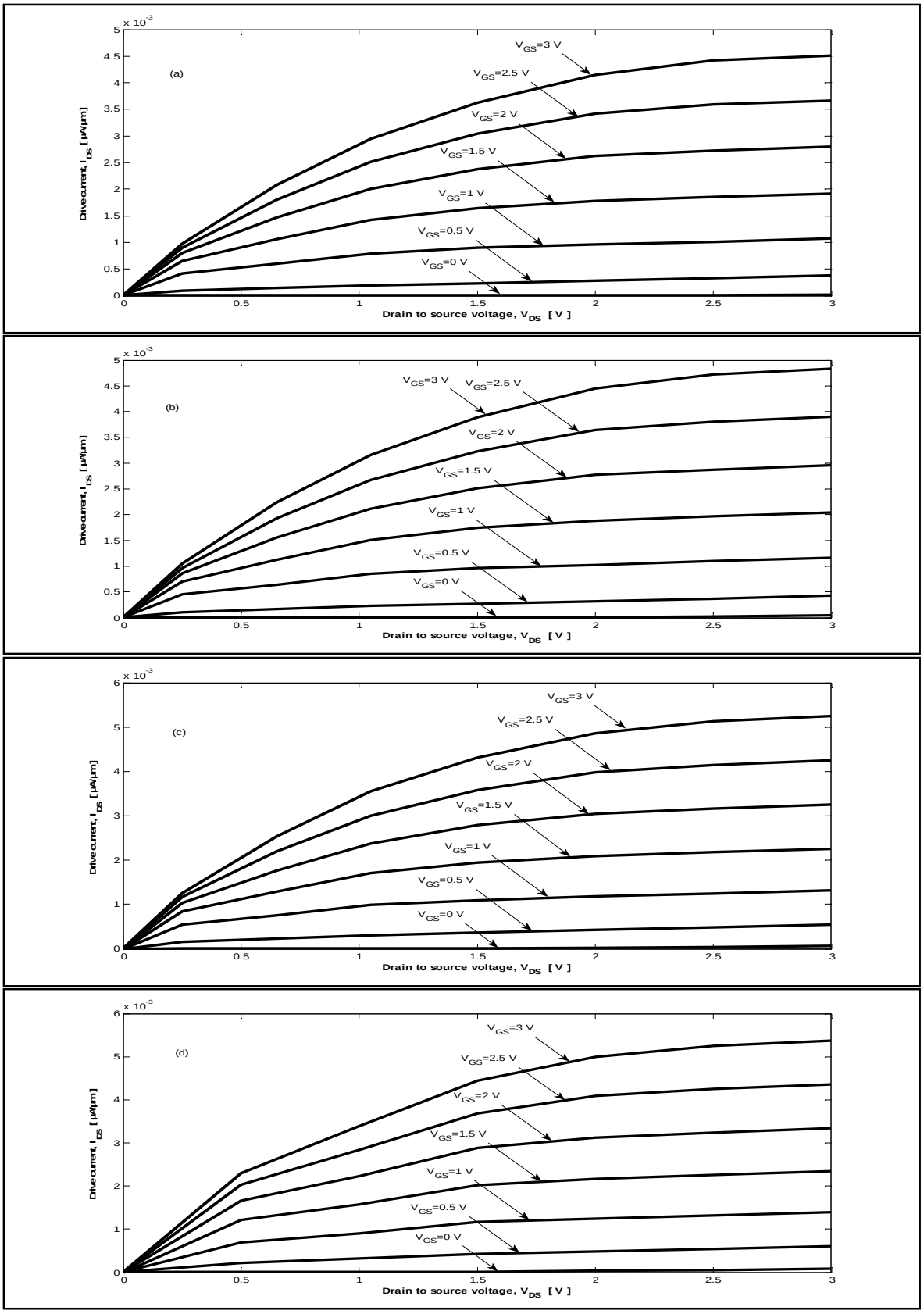

Fig.B$_8$: Output characteristics of 100nm vertical MOSFETs for body doping of 6×10^{16} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) $1 \times 10^{20}/cm^3$.

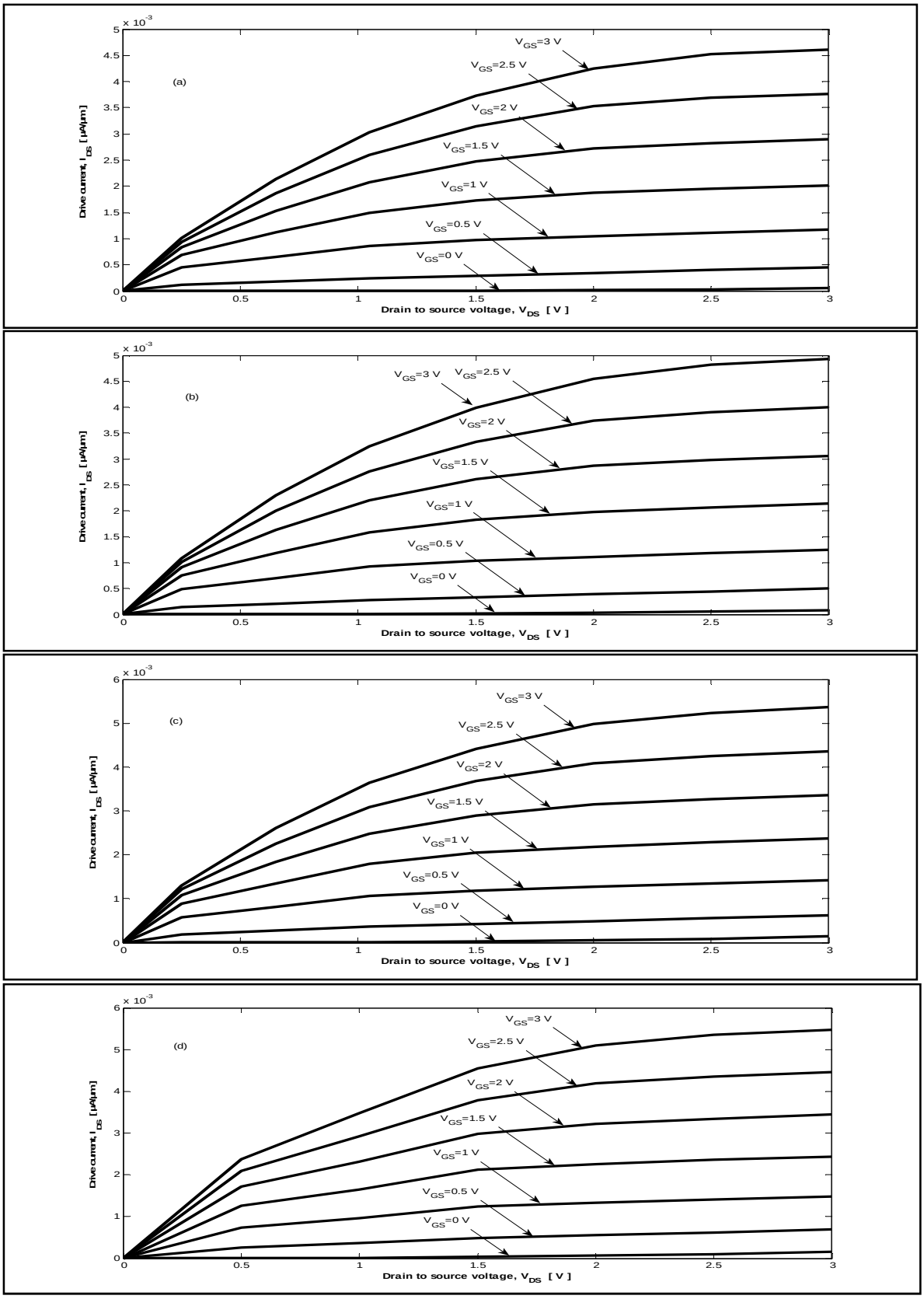

Fig.B$_9$: Output characteristics of 100nm vertical MOSFETs for body doping of 4×10^{16} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) $1 \times 10^{20}/cm^3$.

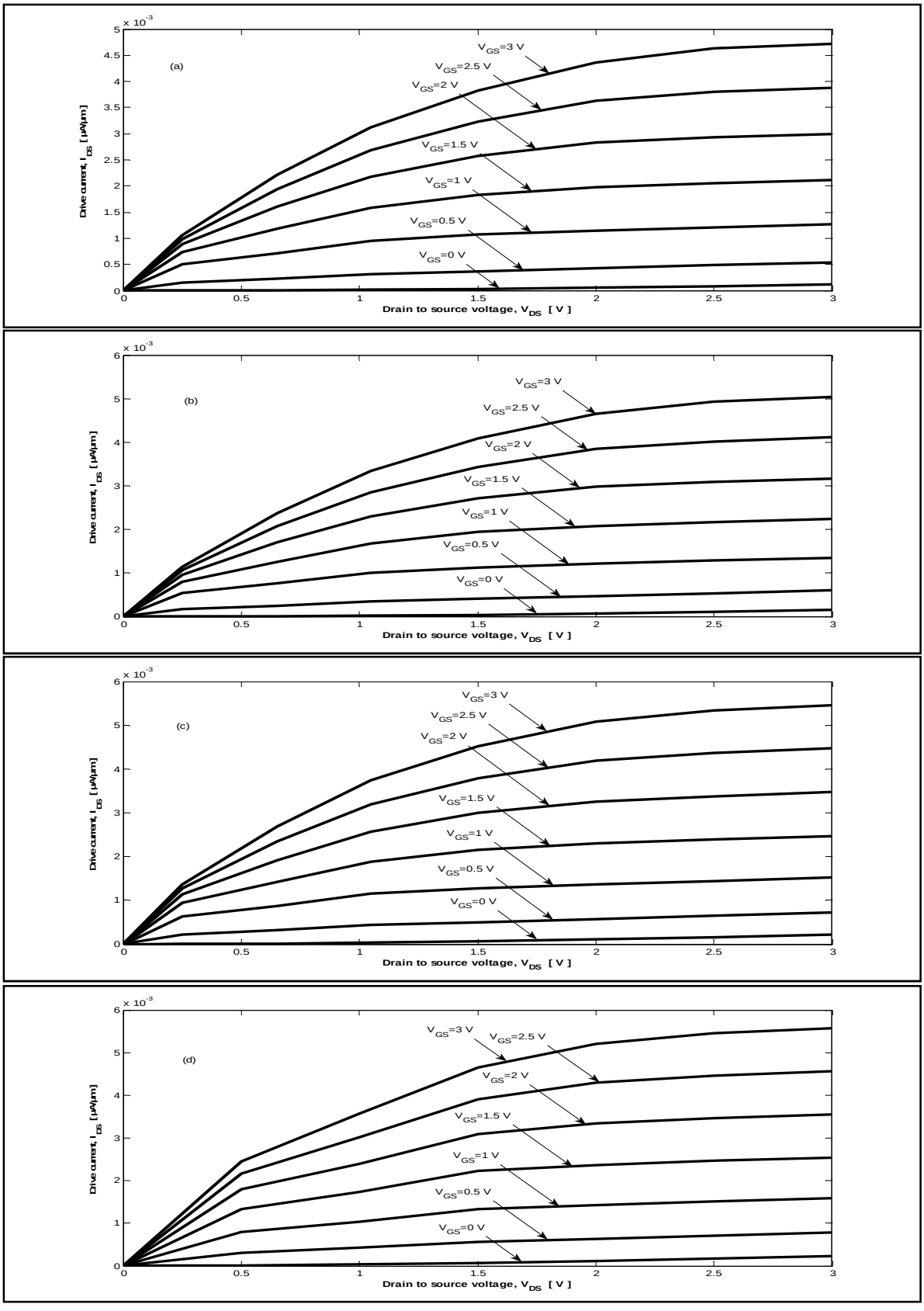

Fig.B$_{10}$: Output characteristics of 100nm vertical MOSFETs for body doping of 2×10^{16} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) $1 \times 10^{20}/cm^3$.

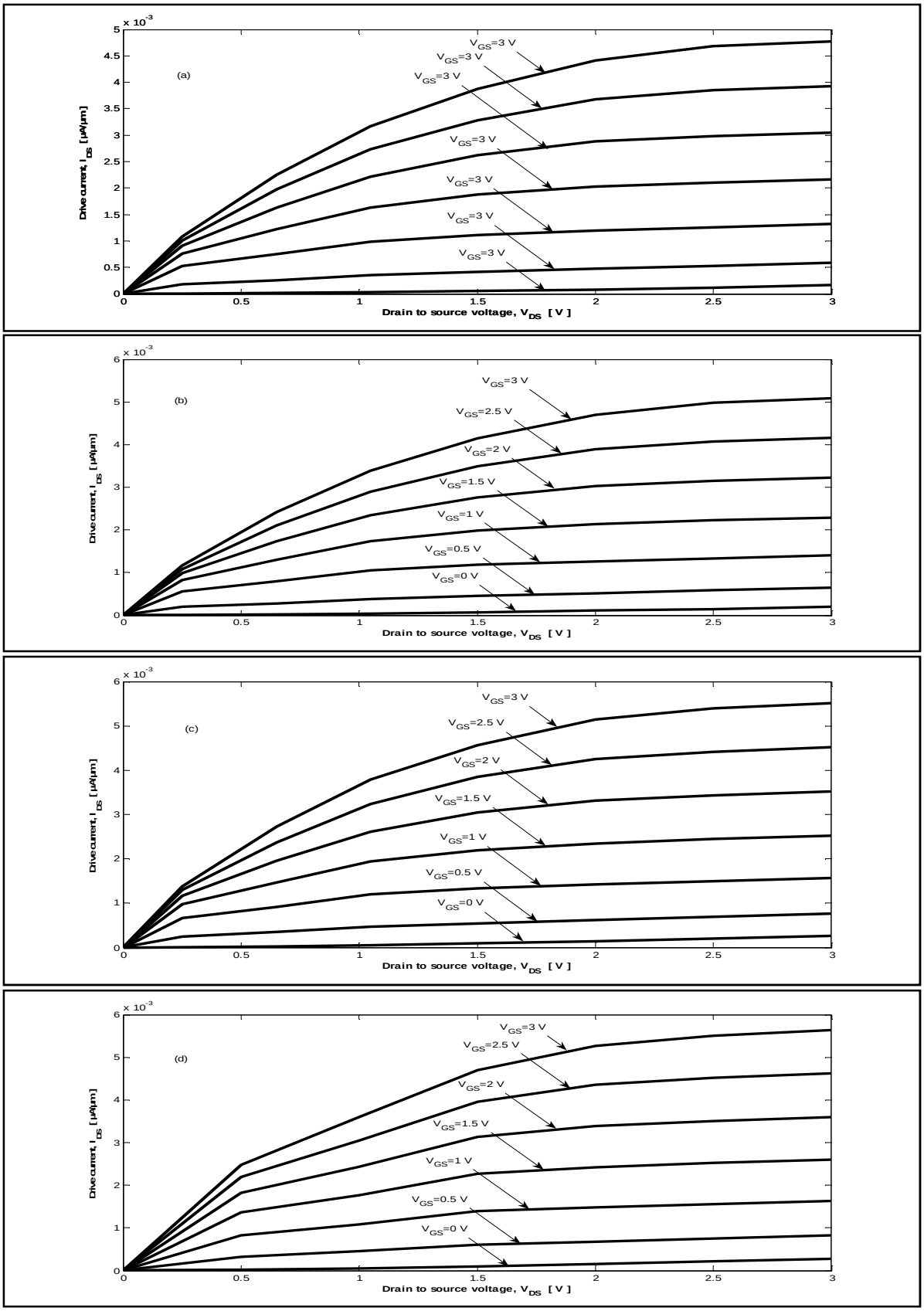

Fig.B$_{11}$: Output characteristics of 100nm vertical MOSFETs for body doping of 1×10^{16} / cm^3 at different LDD doping (a) 5×10^{18} / cm^3, (b) 1×10^{19} / cm^3, (c) 5×10^{19} / cm^3 and (d) $1 \times 10^{20}/cm^3$.

APPENDIX-C

C. Comparison table

C.1: Comparison table at different body doping and LDD doping values.

Table I: Device parameters for body doping 1×10^{18} / cm^3 at different LDD.

BODY Doping $[cm^{-3}]$	**LDD Doping** $[cm^{-3}]$	$\mathbf{V_G}$ [V]	$\mathbf{V_T}$ [V] ($\mathbf{V_{DS}}$=1V) ($\mathbf{I_{DS}}$=0.13mA)	**S** [mV/dec] When ($\mathbf{V_{DS}}$=0.1V&1V)	**DIBL** [mV/V] ($\mathbf{I_D}$=10^{-8}A) ($\mathbf{V_{DS}}$=0.1V&1V)	$\mathbf{I_D}$ [A] From $\mathbf{I_D V_D}$ Curve ($\mathbf{V_{DS}}$=3V&$\mathbf{V_{GS}}$=3V)
1×10^{18}	1×10^{20}	-3 to 3	0.8545	86.77	15.78	0.00322
1×10^{18}	5×10^{19}	-3 to 3	0.95	85.51	15	0.0031
1×10^{18}	1×10^{19}	-3 to 3	1.093	83.35	9.78	0.00276
1×10^{18}	5×10^{18}	-3 to 3	1.153	82.28	6.11	0.00256

Table II: Device parameters for body doping 8×10^{17} / cm^3 at different LDD.

BODY Doping $[cm^{-3}]$	**LDD Doping** $[cm^{-3}]$	$\mathbf{V_G}$ [V]	$\mathbf{V_T}$ [V] ($\mathbf{V_{DS}}$=1V) ($\mathbf{I_{DS}}$=0.13mA)	**S** [mV/dec] When ($\mathbf{V_{DS}}$=0.1V&1V)	**DIBL** [mV/V] ($\mathbf{I_D}$=10^{-8}A) ($\mathbf{V_{DS}}$=0.1V&1V)	$\mathbf{I_D}$ [A] From $\mathbf{I_D V_D}$ Curve ($\mathbf{V_{DS}}$=3V&$\mathbf{V_{GS}}$=3V)
8×10^{17}	1×10^{20}	-3 to 3	0.7838	84.69	19.11	0.00348
8×10^{17}	5×10^{19}	-3 to 3	0.858	84.34	18	0.00336
8×10^{17}	1×10^{19}	-3 to 3	1.017	83.979	13.67	0.00301
8×10^{17}	5×10^{18}	-3 to 3	1.063	83.83	9.67	0.0028

Table III: Device parameters for body doping 6×10^{17} / cm^3 at different LDD.

BODY Doping $[cm^{-3}]$	**LDD Doping** $[cm^{-3}]$	$\mathbf{V_G}$ [V]	$\mathbf{V_T}$ [V] ($\mathbf{V_{DS}}$=1V) ($\mathbf{I_{DS}}$=0.13mA)	**S** [mV/dec] When ($\mathbf{V_{DS}}$=0.1V&1V)	**DIBL** [mV/V] ($\mathbf{I_D}$=10^{-8}A) ($\mathbf{V_{DS}}$=0.1V&1V)	$\mathbf{I_D}$ [A] From $\mathbf{I_D V_D}$ Curve ($\mathbf{V_{DS}}$=3V&$\mathbf{V_{GS}}$=3V)
6×10^{17}	1×10^{20}	-3 to 3	0.6951	85.34	26.22	0.0038
6×10^{17}	5×10^{19}	-3 to 3	0.775	84.95	24	0.00368
6×10^{17}	1×10^{19}	-3 to 3	0.8951	84.89	19.78	0.00332
6×10^{17}	5×10^{18}	-3 to 3	0.9553	83.92	16.89	0.00309

Table IV: Device parameters for body doping 4×10^{17} / cm^3 at different LDD.

BODY Doping $[cm^{-3}]$	**LDD Doping** $[cm^{-3}]$	$\mathbf{V_G}$ [V]	$\mathbf{V_T}$ [V] ($\mathbf{V_{DS}}$=1V) ($\mathbf{I_{DS}}$=0.13mA)	**S** [mV/dec] When ($\mathbf{V_{DS}}$=0.1V&1V)	**DIBL** [mV/V] ($\mathbf{I_D}$=10^{-8}A) ($\mathbf{V_{DS}}$=0.1V&1V)	$\mathbf{I_D}$ [A] From $\mathbf{I_D V_D}$ Curve ($\mathbf{V_{DS}}$=3V&$\mathbf{V_{GS}}$=3V)
4×10^{17}	1×10^{20}	-3 to 3	0.5977	84.14	38.22	0.0042
4×10^{17}	5×10^{19}	-3 to 3	0.6513	82.26	38.11	0.00408
4×10^{17}	1×10^{19}	-3 to 3	0.7815	81.54	36	0.00371
4×10^{17}	5×10^{18}	-3 to 3	0.8194	80.72	32.67	0.00346

Table V: Device parameters for body doping 2×10^{17} / cm^3 at different LDD.

BODY Doping $[cm^{-3}]$	**LDD Doping** $[cm^{-3}]$	$\mathbf{V_G}$ [V]	$\mathbf{V_T}$ [V] ($\mathbf{V_{DS}}$=1V) ($\mathbf{I_{DS}}$=0.13mA)	**S** [mV/dec] When ($\mathbf{V_{DS}}$=0.1V&1V)	**DIBL** [mV/V] ($\mathbf{I_D}$=10^{-8}A) ($\mathbf{V_{DS}}$=0.1V&1V)	$\mathbf{I_D}$ [A] From $\mathbf{I_D V_D}$ Curve ($\mathbf{V_{DS}}$=3V&$\mathbf{V_{GS}}$=3V)
2×10^{17}	1×10^{20}	-3 to 3	0.4555	85.41	59.78	0.00476
2×10^{17}	5×10^{19}	-3 to 3	0.5085	84.895	57.78	0.00464
2×10^{17}	1×10^{19}	-3 to 3	0.5916	76.16	50.44	0.00425
2×10^{17}	5×10^{18}	-3 to 3	0.6289	75.07	45.33	0.00397

Table VI: Device parameters for body doping 1×10^{17} / cm^3 at different LDD.

BODY Doping $[cm^{-3}]$	**LDD Doping** $[cm^{-3}]$	$\mathbf{V_G}$ [V]	$\mathbf{V_T}$ [V] ($\mathbf{V_{DS}}$=1V) ($\mathbf{I_{DS}}$=0.13mA)	**S** [mV/dec] When ($\mathbf{V_{DS}}$=0.1V&1V)	**DIBL** [mV/V] ($\mathbf{I_D}$=10^{-8}A) ($\mathbf{V_{DS}}$=0.1V&1V)	$\mathbf{I_D}$ [A] From $\mathbf{I_D V_D}$ Curve ($\mathbf{V_{DS}}$=3V&$\mathbf{V_{GS}}$=3V)
1×10^{17}	1×10^{20}	-3 to 3	0.3573	120.52	118.24	0.00516
1×10^{17}	5×10^{19}	-3 to 3	0.3843	118.11	111.27	0.00505
1×10^{17}	1×10^{19}	-3 to 3	0.4678	100.32	92.63	0.00463
1×10^{17}	5×10^{18}	-3 to 3	0.5095	95.53	68.92	0.00432

Table VII: Device parameters for body doping 8×10^{16} / cm^3 at different LDD.

BODY Doping $[cm^{-3}]$	**LDD Doping** $[cm^{-3}]$	$\mathbf{V_G}$ [V]	$\mathbf{V_T}$ [V] ($\mathbf{V_{DS}}$=1V) ($\mathbf{I_{DS}}$=0.13mA)	**S** [mV/dec] When ($\mathbf{V_{DS}}$=0.1V&1V)	**DIBL** [mV] ($\mathbf{I_D}$=10^{-8}A) ($\mathbf{V_{DS}}$=0.1V&1V)	$\mathbf{I_D}$ [A] From $\mathbf{I_D V_D}$ Curve ($\mathbf{V_{DS}}$=3V&$\mathbf{V_{GS}}$=3V)
8×10^{16}	1×10^{20}	-3 to 3	0.3357	132.28	135.36	5.26E-03
8×10^{16}	5×10^{19}	-3 to 3	0.3598	131.10	124.54	5.15E-03
8×10^{16}	1×10^{19}	-3 to 3	0.423	119.47	100.54	4.73E-03
8×10^{16}	5×10^{18}	-3 to 3	0.4566	105.44	88.32	4.41E-03

Table VIII: Device parameters for body doping 6×10^{16} / cm^3 at different LDD.

BODY Doping $[cm^{-3}]$	**LDD Doping** $[cm^{-3}]$	$\mathbf{V_G}$ [V]	$\mathbf{V_T}$ [V] ($\mathbf{V_{DS}}$=1V) ($\mathbf{I_{DS}}$=0.13mA)	**S** [mV/dec] When ($\mathbf{V_{DS}}$=0.1V&1V)	**DIBL** [mV] ($\mathbf{I_D}$=10^{-8}A) ($\mathbf{V_{DS}}$=0.1V&1V)	$\mathbf{I_D}$ [A] From $\mathbf{I_D V_D}$ Curve ($\mathbf{V_{DS}}$=3V&$\mathbf{V_{GS}}$=3V)
6×10^{16}	1×10^{20}	-3 to 3	0.3115	158.05	201.61	5.37E-03
6×10^{16}	5×10^{19}	-3 to 3	0.3284	150.88	185.24	5.25E-03
6×10^{16}	1×10^{19}	-3 to 3	0.3788	141.49	142.68	4.83E-03
6×10^{16}	5×10^{18}	-3 to 3	0.408	129.95	119.67	4.51E-03

Table IX: Device parameters for body doping 4×10^{16} / cm^3 at different LDD.

BODY Doping [cm^{-3}]	**LDD Doping** [cm^{-3}]	$\mathbf{V_G}$ [V]	$\mathbf{V_T}$ [V] ($\mathbf{V_{DS}}$=1V) ($\mathbf{I_{DS}}$=0.13mA)	**S** [mV/dec] When ($\mathbf{V_{DS}}$=0.1V&1V)	**DIBL** [mV] ($\mathbf{I_D}$=10^{-8}A) ($\mathbf{V_{DS}}$=0.1V&1V)	$\mathbf{I_D}$ [A] From $\mathbf{I_D V_D}$ Curve ($\mathbf{V_{DS}}$=3V&$\mathbf{V_{GS}}$=3V)
4×10^{16}	1×10^{20}	-3 to 3	0.2786	193.08	318.04	5.47E-03
4×10^{16}	5×10^{19}	-3 to 3	0.2913	184.80	290.8	5.36E-03
4×10^{16}	1×10^{19}	-3 to 3	0.3305	162.77	226.72	4.93E-03
4×10^{16}	5×10^{18}	-3 to 3	0.3524	155.76	192.32	4.61E-03

Table X: Device parameters for body doping 2×10^{16} / cm^3 at different LDD.

BODY Doping [cm^{-3}]	**LDD Doping** [cm^{-3}]	$\mathbf{V_G}$ [V]	$\mathbf{V_T}$ [V] ($\mathbf{V_{DS}}$=1V) ($\mathbf{I_{DS}}$=0.13mA)	**S** [mV/dec] When ($\mathbf{V_{DS}}$=0.1V&1V)	**DIBL** [mV] ($\mathbf{I_D}$=10^{-8}A) ($\mathbf{V_{DS}}$=0.1V&1V)	$\mathbf{I_D}$ [A] From $\mathbf{I_D V_D}$ Curve ($\mathbf{V_{DS}}$=3V&$\mathbf{V_{GS}}$=3V)
2×10^{16}	1×10^{20}	-3 to 3	0.2047	271.49	503	5.58E-03
2×10^{16}	5×10^{19}	-3 to 3	0.2217	245.07	469.14	5.46E-03
2×10^{16}	1×10^{19}	-3 to 3	0.2648	209.89	378.49	5.04E-03
2×10^{16}	5×10^{18}	-3 to 3	0.2872	192.07	327.214	4.72E-03

Table XI: Device parameters for body doping 1×10^{16} / cm^3 at different LDD.

BODY Doping [cm^{-3}]	**LDD Doping** [cm^{-3}]	$\mathbf{V_G}$ [V]	$\mathbf{V_T}$ [V] ($\mathbf{V_{DS}}$=1V) ($\mathbf{I_{DS}}$=0.13mA)	**S** [mV/dec] When ($\mathbf{V_{DS}}$=0.1V&1V)	**DIBL** [mV] ($\mathbf{I_D}$=10^{-8}A) ($\mathbf{V_{DS}}$=0.1V&1V)	$\mathbf{I_D}$ [A] From $\mathbf{I_D V_D}$ Curve ($\mathbf{V_{DS}}$=3V&$\mathbf{V_{GS}}$=3V)
1×10^{16}	1×10^{20}	-3 to 3	0.1459	305.29	630	5.63E-03
1×10^{16}	5×10^{19}	-3 to 3	0.1598	294.18	574.9	5.52E-03
1×10^{16}	1×10^{19}	-3 to 3	0.2064	256.65	466.7	5.09E-03
1×10^{16}	5×10^{18}	-3 to 3	0.2401	232.22	406.79	4.77E-03

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