VIA EFFECTS ON SIGNAL PROPAGATION IN HIGH SPEED TRANSMISSION LINES

By

Saad Bin Abul Kashem

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Approved By

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Thesis Advisor

Md Ishfaqur Raza, PhD

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Chairperson

Anisul Haque, PhD

Abstract

The transmission lines on a printed circuit board are used to transmit data packets from a microprocessor or an application specific integrated circuit (ASIC) to other chips or devices. The quality of the signal being propagated on the transmission line, either a micro strip or a strip line, is a function of its end to end impedance profile. The impedance of the transmission line is not only defined by its own physical characteristics such as material property, dielectric thickness, or trace dimensions but also on the characteristics of the environment where the transmission line is placed. Any impedance changes on the line will affect signal quality due to reflections and crosstalk. The objective of this work is to calculate via effects on transmission line impedance at the high end of the microwave spectrum, i.e. several GHz. Three types of via placement near a differential micro strip trace are studied.

The effect on signal for different placement of via with the differential line was characterized by the opening of eye diagram. The eye diagrams were plotted on Matlab using the data generated with Spice simulation of different system and via configurations. The analysis was done at two different frequencies, 1 GHz and 3 GHz. In this analysis different length configurations were observed. Analysis is done separately on two trace length 13 inch and 24 inch. Later, jitter, setup time, hold time, high margin and low margin of the Eye diagram was calculated. An optimum placement of the via next to a transmission line is then proposed.

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1. Introduction

With newer process and demand for increased system performance, clock speeds are getting faster and data transfer rates are increasing the acceleration of the system speed effects signal integrity. The reliable operation of system also becomes increasingly difficult. To understand this problem extensive work on the matter is needed.

The transmission lines are used in propagation systems to connect different devices. Data transmitted on from one device is carried by the transmission to another device [1]. This device can be a microprocessor or an application specific integrated circuit (ASIC). The data carrying capacity of the transmission lines is defined b its impedance. Transmission line's impedance not only depends on there own characteristics or parameters (material, thickness, dimension etc) but also on the characteristics of the features that exist in the environment surrounding them. The distribution of this impedance determines signal quality, which is best characterized by parameters such as noise, jitter, transmission delay or timing. It also embodies reflections, crosstalk and mismatches between drivers and receivers.

The effect of parasitic features in a transmission system like mutual capacitance and inductance is becoming more significant because of systems running at higher speeds. As the capacitance and inductance depends on system frequency, the capacitive and inductive effect of these parasitic are seriously degrading signal integrity and thus affecting device and system performance.

Accurate modeling of system elements (trace, via) are very important for signal transmission, particularly at the microwave frequencies and above. The signal quality, time delay and overall signal performance is partially dependent on this. The system element's resistance, capacitance, inductance overall impedance must be measured accurately for better performance in high frequency transmission. For this, the system element should be modeled more accurately keeping focus on the frequency of operation.

System or electrical performance of signal propagating in printed circuit boards (PCBs) is determined by the transmission line parameters. More important of these parameters are characteristic impedance, differential impedance, and terminating impedance of both single-ended and differential pairs of micro strip and strip lines.

For accurate extraction of trace model, field solvers are used to extract the RLGC models. The extraction of accurate models are fundamental for various aspects of physical verification such as timing, signal integrity, substrate coupling, and power grid analysis. As electromagnetic behavior is governed by Maxwell's equations, parasitic extraction requires solving these equations. That form may be a simple analytic parallel plate capacitance equation, or may involve a full numerical solution for a complicated 3D geometry with wave propagation [2]. In layout extraction, analytic formulas for simple or simplified geometry can be used where accuracy is less important than speed.

2. Theory and Background

When a signal is propagating in a transmission line, it is dictated by Telegraphers equation [3]. The Telegrapher's Equations describes the voltage and current on an electrical transmission line with respect to distance and time using a pair of linear differential equations. They are developed based on Maxwell's Equations [4].

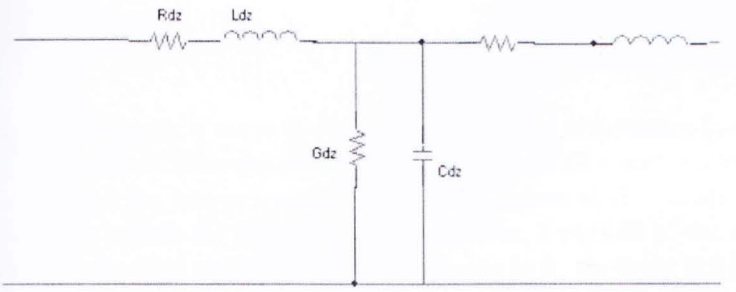

Figure 1: Discredited Transmission Line T-Equivalent Circuit

The transmission line model represents the transmission line as an infinite series of two-port elementary components, each representing an infinitesimally short segment of the transmission line:

The distributed resistance R of the conductors is represented by a series resistor (expressed in ohms per unit length).

The distributed inductance L is represented by a series inductor (henries per unit length).

The capacitance C between the two conductors is represented by a shunt capacitor C (farads per unit length).

The conductance G of the dielectric material separating the two conductors is represented by a conductance G shunted between the signal wire and the return wire (Siemens per unit length).

The model consists of an infinite series of the elements shown in the figure, and that the values of the components are specified per unit length so the picture of the component can be misleading. R, L, C, and G may also be functions of frequency [5].

The line voltage V is dictated by the following 2nd order differential equation -

$$\frac{\partial^2 V}{\partial z^2} = RGV + (RC + LG)\frac{\partial V}{\partial t} + LC\frac{\partial^2 V}{\partial t^2}$$

When the elements R and G are negligibly small the transmission line is considered as a lossless structure. In this hypothetical case, the model depends only on the L and C elements which greatly simplify the analysis. For a lossless transmission line, the second order steady-state Telegrapher's equation is

$$\frac{\partial^2 V}{\partial z^2} = LC \frac{\partial^2 V}{\partial t^2}$$

In this system, the mutual capacitance between traces of a differential pair and via is considered. The via is modeled as a lumped element. In spice modeling of a transmission line, the via is divided and added to the beginning and ending node of the transmission line segment [6]. Normally characteristic impedance of transmission line is

$$Z_0 \approx \sqrt{\frac{Z}{Y}} = \sqrt{\frac{R + jwL}{G + jwC}} \Omega$$

But when a driver emits a wave towards a receiver, the impedance (a measure of the dynamic ohms-law relationship between the current and voltage of a source) of the two must match in order to maximize the power transferred from the driver to the receiver. If the impedance of the receiver does not match the impedance of the driver, a portion of the driver's energy will be reflected by the receiver and therefore unavailable to it. As there is a mismatch in transmission line in our system, (there is a via beside the transmission line in our prescribed system) discontinuity occurs which creates reflection. Reflection equation is dictated by the following equation

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$$

where Z_L is the changed transmission line impedance due to via coupling on transmission line.

2.1. Eye Diagram

In electronics, the term eye diagram[7], an example of which is shown in Figure 1, also known as eye pattern is an oscilloscope display in which a digital data signal from a receiver is repetitively sampled and applied to the vertical input, while the data rate is used to trigger the horizontal sweep. It is so called because, for several types of coding, the pattern looks like a series of eyes between a pair of rails. It can be also plotted on Matlab by inserting data retrieved from simulation.

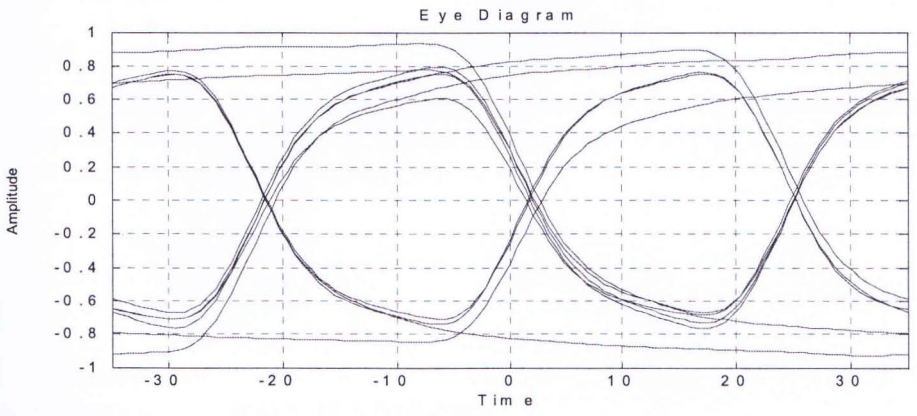

Figure 2: Eye Diagram

2.2. Crosstalk

In electronics, the term crosstalk refers to a disturbance, caused by electromagnetic interference, along a circuit or a transmission line pair [8]. A signal disrupts another signal in an adjacent circuit or transmission line and can cause the signals to become confused and cross over each other. Crosstalk creates an undesired effect in a circuit or channel for a signal transmitted on one circuit or channel of a transmission system [9]. Crosstalk is usually caused by undesired capacitive, inductive or conductive coupling from one circuit, part of a circuit, or channel, to another.

In integrated circuit design, crosstalk normally refers to a signal affecting another nearby signal [11]. Usually the coupling is capacitive, and to the nearest neighbor, but other forms of coupling and effects on signal further away are sometimes important, especially in analog designs. See signal integrity for tools used to measure and prevent this problem, and substrate coupling for a discussion of crosstalk conveyed through the integrated circuit substrate [10]. There are a wide variety of possible fixes, with increased spacing, wire re-ordering, and shielding being the most common .

2.3. Skin effect

The skin effect has practical consequences to some extent in electrical power transmission and distribution systems [12]. While signal is transmitting through micro strip or strip line or vias, skin effect redistributes current across the cross section of the wire.

Because of skin effect, an alternating electric current (AC) shows the tendency to redistribute itself within a conductor so that the current density near the surface of the conductor is greater than that at its core. That is, the electric current tends to flow at the "skin" of the conductor. The skin effect causes the effective resistance of the conductor to increase with the frequency of the current. Skin effect is due to eddy currents set up by the AC current. In the similar fashion, the skin effect causes the effective resistance of the conductor to increase with the frequency of the switching of the signal which is transmitting.

The current density J in an infinitely thick plane conductor decreases exponentially with depth d from the surface, as follows:

$$J = J_S e^{-d/\delta}$$

where δ is a constant called the skin depth. This is defined as the depth below the surface of the conductor at which the current density decays to 1/e (about 0.37) of the current density at the surface (JS). It can be calculated as follows:

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}}$$

where

ρ = resistivity of conductor

ω = angular frequency of current = 2π × frequency

$\mu = \mu_r \mu_o$, absolute magnetic permeability of conductor, where μ_o is the permeability of free space ($4\pi \times 10-7$ N/A2) and μ_r is the relative permeability of the conductor.

Figure 3 is referring that most current is in the surface of the trace because of the skin effect

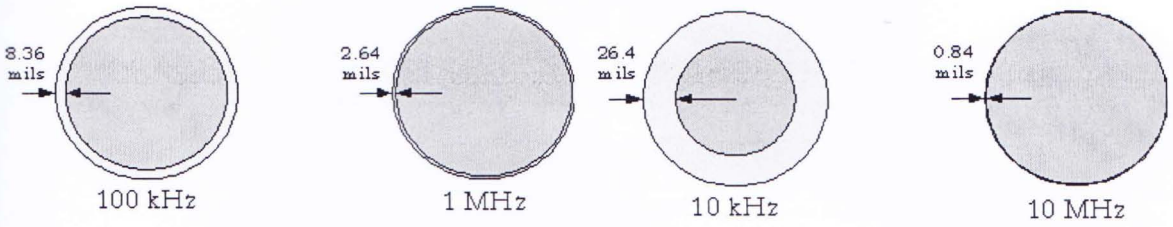

Figure 3: Skin Depth at different frequencies

2.4. Jitter

Jitter is an unwanted variation of one or more signal characteristics in electronics and telecommunications. Jitter may be seen in characteristics such as the interval between successive pulses, or the amplitude, frequency, or phase of successive cycles [7]. Jitter is a significant factor in the design of almost all communications links (e.g. USB, PCI-e, SATA, and OC-48).

Jitter can apply to a number of signal qualities (e.g. amplitude, phase, pulse width or pulse position), and can be quantified in the same terms as all time-varying signals (e.g. RMS, or peak-to-peak displacement). Also like other time-varying signals, jitter can be expressed in terms of spectral density (frequency content). Jitter period is the interval between two times of maximum effect (or between two times of minimum effect) of a jitter characteristic, for a jitter that varies regularly with time.

2.5. FR4 Material:

In surface mount technology (SMT) method for constructing electronic circuits, the components are mounted directly onto the surface of printed circuit boards (PCBs). These PCBs are usually FR4, which are ade with glass fibres buried in resin [13]. For high frequency there are other material, such as GETEK, ROGERS.4350, RLON CLTE which are often considered (Table 1)

Table 1: Material Characteristics of different laminates

Material	Relative permittivity	TanD–loss tangent	Temperature	Relative cost
FR4	4.4	0.018	180 ° C	1
GETEK	3.9	0.012	180 ° C	1.1
ROGERS 4350	3.5	0.004	280 ° C	2.1
ARLON CLTE	2.9	0.0026	288 ° C	5.8

As higher the frequency of the transmitting signal greater the losses in FR4. For this loss, signals loose high frequency components and thus signal definition [14]. Then a lower loss material is preferred.

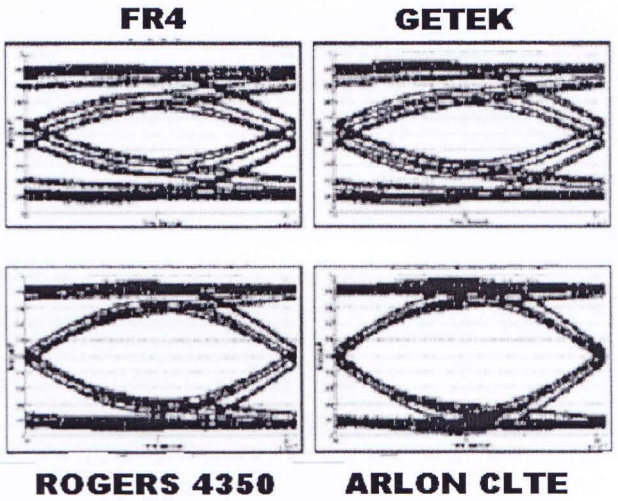

Figure 4: Effect on data eye of high frequency losses in printed circuit board

The output waveform showed here resulted from a 1-volt 32-bit inverting K28.5 input bit pattern (9.6 Gbps, 60 ps edges) that is applied to a 12mil, 50 Ohm strip line trace that is 18" long. Different material jitter and opening comparison (shown in figure 4) is given in table 2.

Table 2: Jitter at high frequency in different materials

Material	Jitter UI	**Opening, mV**
FR4	0.30	238
GETEK	0.28	268
ROGERS 4350	0.20	426
ARLON CLTE	0.19	520

2.6. Loss tangent:

If loss tangent is high then high frequency loss become more significant. So loss tangent is important for high frequency signal transmission. Power is lost in all dielectric materials, usually in the form of heat. Loss tangent (LT) [15]is expressed as the ratio of the resistive power loss to the capacitive power, and is equal to the tangent of the loss angle. In capacitors, LT is the ratio of a capacitor's equivalent series resistance (R) to its capacitive reactance (Xc). LT is usually expressed as a percentage.

$$LT = (R/Xc) \times 100\% = R/(1/\omega C) \times 100\% = \omega RC \times 100\%$$

2.7. Via

In PCB (printed circuit board) design, via , an example of which is shown in Figure 5, refers to a pad with a plated hole that connects copper tracks from one layer of the board to other layer(s) [16]. To be precise, in integrated circuit design, a via is a small opening in an insulating oxide

layer that allows metallic interconnect on different interconnect layers to form a connection Thus, vias are method to changing layers and for connecting devices across layers. Either the holes are electroplated or small rivets are inserted. A via on an integrated circuit is often called a through-chip via, where the via goes from top to bottom layer. High-density multi-layer PCBs may have blind vias, which are visible only on one surface, or buried vias, which are visible on neither (example image of each). Significant work has been done to deterine the effect of vias and also derive sufficiently accurate models [17].

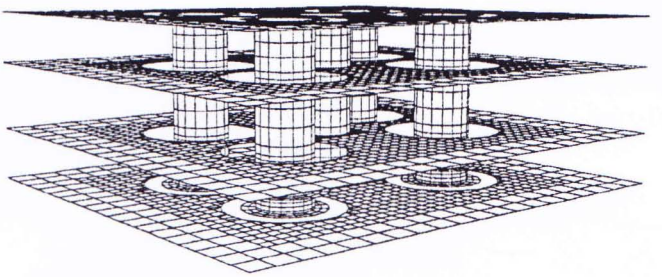

Figure 5: 3D view of vias in multiple layer

3. System Configuration

In our prescribed system, shown in figure 5 and 6, two microprocessors are placed, several inches apart on a printed circuit board (PCB). Microprocessors are connected or communicating with each other by a differential strip line. First traces from a micro processor go down at second layer through via. Then differential strip line carries over the connection in the second layer to some extent. And again traces come back to the top layer through via to connect with other microprocessor. For the sake of simplicity routing in other layer or transition in several layers wasn't considered. But in real world, it won't be always possible. The new systems are confined and the dimension or size decreasing day by day. Many components are packed into small space [18]. That is why; routing on PCB becomes very difficult. Traces have to bend and use multiple layers to connect different elements on PCB.

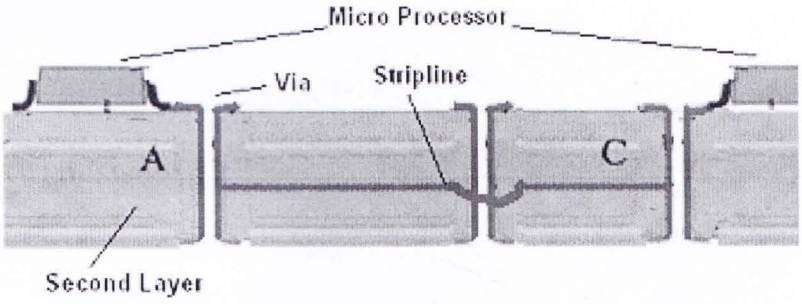

Figure 6: Configuration of system being analyzed (Side View)

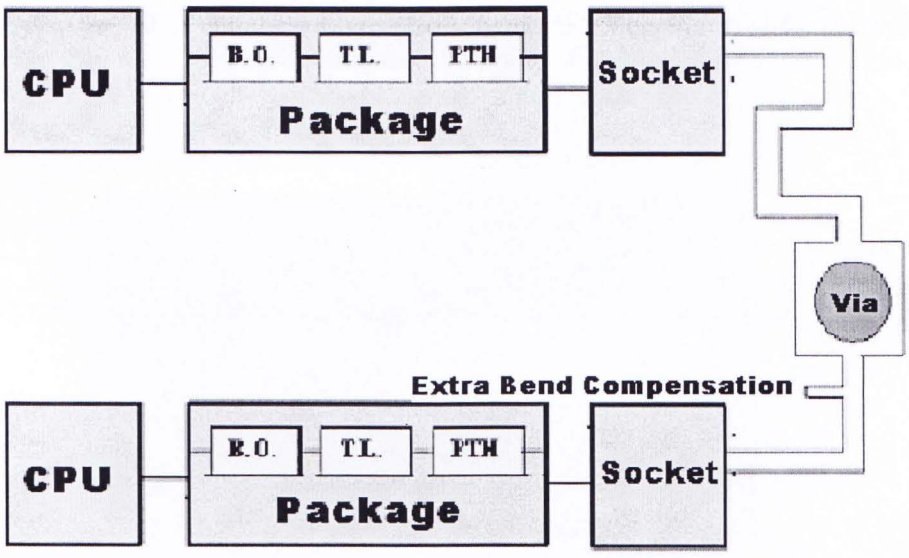

Figure 7: Configuration of system being analyzed (Top View)

This system has a power supply, which output voltage can vary from 1 to 2 Volt. But it has been considered that it supplies 1.05 Volt constantly to this system.

FR4 material is considered for the PCB in this system. The dielectric constant of the FR4 is about 4.4 [16]. The system is not considered to handle high frequency signal. But higher the frequency of the transmitting signal, greater the losses in FR4. For this loss, signals loose high frequency components and thus signal definition. Then a lower loss material is preferred. For high frequency signal sometimes GETEK, ROGERS.4350, RLON CLTE are used. FR4 is more cost effective than these materials.

The pin grid array or PGA type of packaging is used for microprocessors in this system. PGA type of packaging is chosen because for a given number of pins, this type of package occupies less space than older types such as the dual in-line package (DIP).

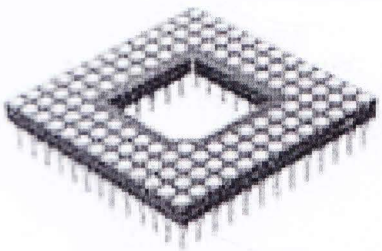

Figure 8: PGA type package

On the PGA type package, an example of which is shown in Figure 8, the microprocessor was mounted in a ceramic slab of which one face was covered, in a square array of metal pins. The pins then inserted into the holes rapidly in the FR4 printed circuit board and soldered in place. They were spaced 2.54 mm (a tenth of an inch) apart. These PGA type of packaged microprocessors are then inserted in this system by the sockets.

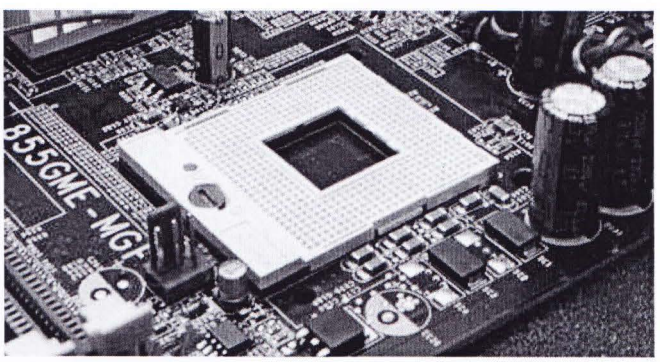

Figure 9: Socket on a printed circuit board.

The socket, an example of which is shown in Figure 8, which is placed on the PCB, accepts the microprocessor and forms an electrical interface with it. These sockets interfaces are based on

the pin grid array (PGA) architecture, in which short, stiff pins on the underside of the processor package mate with holes in the socket. To minimize the risk of bent pins, zero insertion force (ZIF) socket was chosen which allow the processor to be inserted without any resistance, and then grip the pins firmly to ensure a reliable contact after a lever is flipped.

The signal trace which is used on the printed circuit board (PCB) is the equivalent of a wire for conducting signals. Each trace consists of a flat, narrow part of the copper foil that remains after etching. Signal traces are usually narrower than power or ground traces because their current carrying requirements are usually much less. Typical there are two types of transmission line or trace construction, Microstrip and Strip line, an example of which is shown in Figure 10 [19].

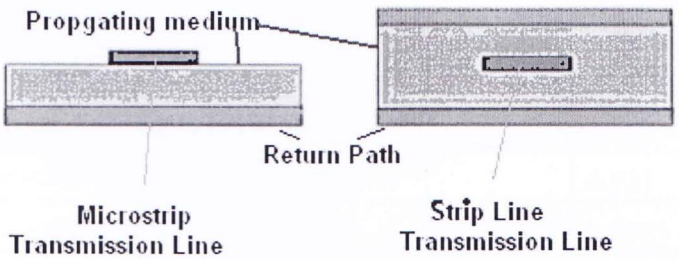

Figure 10: Types of Transmission Line

But in this case, differential strip line is considered. The differential strip line that is used in this system consists of two traces passing side by side carrying the opposite of same signal (see Figure 11). They are equally spaced over the whole path. Typical trace configuration of differential strip line has been chosen. The approximations are given below,

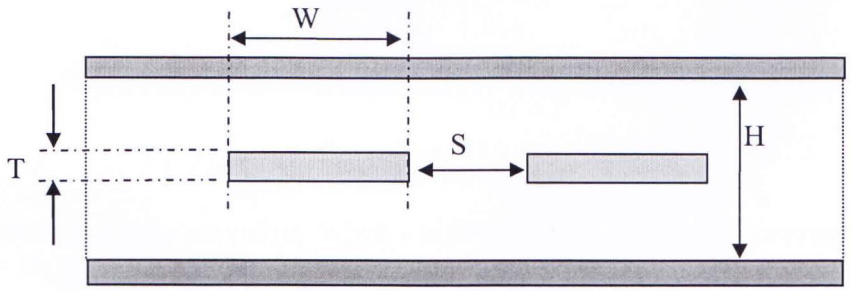

Figure 11: Differential Strip line

Table 3: Differential Strip Line Configuration

Characteristic Impedance (Ohms) Zo	50.0
Substrate Height (mils) H	5.0
Trace Spacing (mils) S	5.0
Finished Copper Weight (mils) T	1.4
Differential Impedance Zdiff (Ohms)	98.09

Differential Impedance is calculated with the following formula [20],

$$Z_{diff} = 2\,Z_0\left(1.347e^{\left(-2.9\left(\frac{S}{H}\right)\right)}\right)$$

Each strip line is considered to has the following configuration

Table 4: Characteristic parameters of Strip line

Dielectric Constant Er	4.4
Trace Width (mils) W	5.0
Finished Copper Weight (mils) T	1.4
Impedance Zo (Ohms)	39.73
Inductance/Inch Lo (nH/in)	7.769
Capacitance/Inch Co (pF/in)	4.921
Propagation Delay Tpd (nS/in)	0.1775

Strip line impedance, inductance, capacitance, propagation delay is calculated with the following formulas [21],

$$Z_0 = \frac{60}{\sqrt{E_r}} \ln\left(\frac{1.9\,(2H + T)}{0.8\,W + T}\right)$$

$$L_0 = 0.001 C_0 Z_0^2$$

$$C_0 = \frac{1.41 E_r}{\ln\frac{3.81H}{0.8W + T}}$$

$$T_{pd} = 0.0833 * 1.016\sqrt{E_r}$$

These formulas are approximation. When a high degree of accuracy is required, these equations should not be used [22]. Approximate formulas are widely available on the web on different websites, which are very helpful for quick calculations [23].

In this system, traces from one micro processor go down at second layer through via. Typical via is considered again to avoid complicacy. The configuration of via is given below with the figure 12 where 8 layer stack up vias considered. Minimum spaces or gap between via and differential line were considered according to this figure 12 in the whole calculation [24].

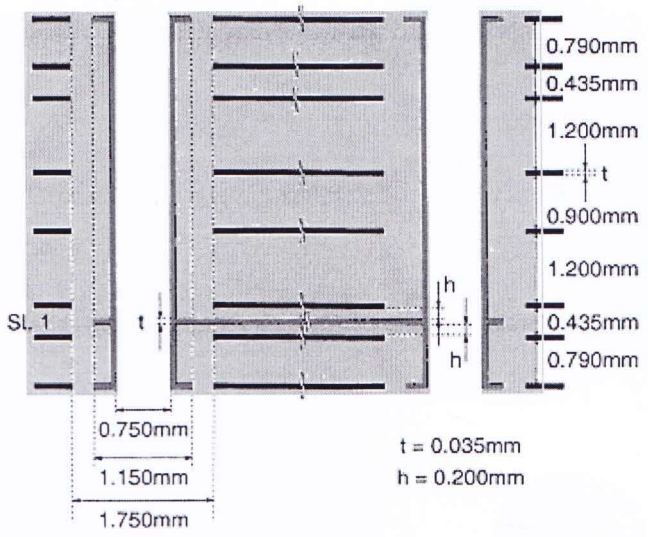

Figure 12: Configuration 8 layer printed circuit board through vias

In second layer strip line is required to bend several times to travel through a busy board (due to complex board layouts). For this, the wires of a differential strip line pair have mismatches in length. One is greater in length (2 * spacing of differential strip line) than the other. This mismatch can cause a serious problem in signal retrieving process from differential strip line. Thus, this mismatch is calculated and added extra strip line as lumped element to the strip line which was shorter in length. Extra length compensation is shown in figure 13.

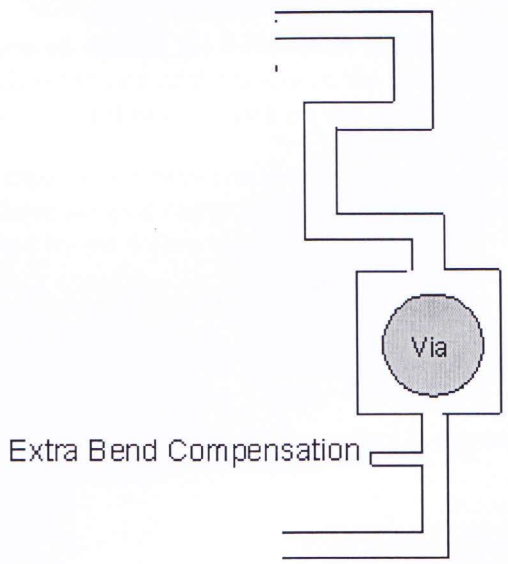

Figure 13: Extra length compensation to omit impudence mismatch

To determine the impact on mutual impedance between the traces and adjacent via, which is the main objective of the research, three types of via placement have been considered in this work. The differential strip line just passes the adjacent via at the second layer. This via can carry another signal or trace from first layer to other layer. But for the sake of simplicity, this via is considered as grounded and no signal is transmitted over this via. While calculating the capacitance all excess capacitance must be considered, which includes ground planes [25]-[26].

In the first via placement, which is shown in Figure 14, type 1, it has been considered that the via is placed between the differential strip line. It is placed such a way that the two wires are extended equally. For this, both differential strip line had to bend and extend equally.

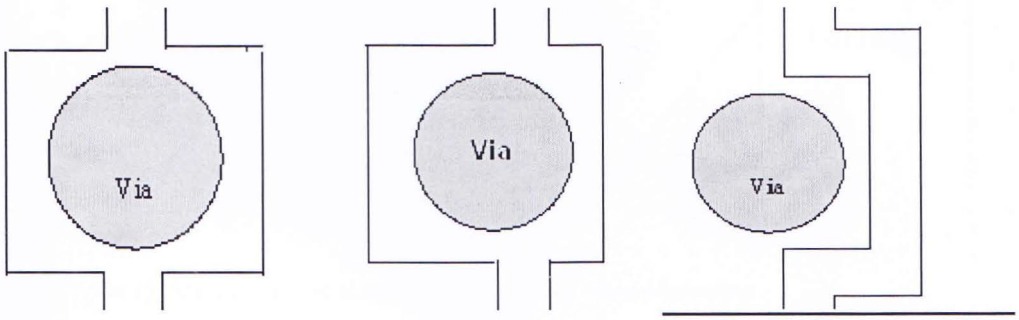

Figure 14: Via configurations, left - type 1, center – type 2, right - type 3.

In the second (type 2) configuration, which is shown in figure 14, the via was again placed in between the two conductors of the differential line. However, the via was placed away from the center, because of which one conductor has to be stretched or extended more then the other.

In the third case, the via was placed outside the differential line which is shown in Figure 14 (right). In this case the via is closer to one of the traces in the differential line. The intention of this configuration is to study the impact of cross talk on the line adjacent to the via.

To avoid complexity, mutual capacitance between via and adjacent trace of via is considered at two points at the trace. Thus these lumped components have some effects in signal transmission. Here capacitance C is calculated by the following equation

$C = \frac{\in A}{d}$ where, A is the interface area, d is the Minimum gap between via & trace.

Calculation of mutual capacitance for type 1 via configuration is shown in figure 15.

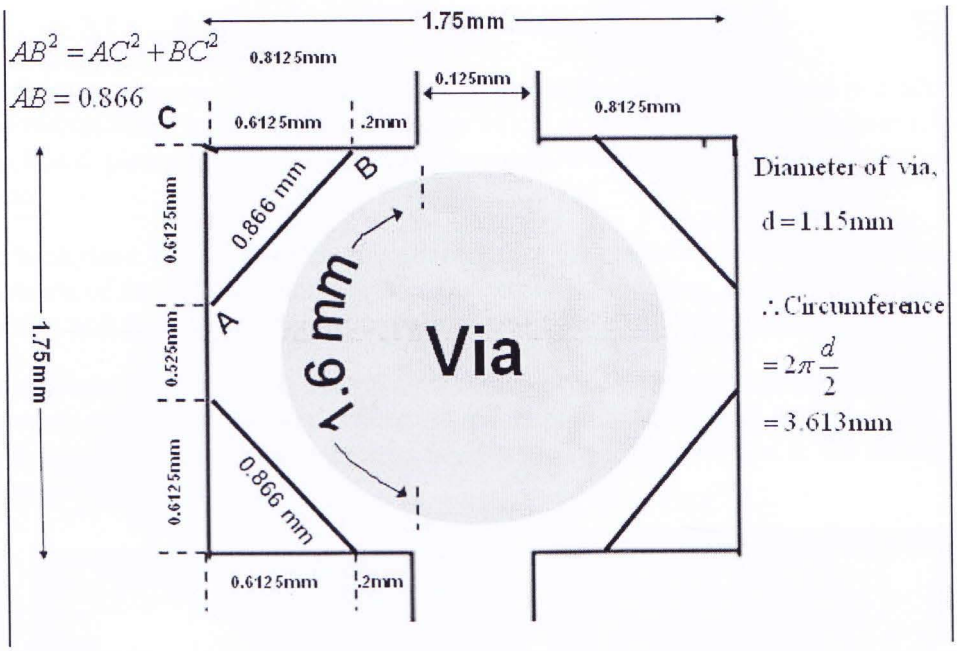

Figure 15: Measuring mutual capacitance of type 1 via configuration

All assumption are made according to figure 11.

Average interfacing length

$$L = \frac{(0.2 + 0.866 + 0.525 + 0.866 + 0.2) + 1.66}{2} mm = 2.159mm$$

A typical value of finished copper weight T is 0.035mm [16].

Then, the average area of adjacent wire and via circumference, A is given by

$$A = L \cdot T = 2.159 * 0.0350\, mm^2 = 0.07556mm^2 = 0.07556 \times 10^{-6} m^2$$

Minimum gap between via & trace, d = 0.3 mm = $0.3X10^{-3}$ m [13]
Permittivity of free space or the electric constant, $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m
The relative permittivity of the FR4 printed circuit board (From table 1) is $\varepsilon_r = 4.4$
Therefore, permittivity, $\varepsilon = \varepsilon_0\, \varepsilon_r = 8.854 \times 10^{-12} \times 4.4 = 12.408 \times 10^{-12}$ F/m

$$\text{Capacitance } C = \frac{\in A}{d} = \frac{12.408 \times 10^{-12} \times 0.07556 \times 10^{-6}}{0.3 \times 10^{-3}} = 3.125E-15 \text{ Farad}$$

This calculated mutual capacitance between via and adjacent trace of via is divided and considered at two points at the trace

3.1. Printed circuit board

The central or primary circuit board, in which a complex electronic system is made up, is called printed circuit board or motherboard (Figure 16). It is also known as a mainboard, baseboard, system board, planar board or, on Apple computers, a logic board, and is sometimes abbreviated as mobo.

Like a backplane, a PCB or motherboard, provides the electrical connections by which the other components of the system communicate. But unlike a backplane, a PCB also contains the central processing unit and other subsystems such as real time clock, and some peripheral interfaces.

A typical desktop computer is built with the microprocessor, main memory, and other essential components on the motherboard. Other components such as external storage, controllers for video display and sound, and peripheral devices are typically attached to the motherboard via edge connectors and cables.

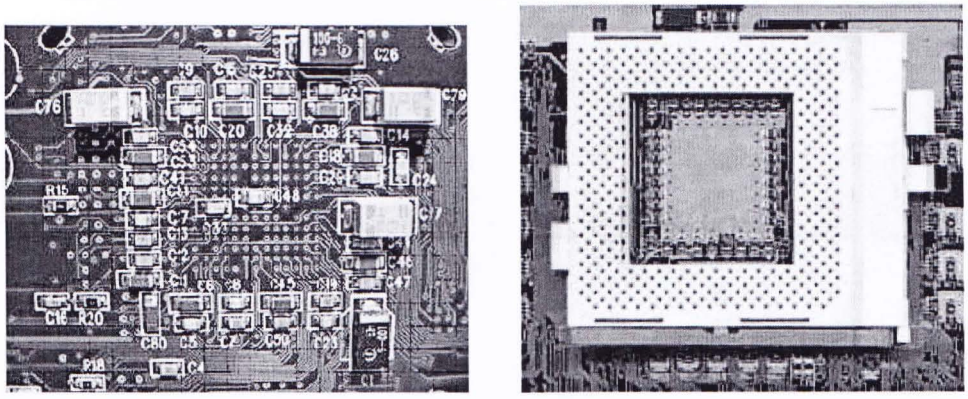

Figure 16: Surface mounted components and a CPU Socket of a Printed circuit board

3.2. CPU socket

On a computer's motherboard, a CPU socket (see Figure 16) or CPU slot is a connector that accepts a CPU and forms an electrical interface with it. Most CPU-sockets interfaces are based on the pin grid array (PGA) architecture, in which short, stiff pins on the underside of the processor package mate with holes in the socket. To minimize the risk of bent pins, zero insertion force (ZIF) sockets allow the processor to be inserted without any resistance, and then grip the pins firmly to ensure a reliable contact after a lever is flipped.

3.3. Package

The earliest integrated circuits were packaged in ceramic flat packs, which continued to be used by the military for their reliability and small size for many years. Commercial circuit packaging quickly moved to the dual in-line package (DIP), first in ceramic and later in plastic. In the 1980s pin counts of VLSI circuits exceeded the practical limit for DIP packaging, leading to pin grid array (PGA) and leadless chip carrier (LCC) packages. Surface mount packaging appeared in the early 1980s and became popular in the late 1980s, using finer lead pitch with leads formed as either gull-wing or J-lead, as exemplified by Small-Outline Integrated Circuit -- a carrier which

occupies an area about 30 – 50% less than an equivalent DIP, with a typical thickness that is 70% less. This package has "gull wing" leads protruding from the two long sides and a lead spacing of 0.050 inches.

In the late 1990s, PQFP and TSOP packages became the most common for high pin count devices, though PGA packages are still often used for high-end microprocessors. Intel and AMD are currently transitioning from PGA packages on high-end microprocessors to land grid array (LGA) packages.

Ball grid array (BGA) packages have existed since the 1970s. Flip-chip Ball Grid Array packages, which allow for much higher pin count than other package types, were developed in the 1990s. In an FCBGA package the die is mounted upside-down (flipped) and connects to the package balls via a package substrate that is similar to a printed-circuit board rather than by wires. FCBGA packages allow an array of input-output signals (called Area-I/O) to be distributed over the entire die rather than being confined to the die periphery.

Traces out of the die, through the package, and into the printed circuit board have very different electrical properties, compared to on-chip signals. They require special design techniques and need much more electric power than signals confined to the chip itself.

When multiple dies are put in one package, it is called SiP, for System In Package. When multiple dies are combined on a small substrate, often ceramic, it's called an MCM, or Multi-Chip Module. The boundary between a big MCM and a small printed circuit board is sometimes fuzzy. Two types common packaging are described below,

Pin Grid Array (PGA):

The pin grid array or PGA is a type of packaging used for integrated circuits, particularly microprocessors [19]. On a PGA, the integrated circuit (IC) is mounted in a ceramic slab of which one face is covered, or partially covered, in a square array of metal pins. The pins can then be inserted into the holes rapidly in a printed circuit board and soldered in place. They are almost always spaced 2.54 mm (a tenth of an inch) apart. For a given number of pins, this type of package occupies less space than older types such as the dual in-line package (DIP).

Ball Grid Array (BGA):

The BGA is a package with one face covered (or partly covered) with pins in a grid pattern [19]. These pins are used to conduct electrical signals from the integrated circuit to the printed circuit board (PCB) it is placed on. In a BGA, the pins are replaced by balls of solder stuck to the bottom of the package. The device is placed on a PCB that carries copper pads in a pattern that matches the solder balls. The assembly is then heated, either in a reflow oven or by an infrared heater, causing the solder balls to melt. Surface tension causes the molten solder to hold the package in alignment with the circuit board, at the correct separation distance, while the solder cools and solidifies.

3.4. Transmission Line and Signal trace:

In this analysis a transmission line was modeled to support signal propagation. The transmission line represents signal trace on a printed circuit board (PCB) which is the equivalent of a wire for

conducting signals. Each trace consists of a flat, narrow part of the copper foil that remains after etching. Signal traces are usually narrower than power or ground traces because their current carrying requirements are usually much less.

Typical there are two types of transmission line or trace construction. Those are –

- Microstrip
- Stripline

However, in this work, only stripline were considered.

3.4.1. Microstrip:

In electrical transmission line, there are several types of transmission line where Microstrip is one of them. Microstrip can be fabricated using printed circuit board [PCB] technology. As shown in the figure 17 below, it consists of a conducting strip separated from a ground plane by a dielectric layer known as the substrate. Microstrip lines are used in high-speed digital PCB designs, where signals need to be routed from one part of the assembly to another with minimal distortion, and avoiding high cross-talk and radiation.

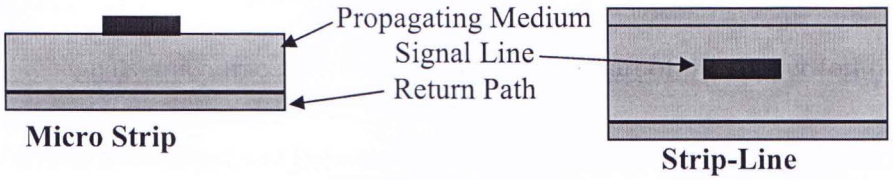

Figure 17: Microstrip (left, above) and Strip Line (right, above) configuration of transmission lines

3.4.2. Stripline:

A strip line is a flat strip of metal which is sandwiched between two parallel planes. The insulating material of the substrate forms a dielectric. The width of the strip, the thickness of the substrate and the relative permittivity of the substrate determine the characteristic impedance of the strip which is a transmission line. As shown in the figure 17 , the central conductor need not be equally spaced between the ground planes. In the general case, the dielectric material may be different above and below the central conductor. A strip line transmission line is similar to a microstrip, except that the microstrip is not sandwiched between two power planes.

4. Data Analysis And Solution

While designing the layout of the transmission lines, certain design rules should be considered. Such as, rise time should not be more than half of the period of the signal. If the rise time is half of the period then the signal will take the form of a triangular wave shape. Also, as a result, the output signal does not get enough time to fall properly to represent binary 0 or logic low. That is why; we should select rise time according to the frequency or data rate.

Here simulation on all the types of via placement is done and from the result eye diagram is plotted. From the eye diagram jitter, setup time, hold time, high margin and low margin is calculated and compared at table 5 (without via)and table 6 (with via) to study the impact of impedance mismatch on the differential impedance on a single line of the pair due to different placement of via near the differential micro strip trace. Eye diagrams are listed below (figure 18 to 23).

On type 3 (worst case) via placement configuration, simulation with two separate frequencies 1 GHz and 3 GHz is done and eye diagrams are showed in figure 24 to 27 to study the impact of impedance mismatch on the differential impedance due to via impact on a single line of the pair. The results are listed at table 7.

Eye diagrams (figure 28 to 31) are the result of analysis done separately on two different trace lengths, at 13 inch and 24 inch. Data is listed in table 8.

Table 9 shows the comparison between eye openings of different configuration.

All the figures depicting the eye at the receiver for different configuration are listed below. At table 5, jitter of all the types of via placement configuration is observed, which shows maximum jitter for type 3 via. Worst Setup time is observed for type 1 via. It is observed that both setup and hold time is maximum for the type 1 via.

Table 5: Eye analysis data for transmission line without via at 3 GHz

Via Placement		Type 1	Type2	Type3
Setup time	T_{setup} (ns)	11.8	11.3	11.2
Hold time	T_{hold} (ns)	11.7	11.4	11.3
High Margin	H_{marg} (V)	0.79	0.78	0.77
Low Margin	L_{marg} (V)	0.76	0.75	0.75
Jitter	J (ns)	0.6	0.62	0.64

Simulation of the motherboard configuration without via was done at 3 GHz for a transmission line that was 13 inches long. The eye observed for the different cases are shown in Figures 18-20.

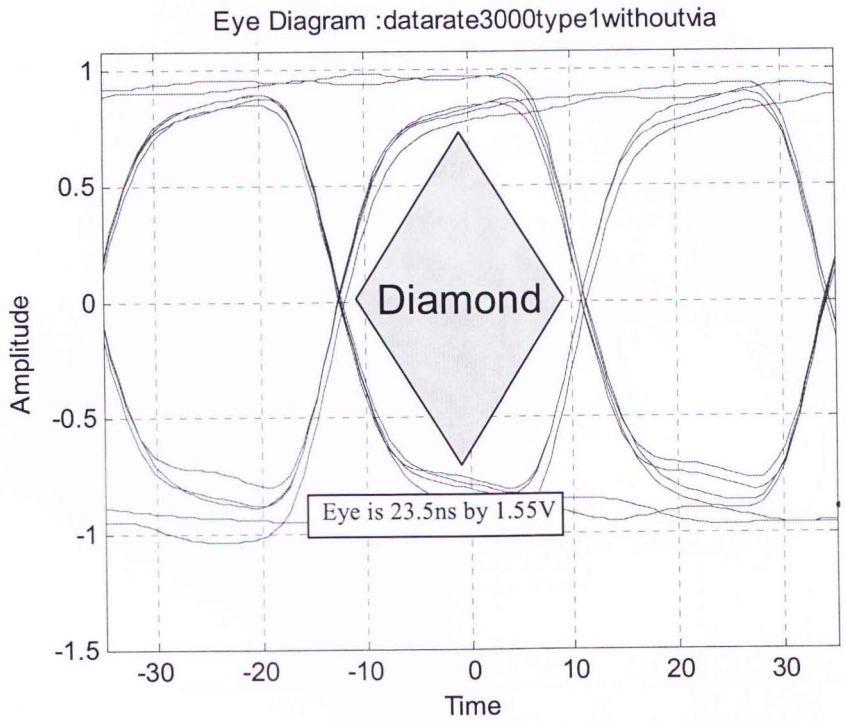

Figure 18: Eye diagram of Design type 1without via at 3GHZ.

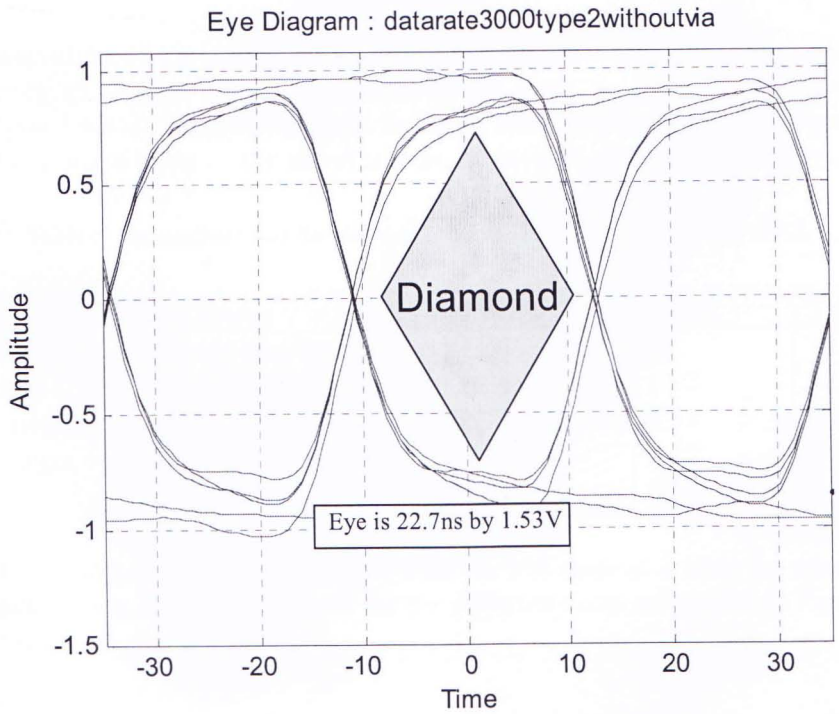

Figure 19: Eye diagram of Design type 2 without via at 3GHZ.

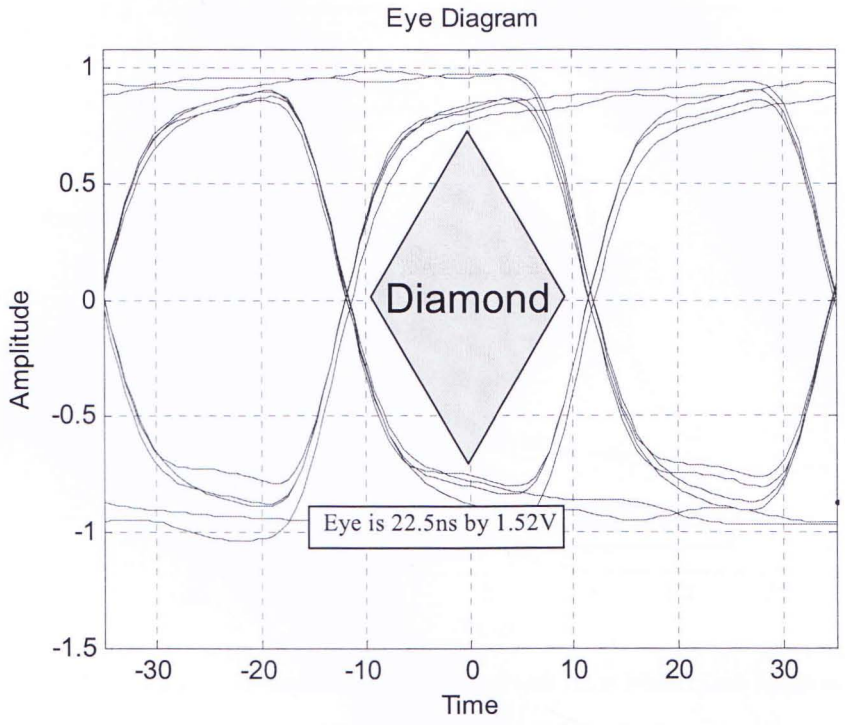

Figure 20: Eye diagram of Design type 3 without via at 3GHZ. Line length is 13".

At table 6, observation of via impact on all the types of via placement configuration is observed at a higher frequency (3 GHZ), which shows maximum jitter for type 3 via. Worst Setup time is observed for type 1 via. It is again observed that both setup and hold time is maximum for the type 1 via. The most important thing is, the effect is more noticeable at higher frequency.

Table 6: Eye analysis data for transmission line (13 inches) and via at 3 GHZ.

Via Placement		Type 1	Type2	Type3
Setup time	Tsetup (ns)	11.44	12	11.1
Hold time	Thold (ns)	11.45	11.2	11.1
High Margin	Hmarg (V)	0.771	0.74	0.73
Low Margin	Lmarg (V)	0.76	0.72	0.72
Jitter	J (ns)	0.61	0.65	0.67

Simulation of the motherboard configuration with via was done at 3 GHz for a transmission line that was 13 inches long. The eye observed for the different cases are shown in Figures 21 to 23.

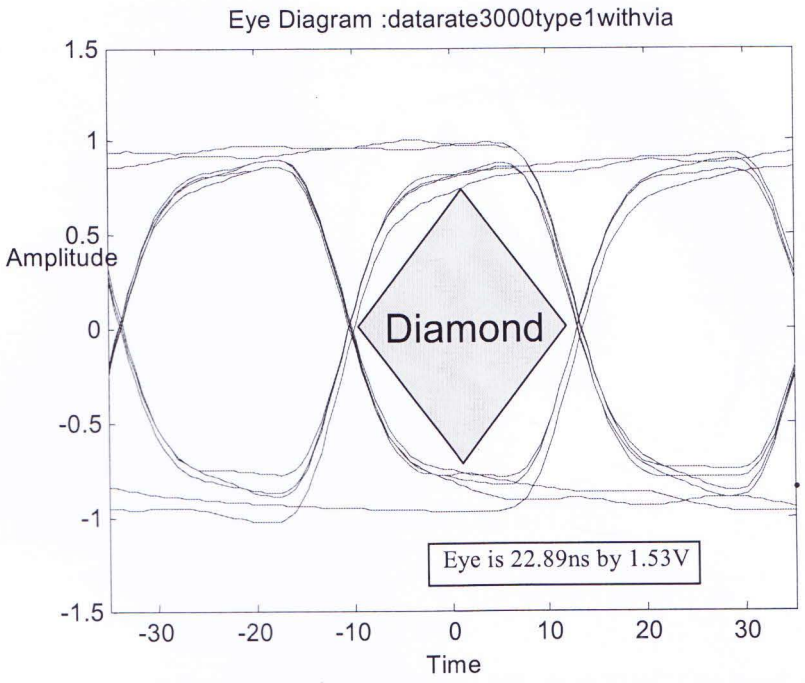

Figure 21: Eye diagram of Design type1with via at 3GHZ. Line length is 13".

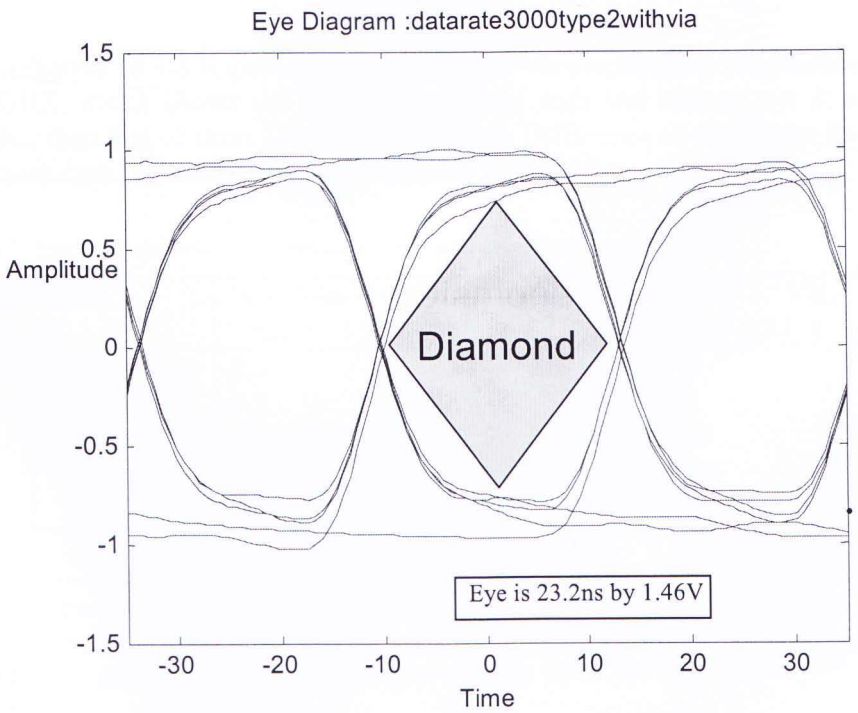

Figure 22: Eye diagram of Design type 2 with via at 3GHZ. Line length is 13".

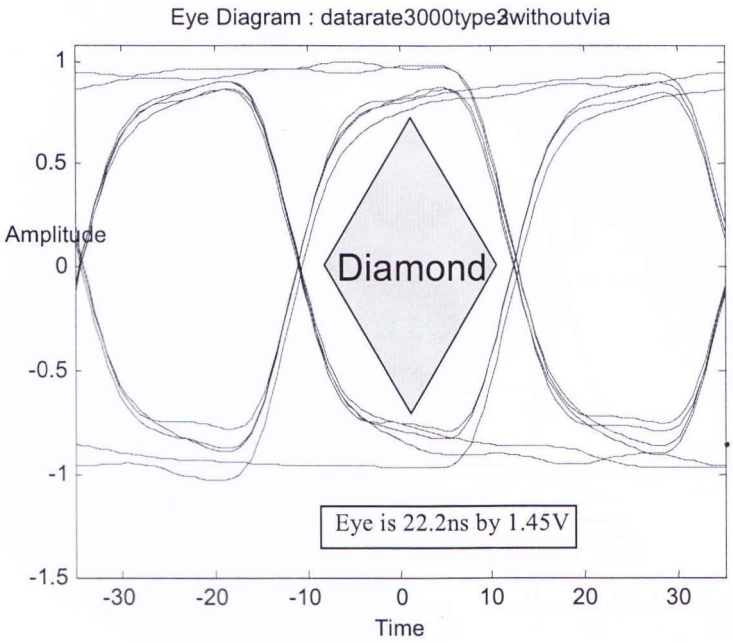

Figure 23: Eye diagram of Design type 3 with via at 3GHZ. Line length is 13".

At table 7 observation of via impact on only the type 3 via placement configuration is observed at a frequency 1 GHZ, which shows the difference of jitter with and without via at long T-line (at 24 inches) is higher than that of short T-line (at 13 inches). Difference of setup time for 13 inches T-line is observed lesser than 24 inches T-line but opposite for hold time.

Table 7: Eye analysis data for transmission line with or without via at 1 GHZ

Via Placement Type 3		With Via Trace =13 in	W/O Via, Trace = 13 in	With Via, Trace = 24 in	W/o Via, Trace = 24 in
Setup time	Tsetup (ns)	8.3	8.5	7.5	7.8
Hold time	Thold (ns)	8.3	8.6	7.8	7.9
High Margin	Hmarg (V)	0.72	0.78	0.55	0.6
Low Margin	Lmarg (V)	0.76	0.79	0.67	0.7
Jitter	J (ns)	0.4	0.5	0.81	0.9

Simulation of the motherboard configuration of only type 3 via placement configuration with and without via was done at 1 GHz for a transmission line that was 13 inches or 24 inches long. The eye observed for the different cases are shown in Figures 24 to 27

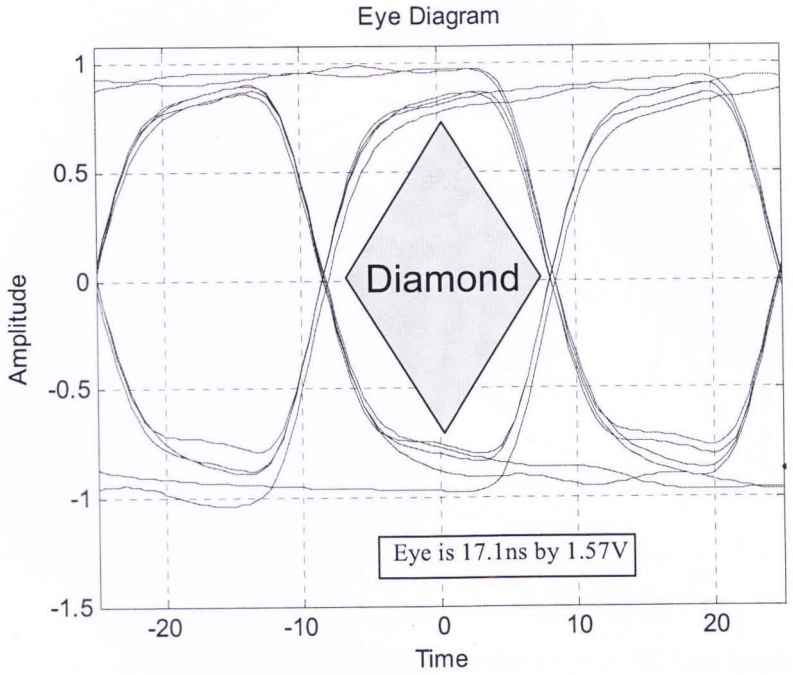

Figure 24: Eye diagram of Design type 3 without via at 1 GHZ. Line length is 13".

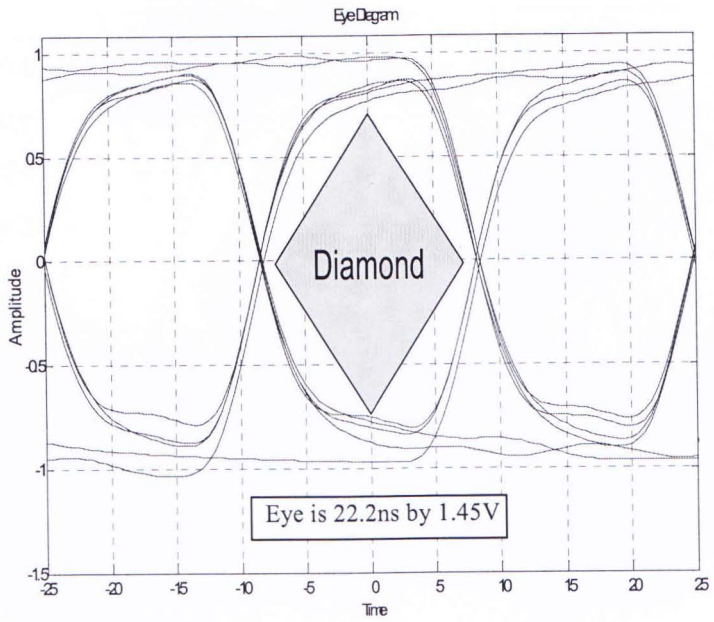

Figure 25: Eye diagram of Design type 3 with via at 1 GHZ. Line length is 13".

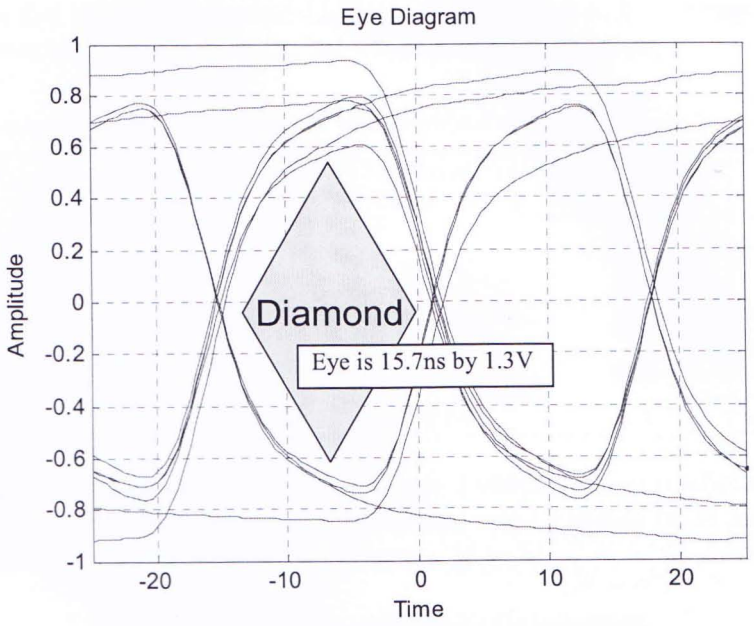

Figure 26: Eye diagram of Design type 3 without via at 1GHZ. Line length is 24".

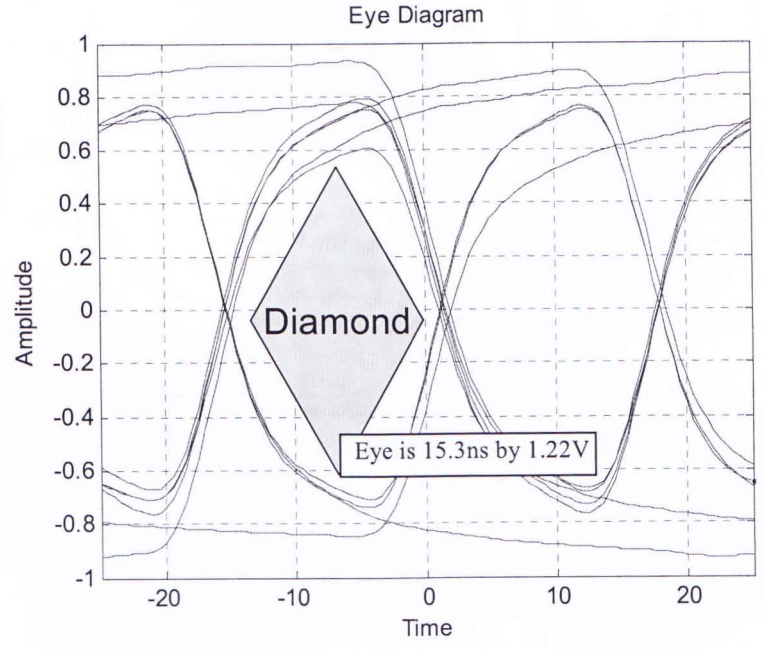

Figure 27: Eye diagram of Design type 3 with via at 1GHZ. Line length is 24".

At table 8 the type 3 via placement configuration is observed at a frequency 3 GHZ for different T-line length, which again shows the difference of jitter with and without via at long T-line (at 24

inches) is higher than that of short T-line (at 13 inches). Difference of both setup and hold time for 13 inches T-line is observed lesser than 24 inches T-line at higher frequency.

Table 8: Eye analysis data for transmission line with or without via at 3 GHZ (type 3 via)

Via Placement Type 3		With Via Trace = 13 in	Without Via Trace = 13 in	With Via Trace = 24 in	Without Via Trace = 24 in
Setup time	Tsetup (ns)	11.1	11.2	10.2	10.6
Hold time	Thold (ns)	11.1	11.3	10.3	10.7
High Margin	Hmarg (V)	0.73	0.77	0.52	0.56
Low Margin	Lmarg (V)	0.72	0.75	0.65	0.67
Jitter	J (ns)	0.67	0.64	1.1	1.7

Simulation of the motherboard configuration of only type 3 via placement configuration with and without via was done at 3 GHz for a transmission line that was 13 inches or 24 inches long. The eye observed for the different cases are shown in Figures 28 to 31.

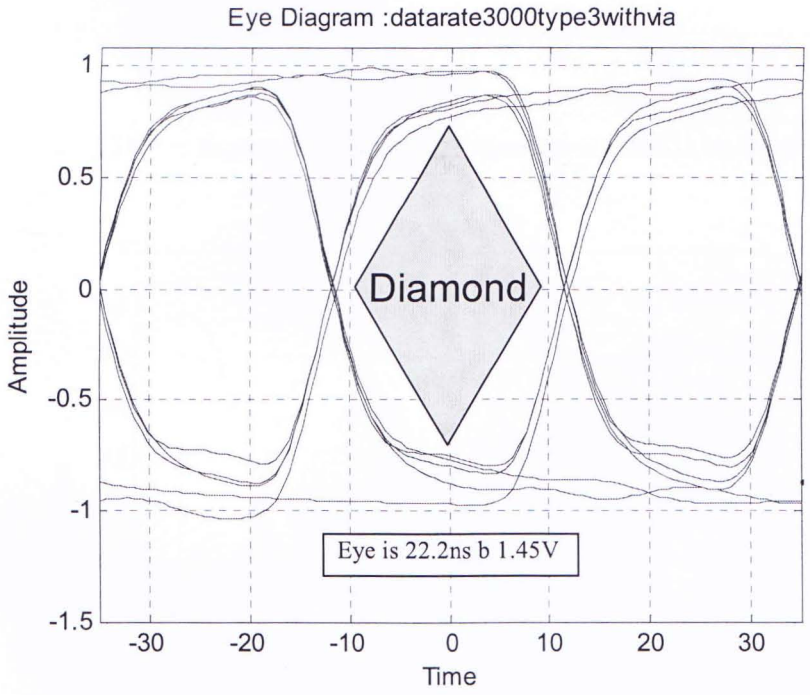

Figure 28: Eye diagram of Design type 3 with via & data rate is 3 GHZ. T-line is 13" long.

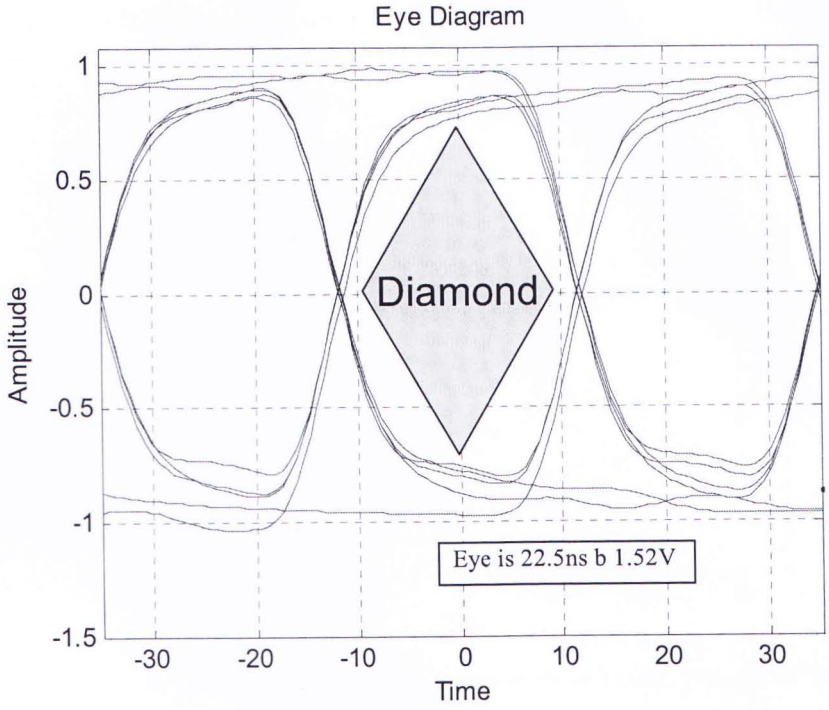

Figure 29: Eye diagram of Design type 3 without via at 3 GHZ. Line length is 13".

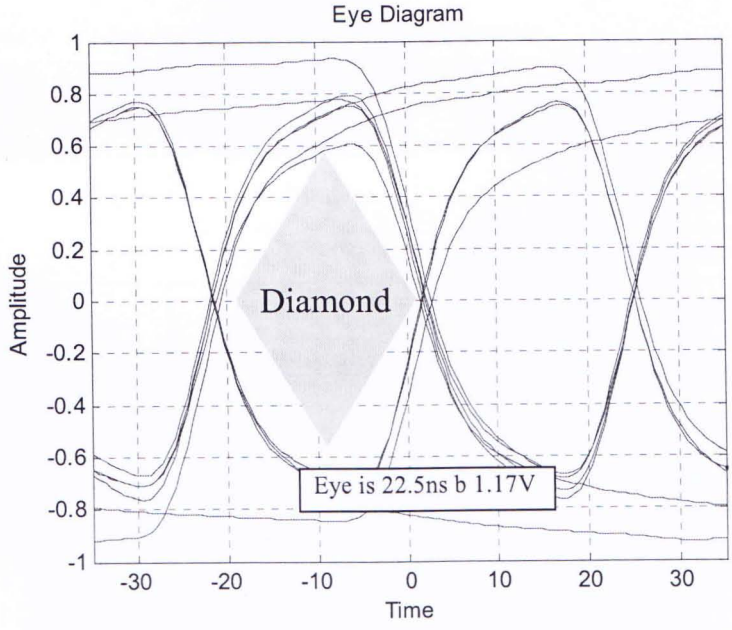

Figure 30: Eye diagram of Design type 3 with via & data rate is 3 GHZ. T-line length is 24" long.

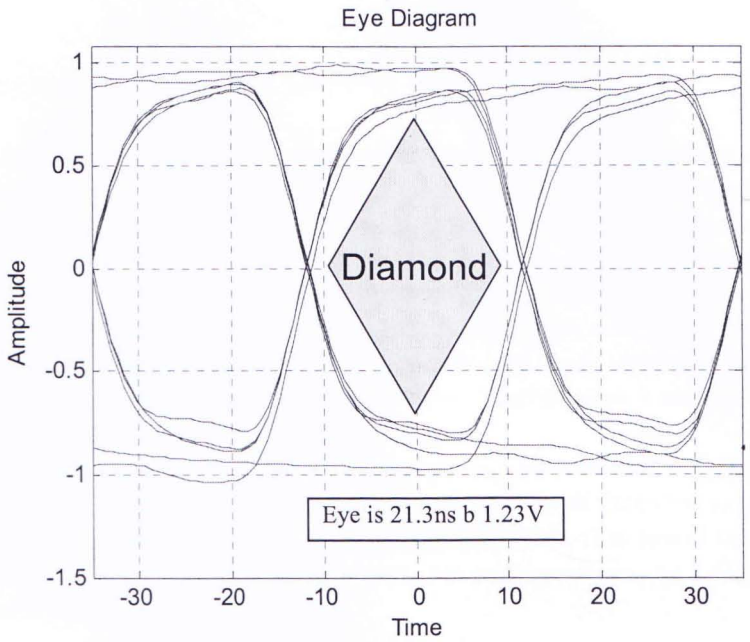

Figure 31: Eye diagram of Design type 3 without via at 3 GHZ. T-line is 24" long.

Table 9 compares the eye openings of different configurations. It is observed that at higher frequency and longer T-line eye opening is worst.

Table 9: Comparison between eye openings of different configuration

Frequency	Line length	via	Design Type	Eye opening
1 GHZ	13"	Without Via	Type3	17.1ns by 1.57V
		With Via		22.2ns by 1.45V
	24"	Without Via		15.7ns by 1.3V
		With Via		15.3ns by 1.22V
3 GHZ	13"	Without Via	Type1	23.5ns by 1.55V
			Type2	22.7ns by 1.53V
			Type3	22.5ns b 1.52V
		With Via	Type1	22.89ns by 1.53V
			Type2	23.2ns by 1.46V
			Type3	22.2ns b 1.45V
	24"	Without Via	Type3	21.3ns b 1.23V
		With Via		22.5ns b 1.17V

From the result of the simulations done, the following can be concluded....

1. Different via placements: As mentioned earlier three types of placement of via near the differential micro strip trace is chosen. Simulation on all the types is done and from the result eye diagram is plotted. From the eye diagram jitter, setup time, hold time, high margin and low margin is calculated to study the impact of impedance mismatch on the differential impedance on a single line of the pair due to different placement of via near the differential micro strip trace. It is found that the difference of jitter for type 1, type 2 and type 3 via placement configuration without via and with via is 0.01, 0.03 and 0.03 respectively. Eye opening change drastically at type 3 rather than 1 and 2.

2. Different signal propagation frequency: Two separate frequencies 1 GHz and 3 GHz is chosen to study the impact of impedance mismatch on the differential impedance due to via impact on a single line of the pair. Comparing the result, it is found that 3 GHz (High frequency) has great effect on type 3 via placement configuration. At 1 GHz jitter of type 1 is 0.81 whereas at 3 GHz jitter is 1.1.

3. Different length configuration: Analysis is also done separately on two different trace lengths, at 13 inch and 24 inch. At 1 GHz frequency jitter of 13 inch length trace type 3 via placement configuration is 0.4 and jitter of 24 inch length trace is 0.81.

Observing impact of different via placement topologies, it is clear that worst impact was on type 3 where as type 2 is moderate and type 1 is the best.

5. Conclusion

The effect of a via on the impedance of a differential pair has been analyzed. Mutual capacitance between via and the adjacent trace is considered at two points of a transmission line trace. The obtained results provide guidelines for via and trace placement for minimizing the effect of adjacent via on differential pair. That is the goal of this work. The simulation results have been verified with simulation up to 9GHz. The simulation model developed using this methodology has also been compared with the distributed element model and is found to be more accurate.

Analyses of different via configuration were observed. Three types of placement of via near the differential micro strip trace have been considered. Simulation analyses on all the configurations have been done. The resultant eye diagram for random bit patterns have also been generated and analyzed. From the eye diagram jitter, setup time, hold time, high margin and low margin were calculated to study the impact of impedance mismatch on the differential impedance on a single line of the pair due to different placement of via near the differential micro strip trace. It is found that the difference of jitter and eye opening change drastically at type 3 rather than 1 and 2. In type 3 the via is placed adjacent to one of the traces in the differential lines (outside the pair), while in the other types the via is placed within the differential pair.

Analysis of the different length configuration from the via coupling perspective was observed. Different length configuration analysis is done separately on two different trace length, 13 inches and 24 inches.

Two separate signal propagation frequency 1 GHz and 3 GHz is chosen to study the impact of impedance mismatch on the differential impedance due to via impact on a single line of the pair. Comparing the result, it is found that 3 GHz (High frequency) system has great effect on type 3 via placement configuration than 1 GHz. For the different cases studied, eye diagrams were calculated to characterize the performance of the transmission line and via interaction. Observing impact of different via placement topologies, it is clear that worst impact was on type 3 where as type 2 is moderate and type 1 is the best.

6. Future work

In this system, the mutual capacitance between traces of a differential pair and via is considered. The via is modeled as a lumped element. In spice modeling of a transmission line, the via is bifurcated and added to the beginning and ending node of the transmission line segment. For more accurate modeling of the via, a distributed model needs to be considered.

For a distributed model implementation, the trace and via must be divided into multiple segments. Each segment's impedance can be calculated by PI network model or T network.

The main focus of this research was to determine the capacitive coupling between via and differential strip line but not on micro strip. Future work can be done on determining the coupling between via and micro strip.

In this analysis a single layer differential strip line is used to connect the devices. This was done to simplify the analysis, keeping focus on the via effects. Therefore routing in other layers and transition between several layers wasn't considered. But in practical system layouts, many components are located on typical printed circuit boards sharing limited landscape. Such boards are typically between 6-14 layers where routing from device to device transitions between layers to accolade complex layout configurations. In these configurations traces also need to bend. These considerations between several layers must be considered.

7. References

[1] P. I. Kuznetsov and R. L. Stratonovich, "The Propagation of Electro-magnetic Waves in Multiconductor Transmission Lines", New York: Pergamon, 1964.

[2] Harrington, Roger F., "Field Computation by Moment Methods", Pub: MacMillan 1968

[3] Richard E. DuBroff, "Electromagnetic Concept and Application", 4th edition, Prentice Hall, Inc. 1996

[4] R. F. Harrington, "Time Harmonic Electromagnetic Fields", New York: McGraw-Hill, 1961.

[5] C. R. Paul and W. W. Everett, "Printed circuit board crosstalk," in Proc. Int. IEEE EMC Symp., 1985, pp. 452-459.

[6] S. Frankel, "Multiconductor Transmission Line Analysis", Dedham, MA: Artech House, 1977.

[7] Howard Johnson & Martin Graham, "High Speed Signal Propagation", Pearson Education Inc, 2003.

[8] Hart, Bryan, "Digital Signal Transmission", Pub: Chapman and Hall 1988.

[9] D. A. Hill, K. H. Cavcey, and R. T. Johnk, "Crosstalk between microstrip transmission lines," Nat. Inst. Standards Techn. Tech. Rep. NISTIR 5015, 1993.

[10] R. K. Hoffman, "Handbook of Microwave Integrated Circuits", Norwood, MA: Artech House, 1987.

[11] J. C. Isaacs and N. A. Strakhov, "Crosstalk in uniformly coupled lossy transmission lines," Bell Syst. Tech. J., vol. 52, pp. 101-115, 1973.

[12] Clayton R Paul, "Electromagnetic Compatibility", John Wiley & Sons, Inc, 2006, 2nd Edition.

[13] Hall, S., G. W. Hall, and J. A. McCall, "High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices", John Wiley & Sons, INC., New York, 2000.

[14] C. R. Paul, "Frequency response of multiconductor transmission lines illuminated by an electromagnetic field," *IEEE Trans. Electromagn. Compat.*, vol. EMC-18, pp. 183-190, 1976.

[15] M. Pozar, "Microwave Engineering", John Wiley & Sons (Asia) Pvt. Ltd, 2004.

[16] Johnson, H. W. and M. Graham, "High Speed Digital Design", A Handbook of Black Magic, Prentice Hall, NJ, 1993.

[17] E. Laermans, J. De Geest, D. De Zutter, F. Olyslager, S. Sercu, and D. Morlion, "Modeling complex via hole structures," in Proc. 10th Topical Meeting Elect. Performance Electron. Packag., Cambridge, MA, Oct. 2001, pp. 149–152.

[18] C. Wei, R. F. Harrington, J. R. Mautz, and T. K. Sarkar, "Multiconductor transmission lines in multilayered dielectric media," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-32, pp. 439450, 1984.

[19] K. C. Gupta, R. Garg, and I. J. Bahl, "Microstrip Lines and Slotlines", Dedham, MA: Artech House, 1979.

[20] Douglas Brooks, "Differential Impedance", Printed Circuit Design, a Miller Freeman publication, August, 1998.

[21] "Design Guidelines for Electronic Packaging Using High Speed Techniques", IPC-D-317A, January 1995.

[22] C. R. Paul and A. E. Feather, "Computation of the transmission line inductance and capacitance matrices from the generalized capacitance matrix," *IEEE Trans. Electromagn. Compat.*, vol. EMC-18, pp. 175-183, 1976.

[23] CITS25, Differential Controlled Impedance Calculator, Polar Instruments Ltd.

[24] Eric Laermans, Member, Jan De Geest, Daniël De Zutter, Frank Olyslager, Stefaan Sercu, and Danny Morlion, "Modeling Complex Via Hole Structures", *IEEE Trans. on advanced packaging*, vol. 24, no. 3, August 2001

[25] P. A. Kok and D. De Zutter, "Capacitance of a circular symmetric model of a via hole including finite ground plane," *IEEE Trans. Microwave Theory Tech.*, vol. 39, pp. 1229–1234, July 1991.

[26] Kok, P.A.; de Zutter, D. "Prediction of the excess capacitance of a via-hole through a multilayered board including the effect of connecting micro strips or strip line," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 2270–2276, Dec. 1994.

8. Appendix

8.1. Netlist File: (Via Type 1 and type 2)

** Project : **Via coupling EFFECTS on signal propagation**

```
*Linear Driver

*-- Voltage parameters
.param vdd      = 1.05          $ in volts

*-- Driver Parmaters
.param cpu_ccomp      = 1.5p      $ driver ccomp in pF
.param rise_time      = 50p   $750p      $ in ps

*-- Driver parameters
.Param data_rate = 3000          $ in MT/s
.param clock_speed = 'data_rate/2'          $ 667MHz
.param freq       = '(clock_speed/2)*1e6'       $ 333MHz
.param period_ctl = '1/freq'
.param period      = '1/freq'
.param pw       = 'period/2'
.param pw_ctl       = 'period/2'
.param half_pw      = 'pw_ctl/2'
.param delay_start_ctl      = 0n
.param delay_start_data      ='delay_start_ctl+period_ctl+period_ctl-half_pw'

        $ use this if simulating a clock to delay for settling

.param data_delay      = 'delay_start_data'
.param idrvm       = 1.0
.param dtr       = rise_time
.param dtf       = rise_time+40p
.param dpwr      = '(period/2)-dtr'
.param dpwf      = '(period/2)-dtf'
.param ron_pmos = 50          $ driver impedance settings pmos
.param ron_nmos = 25          $ driver impedance settings nmos
.param sim_time = 'delay_start_ctl+(70*pw_ctl)'

.param rc = 50
.param m_in =          0.0254       $ meter/inch

* CPU parameter
.param cpu1_tl_mr = '0.469*m_in'   $ in.

* MB

.param mb_tl1 =          '(2*m_in)' $ in.
.param mb_tl2 =          '(2*m_in)' $ in. $Parts of CPU1 to CPU2 TRL length
.param mb_tl3 =          '(2*m_in)' $ in. $ Parts of CPU1 to CPU2 TRL length
.param mb_tl4 =          '(1*m_in)' $ in. $ Parts of CPU1 to CPU2 TRL length
.param mb_tl5 =          '(1*m_in)' $ in. $ Parts of CPU1 to CPU2 TRL length
.param mb_tl6 =          '(1*m_in)' $ in. $ Parts of CPU1 to CPU2 TRL length
.param mb_tl7 =          '(1*m_in)' $ in. $ Parts of CPU1 to CPU2 TRL length
.param mb_tl8 =          '(1*m_in)' $ in. $ Parts of CPU1 to CPU2 TRL length
.param mb_tl9 =          '(1*m_in)' $ in. $ Parts of CPU1 to CPU2 TRL length

* length of trace beside via for different types of Via
.param mb_tl_str_via_type1 =          '(0.0027)' $ m. $ length of trace beside Via type 1
.param mb_tl_str_via_type2a =          '(0.0033)' $ m. $ length of trace beside Via type 2a
```

```
.param mb_tl_str_via_type2b =          '(0.002)' $ m. $ length of trace beside Via type 2b
                                            *Different length at two side as they are not equal
.param mb_tl_str_via_type3 =          '(0.0016)' $ m. $ length of trace beside Via type 3
.param mb_tl_bend =          '( 0.0003)' $ m. $ extra bend length compensation


*Assign length of the trace beside to change the type of Via
.param Extra_Length_trace_1 =          'mb_tl_str_via_type1' $ m
.param Extra_Length_trace_2 =          'mb_tl_str_via_type1' $ m. $Via length type 1


* capacitance for different types of Via
 .param type1_via_capacitane_1 = 3.1250e-15/2          $ in Farade
 .param type2a_via_capacitane_2a = 3.8223e-15/2
 .param type2b_via_capacitane_2b = 3.941e-15/2
 .param type3_via_capacitane_3 = 3.5858e-15/2


* Assign cpacitance of the trace beside to change the type of Via
 .param via_capacitane_1 = 'type1_via_capacitane_1'          $ in Farade
 .param via_capacitane_2 = 'type1_via_capacitane_1'


.param cpu1_pf_len =      '0.8*m_in'      $ in.
.param cpu2_pf_len =      '0.8*m_in'      $ in.
.param top_board2buf_len = '0.5*m_in'     $ in.


*-- HSPICE simulator parameters
.option probe post=1 measdgt=6
.width co = 132
.tran  20e-12 sim_time
.option ingold=1              $ to print data points without unit
*-------------------------------------------------------------------------
*     Include Files
*-------------------------------------------------------------------------
.include '..\saadinclude\linear_driver.inc'
.include '..\saadinclude\bit_patterns_ctl_aug05.inc' $ defines bit pattern
********** included files ************************************
* CPU Package
.inc '..\saadinclude\PKG\breakout_w_rect.sp'
.inc '..\saadinclude\PKG\ddd_667_MinZ.sp'   $ the copy of this file is given below
.inc '..\saadinclude\PKG\pth_3io.sp'
.inc '..\saadinclude\PKG\socket.sp'

* Motherboard
.inc '..\saadinclude\MB1066\mb_minz.rlc' $ the copy of this file is given below
.inc '..\saadinclude\MB1066\mb_minz_bend.rlc'    $ the copy of this file is given below

-------------------------------------------------------------------------
*-- Voltage Rails
V_vsm vddq gnd vdd

*-- Bit Pattern Drivers
Xdrive_CSC1 sdata1 CTL_pulse_DRIVER1       $ diff1 bit pattern defined in bit pattern file
Xdrive_CSC2 sdata2 CTL_pulse_DRIVER2       $ diff2 bit pattern defined in bit pattern file

*-- VCVS with bessel filter input on PWL stimulus
Rfltd1  sdata2 ctl_in  3                   $ diff2 source
xfltd1  ctl_in ctl_out gnd  Bessel2 f3db=3G       $ diff2 3dB filter

Rflts1  sdata1  iws1  3                    $ diff1 source
```

```
xflts1  iws1 cws1 gnd  Bessel2 f3db=3G       $ diff1 3B filter

*-- Driver call
xdrvc1  vddq gnd cpu1_pad_diff2 ctl_out  VCR_driver   $ diff2 behavioral driver
Cmch_1  cpu1_pad_diff2 gnd cpu_ccomp

xdrvds1  vddq gnd cpu1_pad_diff1 cws1  VCR_driver   $diff1 behavioral driver
Ccpu_s1  cpu1_pad_diff1 gnd cpu_ccomp


* CPU1
x_cpu1_breakout_mr  cpu1_pad_diff1     cpu1_pad_diff2   0
 +          cpu1_bo_diff1_mr   cpu1_bo_diff2_mr   0
 +          gnd breakout_w_rect

* CPU Package Transmission Line
w_cpu1_tl_mr N=2
 + cpu1_bo_diff1_mr cpu1_bo_diff2_mr  gnd
 + cpu1_tl_diff1_mr cpu1_tl_diff2_mr  gnd
 + rlgcmodel=ddd_667_minz     $ goto directory or below and u will find the file defined
 + l=cpu1_tl_mr

*********************************************************

* CPU Plated Through Hole (PTH)
x_cpu1_pth  cpu1_tl_diff1_mr cpu1_tl_diff2_mr  gnd
 +        cpu1_pth_diff1    cpu1_pth_diff2   gnd gnd      pth_3io

* CPU Socket
x_cpu1_socket   cpu1_pth_diff1  cpu1_pth_diff2
 +          cpu1_soc_diff1  cpu1_soc_diff2    gnd   zif_socket_couple

*********************************************************
* MB TraceX: CPU1 Pin Field
w_mb1_pf n=2
 + cpu1_soc_diff1  cpu1_soc_diff2   gnd
 + cpu1_pf_diff1  cpu1_pf_diff2   gnd
 + l = cpu1_pf_len
 + rlgcmodel=mb_minz
 + fgd = 0 includersimag=yes

***********************************************
* MB Trace1:
w_mb1 n=2
 + cpu1_pf_diff1 cpu1_pf_diff2  gnd
 + mbd_tl1_diff1 mbd_tl1_diff2  gnd
 + l = mb_tl1
 + rlgcmodel=mb_minz * Assumption is routed in top layer
 + fgd=0 includersimag=yes

***********************************************
* MB Trace_bend_1(Saad):
*** Assumption is differential line 2 get extra length due to bending
w_mb_bend_1 n=1
 + mbd_tl1_diff1 gnd
 + mbd_tlbend_1_diff1 gnd
+ l = mb_tl_bend
 + rlgcmodel=mb_minz_bend * Assumption is differential line 2 is bending
 + fgd=0 includersimag=yes

***********************************************
* MB Trace2:
```

```
w_mb2 n=2
 + mbd_tlbend_1_diff1  mbd_tl1_diff2  gnd
 + mbd_tl2_diff1 mbd_tl2_diff2   gnd
 + l = mb_tl2
 + rlgcmodel=mb_minz * Assumption is routed in top layer
 + fgd=0 includersimag=yes

**********************************************
* MB Trace_bend_2(Saad): *On diff2
w_mb_bend_2 n=1
 + mbd_tl2_diff1 gnd
 + mbd_tlbend_2_diff1 gnd
 + l = mb_tl_bend
 + rlgcmodel=mb_minz_bend
* ** Assumption is differential line 2 get extra length due to bending
 + fgd=0 includersimag=yes

**********************************************
* MB Trace3:
w_mb3 n=2
 + mbd_tlbend_2_diff1 mbd_tl2_diff2  gnd
 + mbd_tl3_diff1 mbd_tl3_diff2   gnd
 + l = mb_tl3
 + rlgcmodel=mb_minz * Assumption is routed in top layer
 + fgd=0 includersimag=yes
**********************************************
* MB Trace_bend_3(Saad): *On diff2
** Assumption is differential line 2 get extra length due to bending

w_mb_bend_3 n=1
 + mbd_tl3_diff2 gnd
 + mbd_tlbend_3_diff2 gnd
 + l = mb_tl_bend
 + rlgcmodel=mb_minz_bend
 + fgd=0 includersimag=yes

**********************************************

* MB Trace4:
w_mb4 n=2
 + mbd_tl3_diff1 mbd_tlbend_3_diff2  gnd
 + mbd_tl4_diff1 mbd_tl4_diff2   gnd
 + l = mb_tl4
 + rlgcmodel=mb_minz * Assumption is routed in top layer
 + fgd=0 includersimag=yes
**********************************************
*(changed on 22nov07)
* MB Trace_bend_4(Saad): *On diff2
w_mb_bend_4 n=1
 + mbd_tl4_diff2 gnd
 + mbd_tlbend_4_diff2 gnd
+ l = mb_tl_bend
 + rlgcmodel=mb_minz_bend * Assumption is differential line 1 is bending
 + fgd=0 includersimag=yes


**********************************************
* MB Trace5:
w_mb5 n=2
 + mbd_tl4_diff1 mbd_tlbend_4_diff2  gnd
 + mbd_tl5_diff1 mbd_tl5_diff2   gnd
 + l = mb_tl5
```

```
 + rlgcmodel=mb_minz * Assumption is routed in top layer
 + fgd=0 includersimag=yes
**********************************************
*(changed on 22nov07)
* MB Trace_bend_5(Saad): *On diff1
w_mb_bend_5 n=1
 + mbd_tl5_diff1 gnd
+ mbd_tlbend_5_diff1 gnd
 + l = mb_tl_bend
 + rlgcmodel=mb_minz_bend * Assumption is differential line 1 is bending
 + fgd=0 includersimag=yes

**********************************************

* MB Trace6:
w_mb6 n=2
 + mbd_tlbend_5_diff1   mbd_tl5_diff2  gnd
 + mbd_tl6_diff1       mbd_tl6_diff2   gnd
 + l = mb_tl6
 + rlgcmodel=mb_minz * Assumption is routed in top layer
 + fgd=0 includersimag=yes

**********************************************
* capacitance for via

c1_trace1  mbd_tl6_diff1    gnd   via_capacitane_1
c1_trace2 mbd_tl6_diff2    gnd   via_capacitane_2

**********************************************
* MB Trace for VIA trace1 :
w_mb6_VIA_trace1 n=1
 + mbd_tl6_diff1    gnd
 + mbd_tl6_VIA_diff1  gnd
 + l = Extra_Length_trace_1
 + rlgcmodel=mb_minz_bend * Assumption is routed in top layer
 + fgd=0 includersimag=yes

**********************************************

* MB Trace for VIA_trace2  :
w_mb6_VIA_trace2 n=1
 + mbd_tl6_diff2    gnd
 + mbd_tl6_VIA_diff2  gnd
 + l = Extra_Length_trace_2
 + rlgcmodel=mb_minz_bend * Assumption is routed in top layer
 + fgd=0 includersimag=yes

**********************************************************************************************
* capacitance for via

c2_trace1 mbd_tl6_VIA_diff1  gnd  via_capacitane_1
c2_trace2 mbd_tl6_VIA_diff2  gnd  via_capacitane_2

**********************************************************************************************
* MB Trace7:
w_mb7 n=2
 +  mbd_tl6_VIA_diff1  mbd_tl6_VIA_diff2   gnd
 + mbd_tl7_diff1 mbd_tl7_diff2   gnd
 + l = mb_tl7
 + rlgcmodel=mb_minz * Assumption is routed in top layer
 + fgd=0 includersimag=yes
```

```
**************************************************
* MB Trace extra bend  compensation:
w_mb_extra_bend n=2
 +  mbd_tl7_diff2  mbd_tl_extra_bend_diff2 gnd
+  mbd_tl_bend2_diff2  mbd_tl_bend2_diff2 gnd
 + l = mb_tl_bend
 + rlgcmodel=mb_minz * Assumption is routed in top layer
 + fgd=0 includersimag=yes

**************************************************
* MB Trace8:
w_mb8 n=2
 + mbd_tl7_diff1  mbd_tl_extra_bend_diff2  gnd
 + mbd_tl8_diff1        mbd_tl8_diff2   gnd
 + l = mb_tl8
 + rlgcmodel=mb_minz * Assumption is routed in top layer
 + fgd=0 includersimag=yes

**************************************************
* MB Trace_bend_6(Saad): *On diff1
w_mb_bend_6 n=1
 + mbd_tl8_diff1 gnd                  **mbd_tl1_diff2  gnd
 + mbd_tlbend_8_diff1 gnd                        ****mbd_tl2_diff2  gnd
 + l = mb_tl_bend
 + rlgcmodel=mb_minz_bend * Assumption is differential line 1 is bending
 + fgd=0 includersimag=yes

**************************************************
* MB Trace9:
w_mb9 n=2
 + mbd_tlbend_8_diff1 mbd_tl8_diff2  gnd
 + mbd_tl9_diff1 mbd_tl9_diff2   gnd
 + l = mb_tl9
 + rlgcmodel=mb_minz * Assumption is routed in top layer
 + fgd=0 includersimag=yes

**************************************************
*MB TraceY: CPU2 Pin Field
w_mb2_pf n=2
 + mbd_tl9_diff1 mbd_tl9_diff2  gnd
 + cpu2_pf_diff1  cpu2_pf_diff2    gnd
 + l = cpu2_pf_len
 + rlgcmodel=mb_minz
 + fgd = 0 includersimag=yes


**********************************************************
* CPU2 Socket
x_cpu2_socket
 + cpu2_pf_diff1  cpu2_pf_diff2
 + cpu2_soc_diff1  cpu2_soc_diff2  gnd zif_socket_couple

**********************************************************
* CPU2 Plated Through Hole (PTH)
x_cpu2_pth
 + cpu2_soc_diff1 cpu2_soc_diff2 gnd
 + cpu2_pth_diff1 cpu2_pth_diff2 gnd gnd pth_3io

**********************************************************
* CPU2 Package Transmission Line
w_cpu2_tl_mr N=2
 + cpu2_pth_diff1 cpu2_pth_diff2 gnd
```

```
+ cpu2_pad_diff1 cpu2_pad_diff2 gnd
+ rlgcmodel=ddd_667_minz    $ goto dir and u will find the file defined
+ l=cpu1_tl_mr

**************************************************
* CPU2
x_cpu2_breakout_mr
 + cpu2_pad_diff1 cpu2_pad_diff2 gnd
 + cpu2_bo_diff1  cpu2_bo_diff2  gnd
 + gnd breakout_w_rect

********* cpu  load ********************************
c_cpu2_load1 cpu2_bo_diff1 gnd cpu_ccomp
c_cpu2_load2 cpu2_bo_diff2 gnd cpu_ccomp
**c_cpu2_load3 cpu2_bo_agr2 gnd cpu_ccomp

*--------------------------------------------------------------------------
*     .Probe Statements
*--------------------------------------------------------------------------
*-- Driver Pad Probe
.probe tran v(cpu1_pad_diff1)
.probe tran v(cpu1_pad_diff2)
.probe tran v(cpu2_bo_diff1)
.probe tran v(cpu2_bo_diff2) * Probe point
.print tran par('v(cpu2_bo_diff1)-v(cpu2_bo_diff2)') * print point

.Alter $ to change the length of traces beside via for Type2
.param Extr_Length_trace_1 =          'mb_tl_str_via_type2a' $ m. $Via length type 2
.param Extr_Length_trace_2 =          'mb_tl_str_via_type2b' $ m. $Via length type 2


.param mb_tl_bend          ='mb_tl_bend+(mb_tl_str_via_type2a-mb_tl_str_via_type2b)/2' $ m.
*Extra length is added with the compensation for extra bending for the mismatch in length $among the
traces beside via for Type2 Via length type 2


* to change the capacitance of traces beside via for Type2
.param via_capacitane_1 = 'type2a_via_capacitane_2a'          $ in Farad
 .param via_capacitane_2 = 'type2b_via_capacitane_2b'

.end
```

8.2. Include file ddd_667_MinZ.sp

*** this is the include file which carries package configuration (RLGC model)**

```
* BEGIN ANSOFT HEADER
* node 1 Trace1_A
* node 2 Trace2_A
* node 3 Ground_A
* node 4 Trace1_B
* node 5 Trace2_B
* node 6 Ground_B
*   Format: HSPICE W Element
*   Length: 1 meters
*   T_Rise: 1E-009 seconds
*    Model: Distributed Lossy Transmission Line
*      Cap: f:/users/rtan1/3linemodel/tpsfrmmatlab/usr55_3io_ddd_667.pjt/es.pjt
*        + /setup2.cap
*      Imp: f:/users/rtan1/3linemodel/tpsfrmmatlab/usr55_3io_ddd_667.pjt/ed.pjt
*        + /setup2.prz
*    Notes: 3-Line couple I/O data signals (ddd) 667MHz Max Z
* END ANSOFT HEADER
```

```
* Note: some off-diagonal matrix elements may be zeroed
* because HSPICE requires this.

*.SUBCKT us_ddd_667_minz 1 2 3 4 5 6
.model ddd_667_minz W modeltype=RLGC N=2
+ Lo=
+  2.953370942477167e-007
+   1.73348309173483e-008
+  2.953160340247037e-007
+ Co=
+  1.373877485584915e-010
+  -6.563917688215942e-012
+  1.377933182491636e-010

+ Ro=
+       40.37964172903712
+       1.121076233183803
+       40.37964172903352

+ Rs=
+     0.00543485272943613
+   0.0004350653121069269
+     0.00546136874995092

* end of file
```


8.3. Include file mb_minz.rlc

```
* this is the include file which carries mother board stripline configuration (RLGC model)
* Note: some off-diagonal matrix elements may be zeroed
* because HSPICE requires this.

.MODEL mb_minz W MODELTYPE=RLGC, N=2
+ Lo = 2.569762e-007
+     3.510568e-008 2.550276e-007

+ Co = 1.443481e-010
+     -1.577618e-011 1.471304e-010

+ Ro = 3.437408e+000
+     0.000000e+000 3.437408e+000

+ Go = 0.000000e+000
+     0.000000e+000 0.000000e+000

+ Rs = 1.564327e-003
+     3.093692e-004 1.555904e-003

+ Gd = 1.511610e-011
+     -1.652078e-012 1.540746e-011

* end of file
```

8.4. Include file mb_minz_bend.rlc

*** this is the include file which carries mother board single transmission line *configuration (RLGC model). It doesn't have mutual capacitance and inductance.**

```
* Note: only self inductance, capacitance matrix elements are kept and *others
are zeroed
* because HSPICE requires this.

.MODEL mb_minz_bend W MODELTYPE=RLGC, N=1
+ Lo = 2.569762e-007
+ Co = 1.443481e-010
+ Ro = 3.437408e+000
+ Go = 0.000000e+000
+ Rs = 1.564327e-003
+ Gd = 1.511610e-011
* end of file
```

8.5. CODE to create Eye Diagram on MatLab

To prepare data in correct format for MatLab – Hspice simulations must perform the following modification for the data output.

Hspice creates data using print command. Use ".print" instead of ".probe".
Example - ".print tran par('v(cpu2_bo_diff1)-v(cpu2_bo_diff2)')" gives the difference of the two trace output in the .lis file.

".option ingold=1" command is used to print data points without unit. To prepare data in correct format for MatLab data should be unit less.

After simulation, a .lis file is created with the same name of the project .sp file. Then the extension of this .lis file needs to be change as .net.

On MatLab window, first import Data File such as "doubleldata3000type3withoutvia.**txt**"
Then write down the following command to create eye diagram.
Command:
Outline steps fort MatLab to prepare data for eye creation.

```
>>doubleldata3000type3withoutvia= doubleldata3000type3withoutvia ( :,2 )
// to create the two column matrix.
>>plot(doubleldata3000type3withoutvia)
>> doubleldata3000type3withoutvia1111=doubleldata3000type3withoutvia (400:1500)
// to omit some of the initial data points. There is some propagation delay and after some time
signal transmission becomes stabilized.
//Then the array becomes
doubleldata3000type3withoutvia1111 =
  -0.6479
  -0.6587
  -0.6688
  -0.6783
  -0.6873
  -0.6955
  -0.7026
        eyediagram(doubleldata3000type3withvia1111,50,50,20)
      // to plot the eye diagram this command is used.
```