An Investigation of the Performance of Low Doped **100-nm Thick p-type Polysilicon Nanowire Biosensor**

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Submitted to the

Department of Electrical and Electronic Engineering Faculty of Sciences and Engineering East West University

In Partial Fulfillment of the Requirements for the Degree of Bachelor of Science in Electrical and Electronic Engineering (B.Sc. in EEE)

Spring, 2016

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Abstract

We investigate the electrical characteristics of 100nm thick 10 μ m long p-type low doped Si nanowire's electrical behavior for biosensor operation. For positive drain voltage application nanowire shows non-linear diode like characteristics where for negative V_{DS} application it exhibits perfect transistor behavior on output characteristics for both positive or negative V_{DS} applications device exhibit sub threshold slope of 83.33mv/decade where shows that poly silicon nanowire is good candidate for bio sensing operation. However maximum sensitivity which can be achieved is limited to 750%. We find that positive V_{DS} application is somehow beneficiary which provides flexibility of wide range of liquid gated voltage depends on biomarker charge whereas negative V_{DS} application restrains liquid gated voltages. This study reveals applicable voltages ranges of 10 μ m long 100nm thick low doped p-type Si nanowire biosensors operation and maximum conductance change possible for detection of biomarkers.

Acknowledgements

First of all, we are grateful to Almighty Allah for granting us such an opportunity to work with this research.

We would like to express our sincere thanks and gratitude to our research supervisor Dr. Mohammad Mojammel Al Hakim, Chairperson and Associate professor, Department of Electrical and Electronic Engineering, East West University, Dhaka, Bangladesh for continuous support, motivation and guidance in the development of this research. It gives us a great impression to have had the opportunity to work with him throughout our research.

We would also like to thank all the faculty members of Department of Electrical and Electronic Engineering for their supports and untiring effort in the management of quality education and we would like to thank our parents for blessing and our friends, well-wishers who helped us in the completion of this research.

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ABSTRACT 2
ACKNOWLEDGEMENTS
AUTHORIZATION PAGE 4
CHAPTER 1. INTRODUCTION8
1.1 MOTIVATION AND OBJECTIVES
1.2 THESIS ORGANIZATION
CHAPTER 2. CARRIER TRANSPORT IN POLYSILICON NANOWIRES
2.1 ELECTRICAL PROPERTIES OF POLYSILICON FILMS
2.2 Seto's Carrier Trapping Theory 10
2.3 Carrier Trapping at Grain Boundaries 11
2.4 Carrier Transport in Polysilicon Films15
2.5 NUMERICAL SIMULATION OF POLYSILICON DEVICES
2.6 Modeling Deep Trap Emission and Absorption with Shockley-Read-Hall Statistics
2.7 Continuous Trap-State Density Distribution Model 21
CHAPTER 3 :METHODOLOGY24
3.1 DEVICE FEATURE AND SIMULATION PROFILE:
3.2 SIMULATION PROFILE
CHAPTER 4: RESULT AND DISCUSSION
CHAPTER 5: CONCLUSION40
REFERENCES

TABLE OF CONTENTS

LIST OF FIGURES

Figure 2.1: (a) The simplified model of the crystallite structure in the polysilicon film showing a single crystallite separated from the two adjoining crystallites by grain boundaries (b) The charge distribution in the structure, showing the negatively charged GB and the surrounding positively charged depletion layer (c) Energy band structure with potential barriers forming at the grain boundaries.

Figure 2.2: (a) As the doping density is increased, the trap states at the grain boundary become filled, increasing the barrier height. When the doping density is increased beyond the critical value N^* , the free carriers reduce the depletion width and the barrier height recedes, (b) barrier height increases linearly as a function of N until reaching the critical value, beyond which it decreases rapidly as a function of 1/NN.

Figure 2.3: An illustration of the possible capture and emission processes from trap states deep in the energy band gap for (a) donor-like traps and (b) acceptor-like traps.

Figure 2.4: An illustration of a possible (a) acceptor-like and (b) donor-like distribution of trap states across the energy band gap and how they relate to the model parameters.

Figure 3.1: Schematic of the simulated p-type silicon nanowire.

Figure 3.2: The distribution of acceptor and donor-like trap states across forbidden energy gap.

Figure 3.3: The trap energy level for acceptor and donor-like traps in reference of conduction and valance band edges.

Figure 3.4: Cross-sectional view of p-type nanowire showing the mesh density used in this simulation.

Fig 4.1 I_{DS} vs. V_{GS} characteristics plot of Silicon nanowire.

Fig 4.2 I_{DS} vs. V_{DS} characteristics plot with positive drain voltage when gate voltages are negative.

Fig 4.3 I_{DS} vs. V_{DS} characteristics plot with positive drain voltage when gate voltages are positive.

Fig 4.4 I_{DS} vs. V_{GS} characteristics plot with positive drain voltage.

Fig 4.5 I_{DS} vs. V_{DS} characteristics plot with negative drain voltage when gate voltage is negative (Id in reverse order).

Fig 4.6 I_D vs. V_{GS} characteristics plot with negative drain voltage (Id in reverse order).

Fig 4.7 Sensitivity of polysilicon p-type NWs with different positive drain voltages.

Fig 4.8 Sensitivity polysilicon p-type NWs plot with different negative drain voltages.

LIST OF TABLES

Table 3.1: Default parameters for equation 3.1

 Table 3.2: Default parameters of Slotbooms Bandgap Narrowing Model for equation 3.3

 Table 3.3: Default mobility model values for polysilicon

 Table 3.4: Default Parameters for Equations 3.9 to 3.14

 Table 4.1: Device parameters and trap states distribution parameters used for simulation

CHAPTER 1. INTRODUCTION

1.1 Motivation and Objectives

Over the last decades, silicon nanowires are emerging as important candidates for biochemical sensors [1-4]. There are many reasons why silicon nanowires are of interest, including high surface-to-volume ratio, high sensitivity and real-time, label free detection without expensive optical components [5]. Although nanowire field effect transistors are used to sense ions, proteins, DNA and viruses, outstanding issues remain, most notably the cost and practicality of fabrication. Therefore, the development of a very low-cost and simple fabrication route suitable for mass manufacture of disposable nanowire sensors would accelerate their uptake as Point of Care (PoC) devices.

There are two major approaches for fabricating nanowire biosensors, namely top-down and bottom-up approaches usually employ metal-catalytic growth [6], which is simple and cheap. However, control of nanowire position and diameter is difficult and electrical contact formation is problematic, making it difficult to construct multiplexed nanowire arrays. Topdown approaches overcome these shortcomings and several groups are used nano-patterning techniques such as deep-UV [7] lithography and electron beam lithography [8-9] to fabricate silicon nanowires on silicon-on-insulator (SOI) substrate. This has the advantage of CMOS compatibility, but a serious disadvantage is the high cost associated with these advanced lithography techniques and expensive SOI wafers. Wet etch of SOI wafers has also been researched as means of creating triangular nanowires without the need for advanced lithography [10-11], but as wet etching is not favored by industry, this approach does not provide a clear route to manufacturing. Recently a low cost, top-down approach to nanowire fabrication has been reported that uses thin film technology and spacer etch technique [12-14]. This approach is particularly attractive because it produces polysilicon nanowires with nanoscale dimensions using mature lithography in combination with standard deposition and spacer techniques that are widely available in industry.

Although poly silicon nanowire biosensors have been successfully demonstrated sensing of protein biomarkers, the sensitivity of polysilicon nanowire as biosensors always remain questionable due to polysilicon grain boundary defects. There is no available in literature rigorously comparing poly silicon nanowire biosensors technology with single crystal silicon nanowire, its sensitivity and technology stand point. Towards, this goal this

thesis performs a preliminary study of a 100nm thick poly silicon nanowire. Sensor performance by investigating its electrical characteristics.

1.2 Thesis Organization

Chapter 1 Motivation and objective of this research.

Chapter 2 provides the necessary background theory to model polysilicon devices by describing the carrier trapping mechanism at grain boundaries. Carrier trapping leads to the formation of the potential barriers that are limiting mechanism in carrier transport through polysilicon films. The model derived assumes a mono-energetic trap level, however this is not realistic so we finish by dis-cussing the inclusion of a continuum of trap states across the energy band gap. Therefore, we go on to look at the implementation of carrier emission/absorption process from deep trap sates in our numerical simulation tools.

Chapter 3 describes the simulation methodology, device structure and the required models for device simulation.

Chapter 4 describes the electrical characteristics of a low doped 100nm thick poly silicon nanowire and extracts its sensitivity to gate voltage to perform a feasibility study of polysilicon nanowire biosensors.

Chapter 5 Summary of this thesis work.

CHAPTER 2. CARRIER TRANSPORT IN POLYSILICON NANOWIRES

2.1 Electrical Properties of Polysilicon Films

A polysilicon film is composed of small crystallites joined together by grain boundaries, where the angle between the adjoining crystallites is often large. Inside each crystallite the atoms are arranged in a periodic manner hence behaves like a small single crystal and the grain boundary itself is a complex structure, usually consisting of a few atomic layers of disordered atoms and a large number of defects due to incomplete atomic bonding. Several models have been proposed to explain the electrical behavior of polysilicon films. The most well-known being the competing theories of carrier trapping and segregation. In the segregation theory, it was proposed that dopant atoms can segregate to the grain boundary because of their lower energy in the disordered GB region, and therefore do not contribute to the conduction process. This would mean that the number of carriers free for conduction would be significantly less than in a, similarly doped, single crystal silicon film. The main failing of segregation theory is that it does not explain the temperature dependence of resistivity in moderately doped polysilicon films, which is thermally activated and displays a negative temperature coefficient. The competing carrier trapping theory was first proposed by Kamins[15] and then later developed into a comprehensive theory of carrier transport by Seto [16]. It has successfully explained most of the electrical properties of polysilicon for the special case where the depletion region extends throughout the entire crystallite. Baccarani et al [17]. published a series of results that Seto's approximation of a monovalent trap energy level was valid. Throughout this work Seto's theory is used as the conceptual basis for explaining conduction phenomena in polysilicon.

2.2 Seto's Carrier Trapping Theory

In this theory it is known that there are a large number of defects due to incomplete atomic bonding at the grain boundary. These defects in the grain boundary are locations where it is possible for carriers to become trapped and immobilized. This results in the traps themselves, and therefore the grain boundary becoming electrically charged. To satisfy charge neutrality an oppositely charged depletion layer of finite width forms on either side of the GB. As a consequence, the energy bands are bent at the GB creating a notch or barrier, which acts to impede carrier transport through the film. The trapping of carriers would therefore, decrease both the carrier concentration and the mobility of the material.

2.3 Carrier Trapping at Grain Boundaries

In Seto's model a number of assumptions were made to simplify his analysis.

- The polysilicon film is composed of identical crystallites with a grain size of L(cm). In a real polysilicon film there can be large variations in the size and orientation of the grains.
- There is only one type of impurity atom present and they are full ionized and uniformly distributed with a concentration of N(cm⁻³). Minority carriers and their associated traps are not considered in the analysis.
- 3. Inside the crystallites the single-crystal band structure of silicon is applicable. Therefore, he is assuming that the structure inside each crystallite is perfect and defect free, which is not necessarily true.
- 4. The grain boundary is of negligible thickness compared to the grain size L with $N_T(cm^2)$ of traps located at trap energy E_t with respect to the intrinsic Fermi level. In a real polysilicon film the traps energies are distributed across the energy gap of the band structure. Although Baccarani et al. [17] concluded that a mono-energetic approximation of the trap states was sufficient to successfully model the behavior of a polysilicon film.

The resulting energy band structure and charge distribution for a polysilicon film with two grain boundaries is shown in fig. 2.1. All the mobile carriers in the region of $(\frac{1}{2}L-1)$ cm from the grain boundary are trapped by the trapping states resulting in a depletion of a potential barrier in the band structure. In this analysis is considered sufficient to treat the problem in one dimension. Under this assumption Poisson's equation becomes

Where ϵ is the dielectric permittivity of polysilicon Integrating (2.1) twice and applying the boundary conditions that V(x) is continuous and $\frac{dv}{dx} = 0$ when x = 1 gives us

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Where V_{vo} is the potential of the valence band edge at the center of the crystallite. Throughout the calculation the intrinsic Fermi level is taken to be at zero energy and energy is positive towards the valence band.

There are two cases that we need to consider relating to the doping concentration.

1.
$$N < \frac{N_T}{L}$$

2. $N > \frac{N_T}{L}$

Where we define a critical doping concentration, $N^* = \frac{N_T}{L}$

Below critical doping concentration, $N < \frac{N_T}{L}$

Considering first of all the case when, $N < \frac{N_T}{L}$. This condition implies that the crystallite is completely depleted of carriers and the traps are partially filled so that l = 0 and (2.2) becomes

Above the critical doping concentration, $N > \frac{N_T}{L}$

In Seto's model the energy of the grain boundary traps is assumed to be deep enough, that they are completely filled, when the dopant concentration exceeds the critical value, $N^* = \frac{N_T}{L}$. As we increase the dopant concentration above this value, the number of trapped carriers remains constant at the value N_T , and the added carriers act to form neutral regions within the grains, as seen in fig. 2.2. This reduces the depletion region width, but to satisfy charge neutrality the value of charge in the depletion regions width, but to satisfy charge neutrality the value of charge in the depletion region remains constant, albeit in a smaller area. This result in the potential barrier height receding. The width of the depletion region decreases according to the relation

$$x_d = \frac{N_T}{2N} \qquad (2.5)$$

Therefore, the barrier height when $N > \frac{N_T}{L}$ is found to be

(a) Crystal

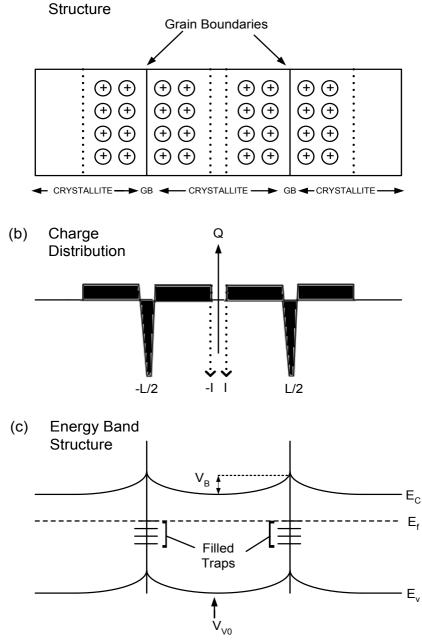


Figure 2.1: (a) The simplified model of the crystallite structure in the polysilicon film showing a single crystallite separated from the two adjoining crystallites by grain boundaries (b) The charge distribution in the structure, showing the negatively charged GB and the surrounding positively charged depletion layer (c) Energy band structure with potential barriers forming at the grain boundaries.

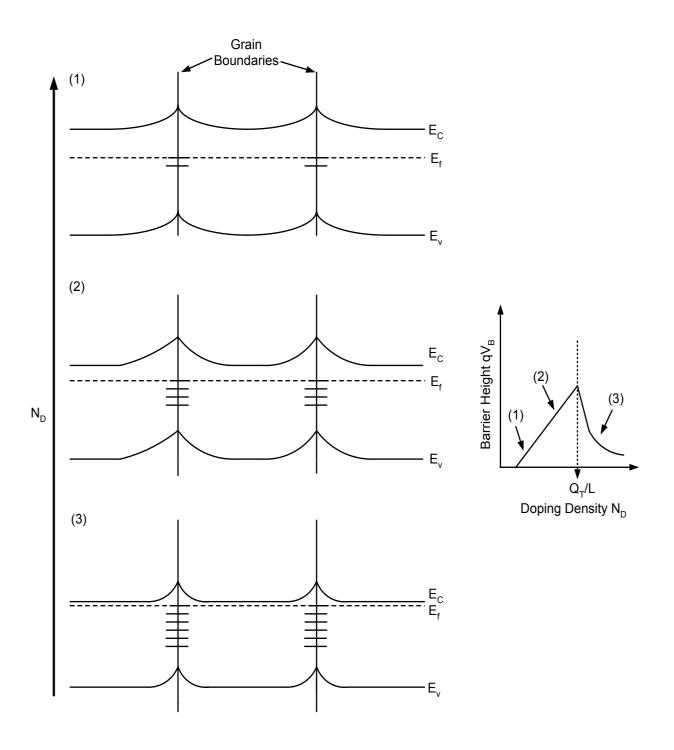


Figure 2.2:(a) As the doping density is increased, the trap states at the grain boundary become filled, increasing the barrier height. When the doping density is increased beyond the critical value N^* , the free carriers reduce the depletion width and the barrier height recedes, (b) barrier height increases linearly as a function of N until reaching the critical value, beyond which it decreases rapidly as a function of $\frac{1}{N}$.

Thus, as shown in Fig. 2.2 as the dopant concentration is increased in the film, firstly the potential barrier increase as a function of N, and then above the critical doping concentration N^* it decreases rapidly as a function of $\frac{1}{N}$.

2.4 Carrier Transport in Polysilicon Films

It is assumed that carrier transport, in moderately doped polysilicon films, is dominated by thermionic transport over the barriers. The reasoning being, that even at moderate doping concentration of found around 1×10^{17} cm⁻³ the barrier width is still tens of nanometers wide. Tunneling is not significant for barriers of this width. At high doping concentrations the barrier is narrow enough that tunneling may contribute to the current flow, however the barrier height at these concentrations may be low enough for it to be no longer a dominant factor in inhibiting carrier transport.

The thermionic-emission current density] can be written as

$$J = qnv_c exp\left[-\frac{q}{kT}(V_B - V)\right]\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots(2.7)$$

where *n* is the free-carrier density, $v_c = \sqrt{\frac{kT}{2\pi m^*}}$ is the collection velocity, V_B is the barrier height with no applied bias, and *V* is the applied bias across the depletion region.

Under an applied bias the current flow is one direction increases while carrier transport in the other direction decreases. Therefore, we must consider current flow in both the forward and reverse directions. The net current density given by; $J = J_F - J_R$. With $V \approx \frac{1}{2}V_G$, where V_G is the bias across one grain boundary.

The net current density under applied bias then becomes

$$J = qnv_c exp\left[-\frac{qV_B}{kT}\right] \left[exp\left(\frac{qV_G}{2kT}\right) - exp\left(-\frac{qV_G}{2kT}\right)\right] \cdots \cdots \cdots \cdots \cdots \cdots (2.10)$$

We can obtain a linear relationship between current and applied voltage if we make the following simplification for low applied voltages

Therefore

We can now obtain an expression for the conduction, $\sigma = \frac{J}{\epsilon} = \frac{JL}{v_G}$

Thus condition in polysilicon is an activated process with activation energy of approximately qV_B , which depends on the dopant concentration and the grain size. Many analytical models of polysilicon nanowire operation in the subthreshold and turn-on regions have been developed based on Seto's theory [18-22]. So far we have developed an analytical model that is valid in one dimension. However, in short channel field effect transistors a two dimensional analysis is necessary to adequately described the device operation. Therefore, we need to use 2D numerical device simulation to realistically study the effect of the GB, in short channel polysilicon nanowires.

2.5 Numerical Simulation of Polysilicon Devices

The trend in the semiconductor industry towards MOSFETs of ever decreasing gate lengths has increase the demand for accurate numerical device simulation technologies. As devices enter the sub-micron regime, complex 2D effects begin to determine the device behavior in the subthreshold regime, and therefore 2D device simulation is needed to provide insight and predictive analysis. The classical Drift-Diffusion model (DD) has been extensively studied for almost forty years, since Gummel et al. reported on the one-dimensional numerical simulation of a silicon bipolar transistor [23]. Even as the MOSFET enters the decananometer regime, where ballistic and quantum mechanical effects can play significant roles in carrier transport, DD modeling is still one of the most practical and powerful tools in FET design. With some modifications (such as the inclusion of momentum and energy balance equations) it can still provide reasonable accuracy and importantly great computational

efficiency, compared to more elaborate techniques, such as practical based ensemble Monte-Carlo simulations.

In our simulation studies of the device, we use commercial simulator ATLAS [24] from SILVACO international. ATLAS uses the basic device modeling equation for DD modeling. The basic semiconductor equation begins with Poisson's equation which describes the relationship between the electrostatic potential ψ to the space charge density ρ

Where, ε is the local permittivity.

The carrier continuity equation for both electrons and holes are defined in terms of the current densities $\vec{J_n}$, $\vec{J_p}$ and the generation and recombination rates for electrons and holes (G_n , G_p and R_n , R_p) respectively.

The electron and hole current densities $\vec{j_n}$ and $\vec{j_p}$ are then expressed in terms of their respective quasi-Fermi potentials ϕ_n and ϕ_p .

Where μ_n and μ_p are the electron and hole mobilities respectively.

The carrier concentration is expressed in the following quasi-Boltzmann form in terms of both quasi-fermi potentials ϕ_n and ϕ_p and the intrinsic potential ψ

$$n = n_i exp[\frac{\psi - \phi_n}{V_T}] \cdots (2.20)$$
$$p = n_i exp[\frac{\psi - \phi_p}{V_T}] \cdots (2.21)$$

Where, V_T is the thermal voltage $(= k_B T/q)$ and n_i is the intrinsic carrier concentration.

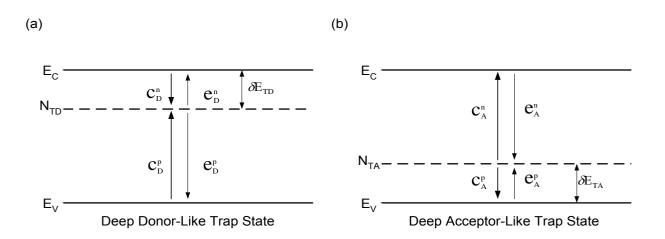


Figure 2.3: An illustration of the possible capture and emission processes from trap states deep in the energy band gap for (a) donor-like traps and (b) acceptor-like traps

2.6 Modeling Deep Trap Emission and Absorption with Shockley-Read-Hall Statistics

We now include the carrier trapping mechanisms, via the deep trap states at the grain boundary. The model used was originally developed for carrier emission-absorption processes from the donors and acceptors in heterojunction structures [25, 26]. However, it is equally applicable to silicon devices. By using the derived expressions, we then modify the basic device transport equations accordingly.

We start by defining two types of trap that exchange charge with the conduction and valance bands through the emission and recombination of electrons. At the grain boundary these would exist in the forbidden energy gap as a result of incomplete or dangling bonds in the semiconductor lattice.

Firstly, we define donor-like traps as positively charged when empty and neutral when filled by electron. Secondly we define acceptor-like traps to be negative when filled by an electron but otherwise neutral. Therefore, traps above the Fermi-level are acceptor-like and those below are donor-like. This is illustrated along with the possible capture and emission processes in fig 2.3

The energies of donor-like (E_{TD}) and acceptor-like (E_{TA}) traps are expressed as

The time evolution of the density of carriers at the deep levels is given by the following rate equations;

$$\frac{\partial}{\partial t}(N_{TD} - N_{TD}^{+}) = C_D^n N_{TD}^{+} n - e_D^n (N_{TD} - N_{TD}^{+}) - C_D^p (N_{TD} - N_{TD}^{+}) p - e_D^p N_{TD}^{+} \cdots \cdots (2.24)$$
$$\frac{\partial}{\partial t}(N_{TA} - N_{TA}^{-}) = C_A^p N_{TA}^{-} p - e_A^p (N_{TA} - N_{TA}^{-}) - C_A^n (N_{TA} - N_{TA}^{-}) n - e_A^n N_{TA}^{-} \cdots \cdots (2.25)$$

Where the carrier emission rates $e_D^n, e_D^p, e_A^n, e_A^p$ are related to the carrier capture rates $C_D^n, C_D^p, C_A^n, C_A^p$ by the relations;

$e_D^n = C_D^n n_1^D \cdots \cdots$
$e_D^p = C_D^p p_1^D \cdots \cdots$
$e_A^n = C_A^n n_1^A \cdots \cdots$
$e_A^p = C_A^p p_1^A \cdots \cdots$

Where n_1^D , p_1^D , n_1^A , p_1^A are given by the following;

$$n_{1}^{D} = nig_{D}exp\left[\frac{\Delta E_{TD}}{k_{B}T/q}\right] \cdots (2.30)$$

$$p_{1}^{D} = nig_{D}exp\left[\frac{-\Delta E_{TD}}{k_{B}T/q}\right] \cdots (2.31)$$

$$n_{1}^{A} = nig_{A}exp\left[\frac{\Delta E_{TA}}{k_{B}T/q}\right] \cdots (2.32)$$

$$p_{1}^{A} = nig_{A}exp\left[\frac{-\Delta E_{TA}}{k_{B}T/q}\right] \cdots (2.33)$$

In Eq. 2.30-2.33, g_D and g_A are the degeneracies of the deep donor-like and acceptor-like trap states. A steady state-solution for the concentration of trapped charge at the GB can found from the Eq. 2.24 and 2.25. This gives us;

$$N_{TD}^{+} = \frac{n_{1}^{D} / C_{D}^{p} + p / C_{D}^{n}}{(n + n_{1}^{D}) / C_{D}^{p} + (p + p_{1}^{D}) / C_{D}^{n}} N_{TD} \cdots (2.34)$$
$$N_{TA}^{-} = \frac{n_{1}^{A} / C_{A}^{p} + p / C_{A}^{n}}{(n + n_{1}^{A}) / C_{A}^{p} + (p + p_{1}^{A}) / C_{A}^{n}} N_{TA} \cdots (2.35)$$

The additional charge at the grain boundary alters the electrostatic potential by appearing as additional charge terms on the right hand side of Poisson's equation. So Eq. 2.15 then becomes;

Where, N_D^+ and N_A^- are the concentrations of ionized shallow donors and acceptors.

In addition, there is induced electron-hole recombination, and therefore there is a change in the current distribution through an additional generation/recombination terms on the right hand side of Eq. 2.16 and 2.17. This gives us the following expressions;

$$q \frac{\partial n}{\partial t} = \nabla . \vec{J_n} + G + R + C_D^n N_{TD}^+ n - e_D^n (N_{TD} - N_{TD}^+) - C_A^n (N_{TA} - N_{TA}^-) n - e_A^n N_{TA}^- \cdots (2.37)$$
$$q \frac{\partial p}{\partial t} = \nabla . \vec{J_p} + G + R - C_A^p (N_{TD} - N_{TD}^+) p - e_A^p N_{TD}^+ - C_A^p N_{TA}^- n - e_A^p (N_{TA} - N_{TA}^-) \cdots (2.38)$$

Where, G and R are the conventional semiconductor generation and recombination terms respectively. If we solve for the steady state (i.e. $\frac{\partial n}{\partial t} = 0$ and $\frac{\partial p}{\partial t} = 0$) then the Eq. 2.37 and 2.38 reduce to the following current continuity equations;

Where, R_{TD} and R_{TA} are the recombination rates through the donor-like and acceptor-like trap states and are given by;

$$R_{TD} = \frac{np - n_1^D p_1^D}{(n + n_1^D) / C_D^p + (p + p_1^D) / C_D^n} N_{DD} \cdots \cdots \cdots (2.41)$$
$$R_{TA} = \frac{np - n_1^A p_1^A}{(n + n_1^A) / C_A^p + (p + p_1^A) / C_A^n} N_{DA} \cdots \cdots (2.42)$$

The expression given by Eq. 2.36, 2.39 and 2.40 are discretized onto a two-dimensional finite difference mesh lattice and then numerically solved in an iterative way using the standard Gummel's scheme [25-28].

2.7 Continuous Trap-State Density Distribution Model

So far we have assumed that the acceptor-like and donor-like trap states are mono-energetic; that is, they exist at only one energy level in the forbidden gap.

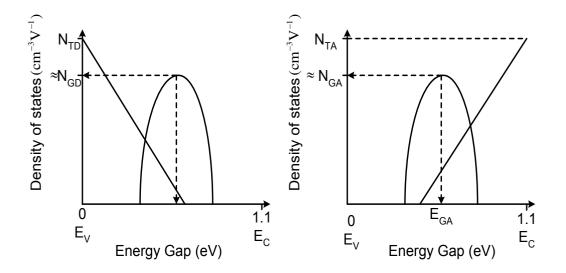


Figure 2.4: An illustration of a possible (a) acceptor-like and (b) donor-like distribution of trap states across the energy band gap and how they relate to the model parameters.

For a more accurate simulation, a continuum of trap states distributed across the energy band gap can be defined, using the commercial device simulator ATLAS. To do this we again modify the space charge term Q_T representing trapped charge. This is given by

$$-p = q(p - n + N_D^+ - N_A^-) + Q_T \cdots \cdots \cdots \cdots \cdots \cdots (2.43)$$
$$Q_T = q(p_T - n_T) \cdots \cdots \cdots \cdots \cdots \cdots \cdots (2.44)$$

Where, N_D^+ and N_A^- are the ionized donor and acceptor concentrations respectively and p_T and n_T are the trapped hole and electron concentrations respectively.

Again we assume that the trap states consist of both donor-like and acceptor-like states, distributed across the forbidden energy gap. We can write the total density of states as

$$g(E) = g_D(E) + g_A(E) \cdots (2.45)$$

Where, $g_D(E)$ is the total density of donor-like trap states and $g_A(E)$ is the total density of acceptor-like trap states. Attempts to experimentally measure the continuum of trap states at the grain boundary in Polysilicon films, suggest that both, donor-like and acceptor-like states, consist of two components. Firstly, an exponential tail distribution which intercepts the

adjacent energy band at its maximum value and decays rapidly toward the center $(g_{TA}(E))$ for acceptor and $g_{TD}(E)$ for donors). Secondly a Gaussian distribution of traps located deep in the energy gap $(g_{GA}(E))$ for acceptors and g_{GD} for donors). These terms are expressed as;

$$g_{TA}(E) = N_{TA}exp\left[\frac{E-E_{C}}{W_{TA}}\right] \cdots (2.46)$$

$$g_{TD}(E) = N_{TD}exp\left[\frac{E-E_{C}}{W_{TD}}\right] \cdots (2.47)$$

$$g_{GA}(E) = N_{GA}exp\left[-\left[\frac{E_{GA}-E}{W_{GA}}\right]^{2}\right] \cdots (2.48)$$

$$g_{GD}(E) = N_{GD}exp\left[-\left[\frac{E_{GD}-E}{W_{GD}}\right]^{2}\right] \cdots (2.49)$$

Where, N_{TA} and N_{TD} are the trap state densities at the point of intercept with the conduction band (acceptor-like) and valence band (donor-like) respectively and W_{TA} , W_{TD} are the characteristic decay energies, defining how rapidly the distribution decays towards the center of the band gap. For the Gaussian type states; N_{GA} and N_{GD} are the total density of trap states, W_{GA} and W_{GD} are the characteristic decay energies defining the spread of the Gaussian and finally, E_{GA} and E_{GD} are the position of the Gaussian peaks in the energy band gap. All quantities are for acceptor-like and donor-like trap respectively as denoted in the subscript. For clarification, the role of these quantities by the example distribution shown in Fig. 2.4

To calculate the trapped charge, we perform a numerical integration of the product of the trap density and its occupation probability over the forbidden energy gap. This gives

$$n_{T} = \int_{E_{V}}^{E_{C}} g_{A}(E) f_{A}(E, n, p) dE \dots (2.50)$$
$$p_{T} = \int_{E_{V}}^{E_{C}} g_{D}(E) f_{D}(E, n, p) dE \dots (2.51)$$

for trapped electrons and hole respectively, where f_A and f_D are the occupation probability for acceptor-like and donor-like traps.

If we them assume that the capture cross section for Gaussian and tail states are equal, then the occupation probabilities are then given by

Where, σ_{ae} , σ_{ah} and σ_{de} , σ_{dh} are the electron and hole capture cross sections for acceptor-like and donor-like traps respectively. The effective electron and hole concentrations, n_t and p_t are defined as

$$p_t = n_i exp \left[\frac{E_i - E}{kT} \right] \cdots \cdots \cdots (2.54)$$
$$n_t = n_i exp \left[\frac{E - E_i}{kT} \right] \cdots \cdots \cdots (2.55)$$

Where, n_i , is the intrinsic carrier concentration, E is the trap energy level, E_i is the intrinsic fermi level and T is the lattice temperature.

The Sockley-Read-Hall recombination/generation rate [27-29] per unit time is modified to include the multiple trap levels and is given by

Summary

In summary, we have derived an analytical model of carrier trapping at the grain boundary based on the pioneering work by Seto's Carrier Trapping Theory

This model predicts that the formation of a potential barrier at the GB where the barrier height is a function of doping density. The barrier height increases linearly until it reaches a critical doping density at which point any further increase in doping causes the barrier height to rapidly decrease.

To incorporate these effects into 2D simulation we show that a carrier trap model, based on the deep donor and acceptor states, can be used to model GB traps. The carrier and the emission processes are modeled using Shockley-Read-Hall statistics. We also commercial simulator ATLAS, extends the mono-energetic trap model, to allow the inclusion of a continuum of trap states across the energy band gap.

CHAPTER 3. METHODOLOGY

3.1 Device feature and simulation profile:

The exploration of sensor performance of silicon nanowire was done with the help of numerical simulations using the SILVACO Atlas device simulator [30].

A p-type silicon nanowire with 100 nm thickness was created on a 500 nm Silicon Nitride (Si_3N_4) which was deposited on a 500 nm buried Si layer. We have used 10um length of lightly doped nanowire. A secondary gate (back-gate) is made with 10 nm Al (Aluminum) beneath the buried n-type Si layer with doping concentration 10^{16} /cm³. A heavily doped n-type poly-silicon layer was used as top gate material with doping concentration 10^{20} /cm³ and the gate oxide thickness was 2nm. In the silicon nanowire, two heavily doped regions on the two sides of the channel were implemented to ensure ohmic contacts on the source/drain regions. The heavily doped source/drain regions were p-type with the doping density of 10^{20} /cm³. The channel doping was p-type with doping concentration of 10^{16} /cm³.To contact source, drain and gate, Aluminum (Al) electrode was used.

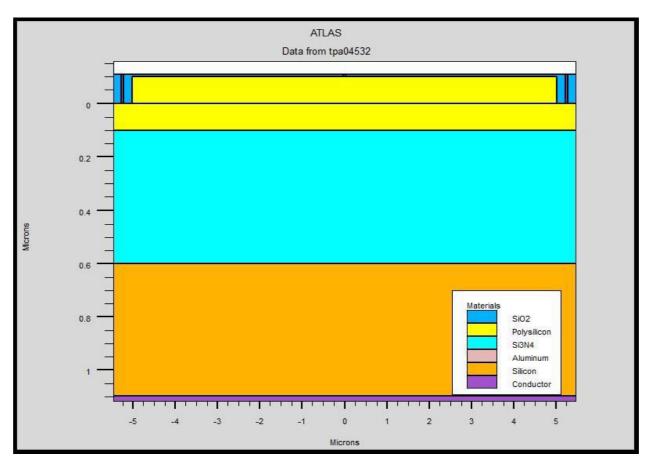


Figure 3.1: Schematic of the simulated p-type silicon nanowire.

As Si NW is 100nm thick quantum effect is neglected and a classical drift diffusion model is used to investigate SiNW behavior. The Shockley-Read-Hall (SRH) model was used for recombination phenomenon within the device. The carrier emission and absorption process (or Phonon transitions) occur in the presence of a trap (or defect) within the forbidden gap of the semiconductor. The theory of two steps process which was first proposed by Shockley and Read [27] and then by Hall [29]. The Shockley-Read-Hall recombination is modeled as follows:

$$R_{SRH} = \frac{pn - n_{ie}^2}{TAUPO[n + n_{ie} \exp\left(\frac{ETRAP}{kT_L}\right) + TAUNO[p + n_{ie} \exp\left(\frac{-ETRAP}{kT_L}\right)} \cdots \cdots \cdots (3.1)$$

Where, ETRAP is the difference between the trap energy level and the intrinsic Fermi level, TL is the lattice temperature in degrees Kelvin and TAUN0 and TAUP0 are the electron and hole lifetimes. This model is activated with the SRH parameter of the MODELS statement. The electron and hole lifetime parameters TAUN0 and TAUP0 are user definable on the MATERIAL statement. The default values for carrier lifetimes are shown in Table 3-1.

Table 3.1: Default Parameters for Equation 3.1	

Statement	Parameter	Defaults	Units
MATERIAL	ETRAP	0	V
MATERIAL	TAUNO	1.0×10-7	S
MATERIAL	TAUPO	1.0×10-7	S

In NW the presence of heavy doping which is 10^{20} /cm³. Bandgap narrowing model uncomforted. A decrease in the bandgap separation occurs, when the doping increases where the conduction band is lowered by approximately the same amount as the valance band raised. In Atlas this is simulated using this formula-

$$n_{ie}^2 = n_i^2 \left(\frac{\Delta E_g}{kT}\right) \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots (3.2)$$

We have used bandgap narrowing model by specifying the BGN parameter of the MODELS statement. Bandgap narrowing effects may be described by an analytic expression relating the variation in bandgap,

 Δ Eg, to the doping concentration, N. The expression used in ATLAS is from Slotboom and de Graaf [35]:

$$\Delta E_g = BGN. E\{ln \frac{N}{BGN.N} + \left[\left(ln \frac{N}{BGN.N}\right)^2 + BGN.C\right]^{\frac{1}{2}}\}\cdots\cdots\cdots\cdots(3.3)$$

The default values for the parameters BGN.E, BGN.N and BGN.C are shown in Table 3.2[30].

Table 3.2: Default parameters of Slotbooms	s Bandgap Narrowing	Model for equation 3.3
--	---------------------	------------------------

Statement	Parameter	Default	Units
MATERIAL	BGN.E	9.0×10^{16}	V
MATERIAL	BGN.N	1.0×10^{16}	cm ⁻³
MATERIAL	BGN.C	0.5	-

Fermi: Electrons in thermal equilibrium at temperature TL with a semiconductor lattice obey Fermi-Dirac statistics. That is the probability $f(\varepsilon)$ that an available electron state with energy ε is occupied by an electron is:

Where E_F is a spatially independent reference energy known as the Fermi level and k is Boltzmann's constant.

In the limit that ε - E_F>>kT_L Equation 3-25 can be approximated as:

$$f(\varepsilon) = \exp(\frac{E_F - \varepsilon}{kT_L}) \cdots \cdots \cdots \cdots \cdots (3.5)$$

The use of Boltzmann statistics instead of Fermi-Dirac statistics makes subsequent calculations much simpler. The use of Boltzmann statistics is normally justified in semiconductor device theory, but Fermi-Dirac statistics are necessary to account for certain properties of very highly doped (degenerate) materials. The remainder of this section outlines derivations and results for the simpler case of Boltzmann statistics which are the default in ATLAS. Users can specify that ATLAS is to use Fermi-Dirac statistics by specifying the parameter FERMI on the MODEL statement.

In this research work we used constant mobility model for polysilicon NWs simulation because TFT module in ATLAS is compatible with constant low field mobility model only. Use of other mobility model overwrites constant low field model and gives inaccurate results. Constant low field mobility model is independent of doping concentration, carrier densities and electric field. It does account for lattice scattering due to temperature according to:

$$\mu_{n0} = MUN(\frac{T_L}{300})^{-TMUN} \dots \dots \dots \dots \dots (3.6)$$
$$\mu_{p0} = MUP(\frac{T_L}{300})^{-TMUP} \dots \dots \dots \dots \dots \dots \dots (3.7)$$

Where, T is the lattice temperature. The low field mobility parameters: MUN, MUP, TMUN and TMUP can be specified in the MOBILITY statement with the defaults as shown in Table 3.3.

Statement	Parameter	Defaults	Unit
MOBILITY	MUN	1000	cm2 / V. s
MOBILITY	MUP	500	cm2 / V. s
MOBILITY	TMUN	1.5	-
MOBILITY	TMUP	1.5	-

Table 3.3: Default mobility model values for polysilicon

However, we have used MUN=14 cm2 / V.s and MUP=6 cm2 / V.s. parameter under the MATERIAL statement.

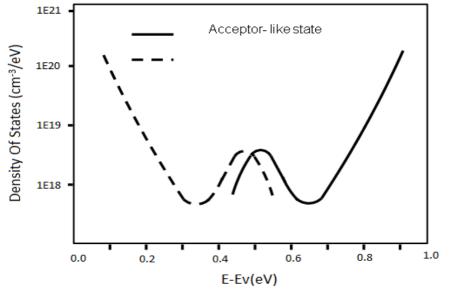
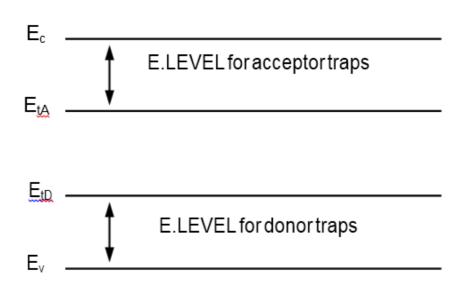
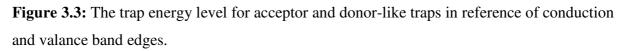


Figure 3.2: The distribution of acceptor and donor-like trap states across forbidden energy gap.

Polysilicon is a disorder material which contains a large number of defects states within the band gap of the material and interface. To accurately simulate the polysilicon NWs with defects in ATLAS; the continuous defect density of states (DOS) used. The defect states as a combination of exponentially decaying band Tail states and Gaussian distribution of mid gap states [31-32] shown in Fig. 3.2 which theory described in chapter 2. In our work we have used continuous defect density of states (DOS) for p-type polysilicon nanowire simulation.

In polysilicon devices interface trap levels capture carriers, which slow down the switching speed of any device. The capture cross sections are used to define the properties of each trap. In ATLAS the INTTRAP command activates interface defect traps at discrete energy levels within the bandgap of the semiconductor shown in Fig. 3.3. We used discrete interface trap levels for simulation as it significantly reduces run time





The total charge caused by the presence of traps is added into the right hand side of Poisson's equation. The total charge value is defined by:

$$Q_T = q(p_t - n_t) \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots (3.8)$$

Where, n_t and p_t are the densities of trapped charge for donor-like and acceptor-like traps respectively.

The trapped charge depends upon the trap density and its probability of occupation, $F_{n,p}$. For donor-like and acceptor-like traps, respectively, the trapped charge is calculated by the equations:

$$n_t = DENSITY \times F_n \cdots \cdots \cdots \cdots \cdots (3.9)$$
$$p_t = DENSITY \times F_p \cdots \cdots \cdots \cdots \cdots \cdots \cdots (3.10)$$

The probability of occupation assumes that the capture cross sections are constant for all energies in a given band and follows the analysis developed by Simmons and Taylor [33]. The probability of occupation is defined by the following equations for donor- and acceptor-like traps respectively:

$$F_n = \frac{V_n SIGN \ n + e_p}{V_n (SIGN \ n + SIGP \ p) + (e_n + e_p)} \cdots (3.11)$$

$$F_p = \frac{V_p SIGP \ p + e_n}{V_p (SIGN \ n + SIGP \ p) + (e_n + e_p)} \cdots (3.12)$$

Where, SIGN and SIGP are the carrier capture cross sections for electrons and holes respectively, V_n and V_p are the thermal velocities for electrons and holes and the electron and hole emission rates. e_n and e_p are defined by:

Where, E_i is the intrinsic Fermi level position, E.LEVEL is the energy level in the bandgap of each discrete trap center and DEGEN.FAC is the degeneracy factor of the trap center. The latter term takes into account that spin degeneracy will exist, that is the "empty" and "full" conditions of a flaw will normally have different spin and orbital degeneracy choices.

Table 3.4 User-Specifiable Parameters for Equations 3.9 to 3.14

Statement	Parameter	Unit
INTRAP	E.LEVEL	eV
INTRAP	DENSITY	cm ³
INTRAP	DEGEN.FAC	
INTRAP	SIGN	cm ²
INTRAP	SIGP	cm ²

3.2 Simulation profile

Device simulation using SILVACO device simulator ATLAS usually faces convergence problems and necessitates a long run times. To avoid these problems, the simulation of silicon nanowire MOSFET has been divided into a few groups. At first, structure definition was performed. In this definition the simulation focused on creating the structure with a suitable mesh density. Regions and electrodes were defined as depicted in Fig. 2.2. Finer nodes were assigned in critical areas, such as across the gate oxide for an accurate 10nm thickness to monitor channel activity and to get a better picture of the depletion layer and junction behavior near the source/drain boundaries. A coarser mesh was used elsewhere in order to reduce simulation run time.

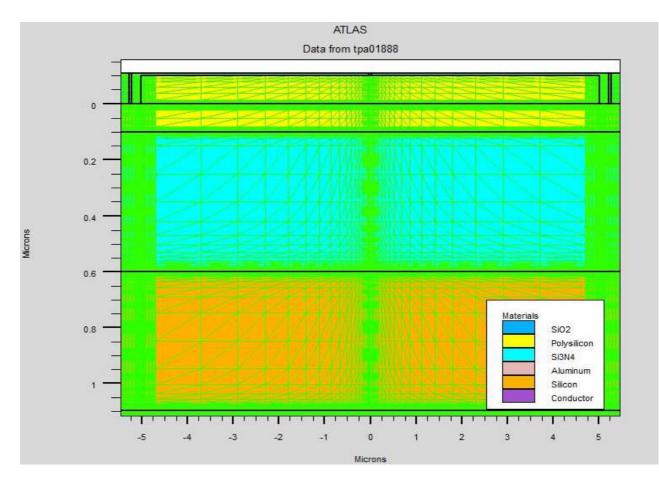


Figure 3.4: Cross-sectional view of p-type nanowire showing the mesh density used in this simulation.

Once the structure and the mesh were found to be as desired, the simulation was performed with appropriate models as discussed in section 3.1 and numerical solving methods. The model was invoked by using the statements FERMI, SRH, BGN. The numerical solving

methods GUMMEL, NEWTON were used to reduce the simulation run time, while keeping the accuracy of the simulation at an acceptable level.

To get convergence, a special bias point solving method was used. It was found that the simulation faced difficulty in solving the initial desired bias points. i.e. $\pm 3V$, $\pm 7V$, $\pm 15V$ and -30V for backgate voltage and $\pm 1V$ for drain voltage. Therefore, the initial gate bias was set to 0.005V and the next bias point was set to 0.05 V, before finally setting the bias point to desired value.

CHAPTER 4: RESULT AND DISCUSSION

In this section we investigate the DC electrical characteristics of 100nm thick 10 μ m long polycrystalline silicon nanowire and extract its conductance charge with the change of the top gate voltages to investigate its suitability DC biosensors. To get physical results nanowire characteristics is first calibrated with reported experimental results of poly crystalline Si nanowire biosensors. Exactly like reported fabrication [34] our structure also comprises of a 100nm polysilicon layer or 500nm nitride. Polysilicon nanowire length is 10 μ m whereas the substrate is taken n-type with doping $10^{16}/cm^3$. Nanowire was covered with 10nm of oxide layer and two heavily doped p-type regions $(10^{20}/cm^3)$ at the two sides of nanowire are used as source and drain. As reported in the literature the body doping of nanowire is taken as $10^{16}/cm^3$.

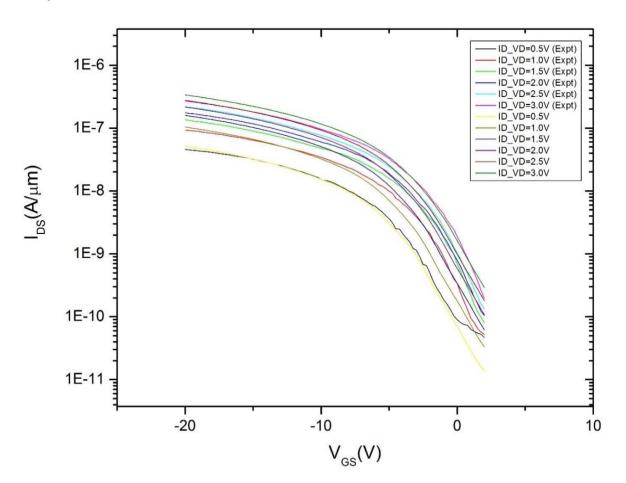


Fig 4.1 I_{DS} vs. V_{GS} characteristics plot of Silicon nanowire

Fig 4.1 compares simulated sub-threshold characteristics of 10μ m long 100nm thick p-type Si nanowire with experimental results. Using continuous grain boundary model inside polysilicon layer and donor type interface state both at the top of oxide-polysilicon and bottom nitride/Si interface gave the excellent match with the experiment as can be seen from fig 4.1 such calibration was achieved using model parameters as shown in table 4.1. During this calibration run Si substrate is used as gate as available experimental data available only for V_{substrate} sweeping.

Device Parameter	Symbol (Units)	Value
Channel Length	L(µm)	10
Channel Width	W(µm)	0.1
Oxide Thickness	t _{ox} (nm)	10
Polysilicon Thickness	t _{si} (nm)	100
Nitride Thickness	t _{nitride} (nm)	500
Silicon Thickness (n-type)	t _{silicon} (nm)	500
Back Gate Thickness	t _{backgate} (nm)	10
Source and Drain Dopant Density	$p^{+}(cm^{-3})$	1×10^{20}
Polysilicon Doping Density	$p^{+}(cm^{-3})$	6×10 ¹⁶
Silicon Substrate Doping Density	$n^{+}(cm^{-3})$	1×10 ¹⁶
Capture Cross Section of Electrons in Acceptor-like States	$\sigma_{ae}(cm^2)$	1×10 ⁻¹⁶
Capture Cross Section of Holes in Acceptor-like States	$\sigma_{ah}(cm^2)$	1×10 ⁻¹⁴
Capture Cross Section of Electrons in Donor-like States	$\sigma_{de}(cm^2)$	1×10 ⁻¹⁴
Capture Cross Section of Holes in Donor-like States	$\sigma_{dh}(cm^2)$	1×10 ⁻¹⁶
Density of Acceptor –like tail States	$N_{TA}(cm^{-3}eV^{-1})$	2×10 ¹⁹
Density of Donor –like tail States	$N_{TD}(cm^{-3}eV^{-1})$	1.2×10^{-18}
Density of Acceptor –like Gaussian States	$N_{GA}(cm^{-3})$	1×10 ¹⁸
Density of Donor –like Gaussian States	$N_{GD}(cm^{-3})$	1×10 ¹⁷
Decay Energy for Acceptor-like Tail states	W _{TA} (eV)	0.05
Decay Energy for Donor-like Tail states	W _{TD} (eV)	0.05
Decay Energy for Acceptor-like Gaussian states	W _{GA} (eV)	0.1
Decay Energy for Donor-like Gaussian states	W _{GD} (eV)	0.1
Energy of Gaussian for Acceptor-like States	E _{GA} (eV)	0.51
	1	

Table 4.1 Device parameters and trap states distribution parameters used for simulation

Energy of Gaussian for Donor-like States	$E_{GD}(eV)$	0.51
Capture Cross Section of the Trap for Electrons at Interface	$\sigma_n(cm^2)$	1×10 ⁻¹⁴
Capture Cross Section of the Trap for Holes at Interface	$\sigma_p(cm^2)$	1×10 ⁻¹⁶
Density of Donor-like Interface trap States	$D_{it}(cm^{-2})$	1.6×10 ⁻¹¹
Degeneracy Factor		1

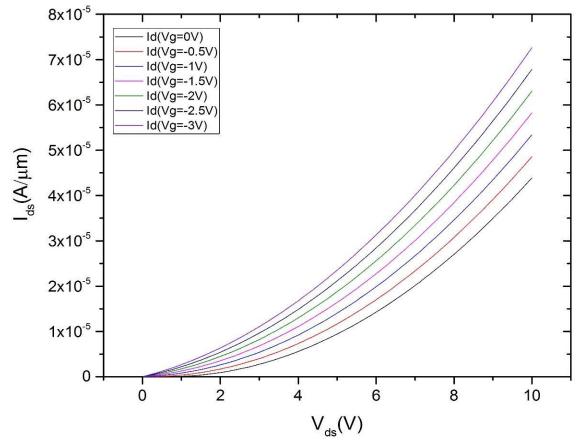


Fig 4.2 I_D vs. V_D characteristics plot with positive drain voltage when gate voltages are negative

Once calibration of nanowire's I_D -V_{GS} characteristics been achieved using V_{substrate} as back gate, a top gate made of n-type $10^{20}/cm^3$ doped is used to investigate sensor performance as it is expected that during sensing operation biomarkers are targeted to be attached in the top surface of nanowire. Fig 4.2 shows nanowire's I_{DS} vs V_{DS} characteristics while V_{DS} is positive and has been swept from 0 to 10v. During this run V_{GS} was charged from 0V to -3V in -0.5V steps. It can be seen that for positive V_{DS} sweeping nanowire's I_{DS} -V_{DS} characteristics are inherently non-linear and nanowire's drive current increase with increasing negative V_{GS} values. For V_{DS} value of +5V, drive current is 9.42E-06A/µm at V_{GS} =0V which increases to a value of 2.35E-05A/ μ m at V_{GS} = -3V. Thus increase in drive current can be explained by hole accumulation in p-type nanowire upon application on negative V_{GS} values.

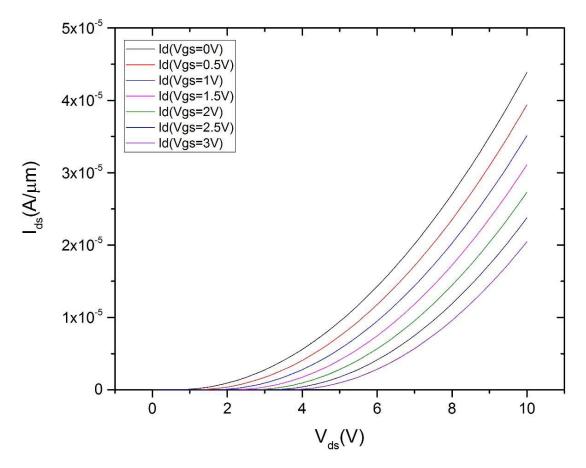


Fig 4.3 I_{DS} vs. V_{DS} characteristics plot with positive drain voltage when gate voltages are positive

Fig 4.3 shows I_{DS} vs V_{DS} characteristics of p-type Si nanowire when V_{DS} is swept from 0V to +10V but V_{GS} has been charged from 0 to +3V. It can be seen that when V_{DS} is positive with the increase of positive V_{GS} values drive current characteristics is becoming more non-linear than the characteristics when allowed V_{GS} is negative. In addition, drive current value is found to decrease with the increase of positive V_{GS} values for any fixed V_{DS} . The decrease of the drive current and increased of non-linearity in the characteristics with the increase of positive V_{GS} values can be explained by depletion of p-type nanowire upon application of positive V_{GS} values thereby making nanowire more sensitive.

Fig 4.4 shows sub threshold (I_{DS} vs. V_{GS}) characteristics of the p-type polysilicon nanowire for positive drain voltages from +0.5V to +3V in 0.5V step while gate voltage has been swept from -10V to +10V. It can be seen that 10µm long and 100nm thick polysilicon nanowire exhibit a sub threshold slope of 83.33mV/decade and I_{DS} -V_{GS} curve shifts to right for increasing in gate voltage. This shift is known as drain induced barrier lowering in CMOS technology and is measured by constant current threshold technique.

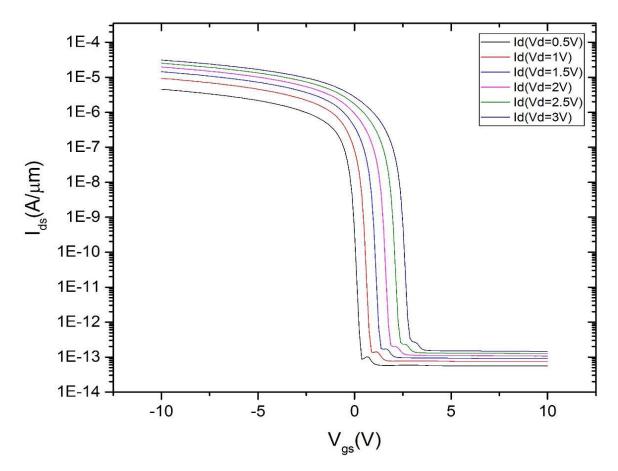


Fig 4.4 I_{DS} vs. V_{GS} characteristics plot with positive drain voltage

Such a sub-threshold slope is actually quite promising for poly Si nanowire biosensor operation if operating point is chosen inside the linear region on sub threshold slope. Traditionally DIBL is known to be disadvantageous for MOS circuits. However, for biosensor operation this shift/DIBL somehow beneficiary as it is providing flexibility of wide range liquid gated voltage values with associated V_{DS} values depending on the charge of targeted biomarkers.

Fig 4.5 shows I_{DS} vs. V_{DS} characteristics of p-type polysilicon nanowire when V_{DS} is negative for different values of negative V_{GS} values. In comparison to the characteristics of positive V_{DS} values, the characteristics with negative V_{DS} values show a drastic change in behavior poly Silicon nanowire at this bias condition exhibit excellent transistor characteristics with perfect saturation in behavior. However, due to hole accumulation saturation current also increases with increasing negative V_{GS} values when the applied V_{DS} is negative. We have also investigated I_{DS} - V_{DS} characteristics of p-type poly silicon nanowire when V_{DS} is negative but V_{GS} is positive.

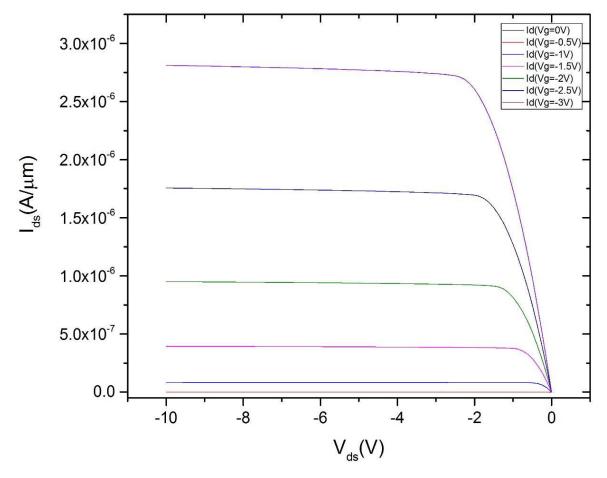


Fig 4.5 I_{DS} vs. V_{DS} characteristics plot with negative drain voltage when gate voltage is negative (I_{DS} in reverse order)

If this condition device drive current is insignificant and nanowire shows anomalous conduction characteristics due to significant V_{GS} associated depletion of carriers.

Fig 4.6 shows sub-threshold characteristics of p-type poly silicon nanowire when V_{DS} is negative. For negative V_{DS} application device exhibit a sub-threshold slope 83.33 mv/decade which is similar to the sub-threshold slope with positive V_{DS} supplication. However, for negative V_{DS} values no DIBL is seen and I_{DS} - V_{DS} curve does not shift upon increasing the applied V_{DS} . This behavior imply that p-type ply silicon nanowire still could be good biosensor if operating point is chosen inside linear region of the curve. However, absence of DIBL restricts the applicable liquid gate voltages for biosensors.

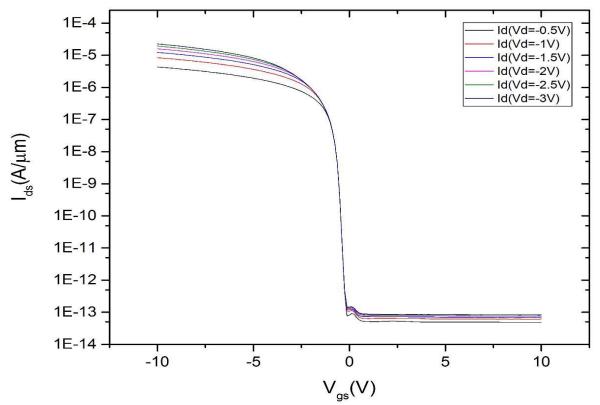


Fig 4.6 I_{DS} vs. V_{GS} characteristics plot with negative drain voltage (I_D in reverse order)

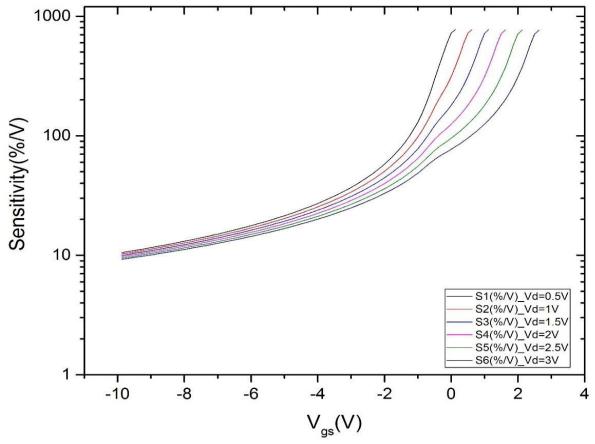
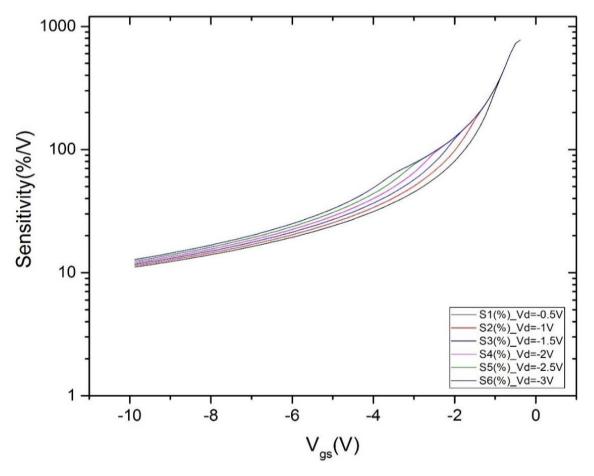
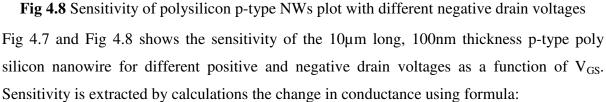


Fig 4.7 Sensitivity of polysilicon p-type NWs with different positive drain voltages





$$Sensitivity = \frac{(I_2 - I_1)}{\{I_2 \times (V_{G2} - V_{G1})\}} \times 100(\%/V) \cdots \cdots \cdots \cdots \cdots (4.1)$$

It can be seen that the maximum sensitivity for the positive drain voltage in fig 4.7 is 774%/V when V_{DS} is +0.5V and V_{GS} is 0.125V and 765%/V when V_D is +3V and V_{GS} is 2.625V. The sensitivity curve shifts towards positive V_{GS} values with increasing in drain voltages. Sensitivity reduces with the increase of negative V_{GS} values. For the negative drain voltage, the maximum sensitivity is 774%/V at peak for all V_D values and when V_{GS} is -0.375V. The sensitivity curve does not shift with increasing V_{DS} voltages and sensitivity again decreases with increasing negative V_{GS} values. However, both for positive and negative V_{DS} applications maximum sensitivity that can be achieved using 10µm long 100nm thick nanowire is around **≈ 750%**. This value of sensitivity may not be as good as single crystal Si nanowire but possible enough for applying p-type 10µm long 100nm thick Si nanowire as biosensor.

CHAPTER 5: CONCLUSION

We have investigated electrical characteristics of 100nm thick 10 μ m long p-type low-doped Si nanowire's electrical behavior for biosensor operation. For positive drain voltage application nanowire shows non-linear diode like characteristics where for negative drain voltage application it exhibits perfect transistor behavior on output characteristics. For both positive and negative V_{DS} applications device exhibit sub threshold slope of 83.33 mv/decade which shows that poly silicon nanowire is good candidate for bio sensing operation. However maximum sensitivity which can be achieved is limited to 750%. It is also found that positive V_{DS} application is somehow beneficiary which provides flexibility of wide range of liquid gated voltage depends on biomarker charge whereas negative drain voltage application restrains liquid gated voltages. This study reveals applicable voltages ranges of 10 μ m long 100nm thick low doped p-type Si nanowire biosensors operation and maximum conductance change possible for detection of biomarkers.

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