

An Investigation on the corner effects of non-classical MOS architecture

By

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Abstract

Traditionally, the technological development has been performed by means of the scaling down of the device dimensions, each vertically and laterally. Nonetheless, as device dimensions moved into nanometer regime, quantum mechanical tunnelling and bodily barrier have rendered device down-scaling a difficult task. Revolutionary measures, together with making use of substitute materials and replacement device structure are as a result inevitable to be able to maintain Moore's regulation. Among these novel devices, the vertical MOS transistor is deemed promising as it presents related, if not better performance than different novel devices and yet it's CMOS method compatible.

On this thesis, the effects of corner in the vertical MOS transistor had been investigated utilising 3-dimensional device simulator, ATLAS3D from Silvaco TCAD bundle. Various gate structure and gate widths were simulated and investigated. The gate length, L_G was once stored at 60 nm for the entire simulations, with the gate oxide of 2nm thick and pillar measurement of $100\text{nm} \times 100\text{nm} \times 100\text{nm}$. The substrate doping concentration used is $1 \times 10^{18} \text{ cm}^{-3}$, even as the source or drain area is modelled with abrupt junction and uniform concentration of $1 \times 10^{21} \text{ cm}^{-3}$. A evenly doped area of $1 \times 10^{18} \text{ cm}^{-3}$ is used to modelled a doubly doped drain constitution.

The simulation of the quadruple gate and corner gate vertical MOS transistor are also awarded and analyzed for width edge and corner effects. The current drive increases because the gate width is extended however off-state current decreases at identical time. This leads to lower subthreshold slope for higher gate dimension devices and could be thanks to additional distance of adjacent gates once the gate dimension is reduced, thus amplifying the dimension edge result.

For many of the gate structures simulated, the corners of the pillar area unit determined to activate sooner than the non- corner sections, thus confirmed a threshold voltage decreasing at the corners. The corner section has shown a major contribution to complete drain current when the device is biased above the threshold voltage. With corner section occupying 240nm of the gate width, and the non-corner section taking 240nm, at 0.1V the drain current contribution of corner section is estimated to be 36.75% and at 1.0V the drain current contribution of corner section is estimated to be 2.30% founded on physical ratio. With corner section occupying 160nm of the gate width, and the non-corner section taking 160nm, at 0.1V the drain current

contribution of corner section is estimated to be 85.43% and at 1.0V the drain current contribution of corner section is estimated to be 3.46% founded on physical ratio. In corner gate and double gate taking 80nm at 0.1V the drain current contribution of corner section is estimated to be 97.44% and at 1.0V the drain current contribution of corner section is estimated to be 6.20% founded on physical ratio. This is believed to be valuable to increase the saturation current drive.

The percentage contribution of complete drain current from the corner section lowered when V_G is decreased, and was once least at V_G close to threshold voltage. However, when V_G is further decreased, the corner begins to make contributions to the drain current once more and might overtake the have an effect on of non-corner section when the drain voltage is high.

The discussion given during this thesis is intuitive and more verification with measured knowledge will certainly create it additional credible.

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First of all, we would like to thank and express our gratitude to our thesis supervisor professor Dr. Mohammad Mojammel Al Hakim, Department of Electrical and Electronic Engineering of East West University, Dhaka, Bangladesh for his motivation, continuous support and affectionate guidance. It has been a pleasant learning process. Without his motivation and dedication we could not reached this phase of thesis. We again thank our supervisor from the core of our heart.

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Finally we would like to our parents without them we could not be reached in this stage and also want to thank to our lovely friends and well-wisher for their support and encouragement in this work.

Approval

The thesis title “An Investigation on the corner effects of non-classical MOS architecture” submitted by Asef Bin Amdad (2013-2-80-014), Suraiya Jabin (2013-2-80-039) and Sayma Islam Nitu (2013-2-80-105) in the semester of Summer-2017, has been approved as satisfactory in partial fulfilment of the degree of the Bachelor of Science in Electrical and Electronic Engineering on August, 2017.

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Authorization

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Chapter 1

1.1 Introduction:

Increasing industry's needs for more overall performance and capability at lower cost has pushed many foundries to work beyond the visions of Moore's Law and International technology Roadmap for Semiconductor (ITRS). In Fact, the rate of development has always been ahead of the expected functions estimated by using ITRS [1], [2]. This astonishing technological advancement has been historically achieved through the scaling down of the device dimensions, both the vertical dimensions, such as the gate dielectric thickness and junction depth, and the lateral dimensions, such as gate length and lithographic feature size or pitch size. At present, in high performance applications, transistor dimensions have shrunk beyond nanometer regime, with gate length at sub-100nm regime and gate oxide thickness than 2nm.

At this nanometer regime, direct quantum-mechanical tunnelling of carriers starts to occur, resulting in an exponential increase in off-state leakage current. In addition, the physical thickness limit of the gate oxide layer, for instance, is predicted to be 7\AA in order to properly function as a dielectric layer [3], [4]. Hence, conventional down scaling cannot continue forever. Future improvement, inevitably, needs innovative measures to surmount the barriers of scaling due to fundamental physical constraints.

1.2 Alternative Innovations:

While efforts is still been put into realizing down-scaling with conventional techniques, innovative measures to look into alternative materials and alternative structures have drawn a lot more attentions from academia, in addition to industrial players. Many innovative techniques, which includes introducing strained silicon to increase carriers's mobility, and using alternative materials such as high-K gate dielectric and metal gate could be next [5]. alternative structure such as ultra-thin body (UTB) MOSFET, novel non-planar structure such as Vertical MOS transistor which is not visible in planar devices due to manufacturing process complexity and parasitic effects.

In our thesis studies, we focused on the non- classical MOS architecture and the projection of non-planner devices. Non-planner devices give the excellent performance in present. We focused on the 3-dimensional devices of corner effect in non-planner devices. In previous, no worked based on the corner effect, it seems new to us and everyone. If further investigate about corner effect, we haven't knowledge about it. Corner effect based on the corner of pillar towards the subthreshold performance of the transistor and short channel effects on the device.

Chapter 2

2.1 Overview:

In this work, the 3-dimensional vertical MOS transistor is simulated by using Silvaco's ATLAS device simulation software. The main focus of this simulation is effect of the corners of the pillar towards the subthreshold performance of the transistor and short channel effects on the device. The simulation models and simulation profiles, with various gate structures and widths were discussed and simulated. The $I_{DS}-V_G$ curve For V_{DS} at 0.1V and 1.0V were simulated and plotted.

2.2 Device Features:

With various gate structures and widths ,we have discussed about six gate structures which are named as surround gate, quadruple gate, single gate ,double gate, corner gate and combined gate and their various gate widths of 400nm, 368nm, 320nm, 240nm, 160nm, 80nm, 40nm and 32nm were simulated. Here each gate structures has different gate width but has same gate length of 60nm, gate oxide thickness of 2nm and a pillar size of 100 nm×100nm×100nm. The substrate doping concentration is assumed to be $1 \times 10^{18} \text{cm}^{-3}$ for achieving a low sheet resistance and very thin depletion depths[58]. The source /drain region is modeled with abrupt junction and uniform concentration of $1 \times 10^{21} \text{cm}^{-3}$, assuming a solid source diffusion technology is available. Due to its simplicity and practicality in modeling, the source/drain structure is modeled with doubly doped drain with minimum overlap (DDD) structure, in preference to opposed to popular lightly doped drain (LDD) structure, or large-angle-tilt implanted drain (LATID) structure[59-62] .

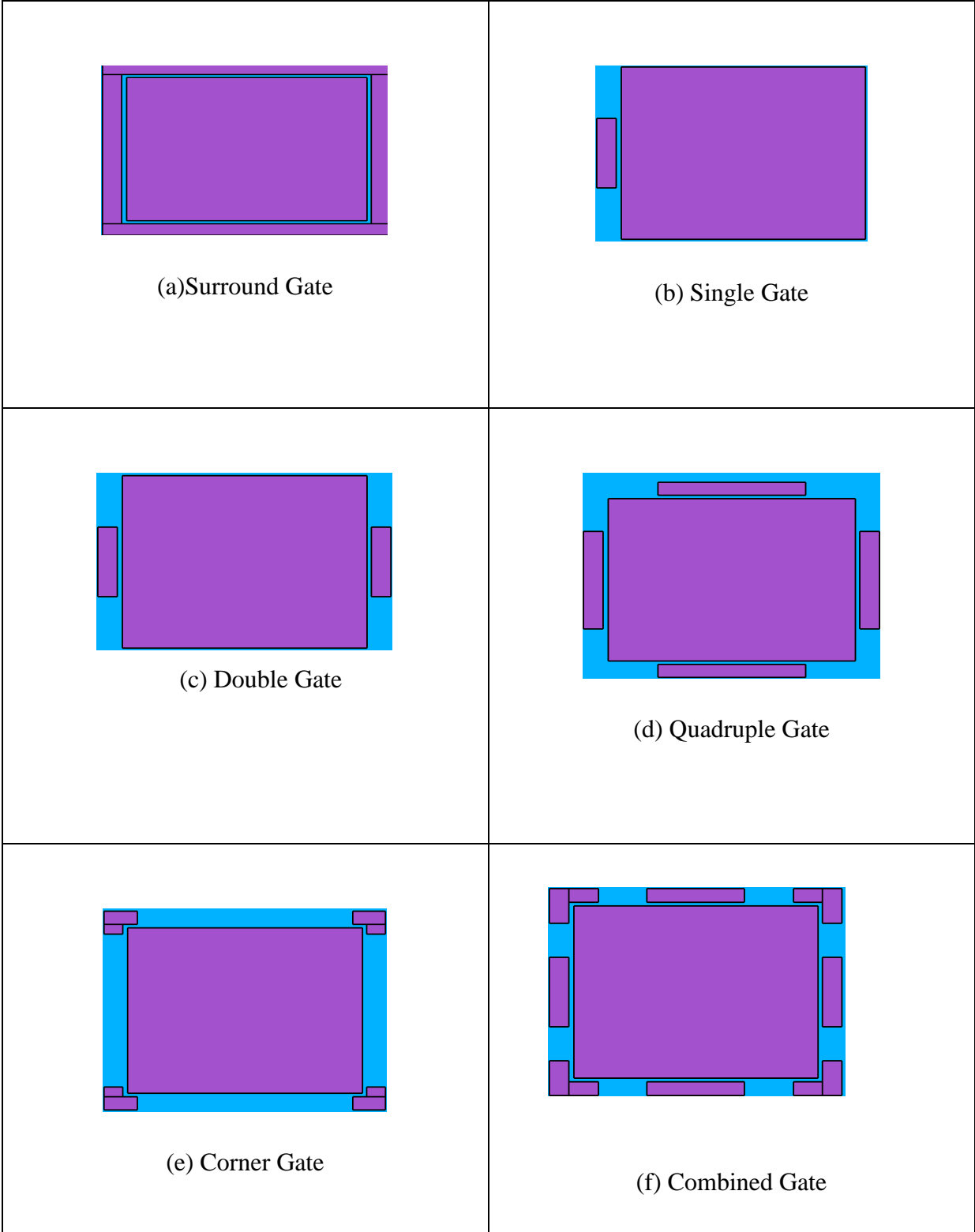


Figure 2.1: Top View of various gate structures used in the simulation

Chapter 3

3.1 Simulation Models:

ATLAS provides different types of physical models, which are mobility models, carrier recombination and regeneration models, energy balance simulations, lattice heating simulations, classical carrier statistic models and quantum carrier statistic models [67]. From these different types of models, carrier recombination and mobility models are usually specified. There are some default models also look after, for example carrier statistic modeling. For a more through analysis some of these models can be coupled together. There are some models which are not fully supported in 3D simulation. So for clarity it is important to refer the manual.

In this work the electrostatic potential and current concentration in all x-,y- and z- direction are of particular interest. The dependency of carrier mobility in parallel and transverse field should include for the selection of physical model.

Lombardi CVT model couples the transverse field, doping dependent and temperature dependent which are arts of the mobility model. CVT model also applies in the parallel electric field dependent mobility model for velocity saturation. The CVT model performs better in solving the bias point.

3.2 Simulation Profile:

The simulation of this 3D vertical MOS transistor has been divided into a several part. First of all we concentrate the structure with appropriate mesh density. In some difficult area finer nodes were allocated, like an accurate 2nm thickness across the gate oxide, to observe the channel activities near the sidewall of the pillar, near the source or drain boundaries to get a better picture of the depletion layer and the junction characteristics. To reduce the simulation run time coarser mesh has been used for long time, which can be calculated by N^α , where N is the number of nodes and α is either 2 or 3 depends on the complexity of the structure. Eliminate statement is using to enumerate the mesh density to coarser at the areas around substrate and field oxide.

When the structure and mesh are done, to obtain the best choice of model, numerical solving method and bias point solving preference the simulation is being performed. In order to reduce

the simulation run time and to keep the accuracy of simulation result in tolerable level the above mention phase is playing a vital role here. Depicted simulation model has been given in section simulation model.

In this work for different gate structure and gate width simulation cases were established. The gate widths chosen based on the defined mesh density. The chosen gate widths are listed in the table 3.1. The mesh density will be constant for all simulations to perform a coherent analysis. Here, 14 tests cases were simulated which are listed in table 3.1, first for drain voltage, $V_{DS}=0.1V$ and the gate voltage, V_G changed from 0.1V to 1.5V. In lower drain voltage, from the analysis probably able to illustrate the short channel effect and also focuses on the current and potential of the transistor which are affected by the gate structures. Therefore, V_{DS} is increased to 1.0V and changing gate voltage V_G the same way, the simulation were repeated.

Test case	Gate Width(nm)	Gate Structures
01	400	Surround Gate
02	400	Quadruple Gate
03	368	Combined Gate
04	368	Quadruple Gate
05	320	Quadruple Gate
06	240	Corner Gate
07	240	Quadruple Gate
08	240	Combined gate
09	160	Quadruple Gate
10	160	Corner Gate
11	80	Double Gate
12	40	Single Gate
13	80	Corner Gate
14	32	Corner Gate

Table 3.1: List of test cases used in the simulation

Chapter 4

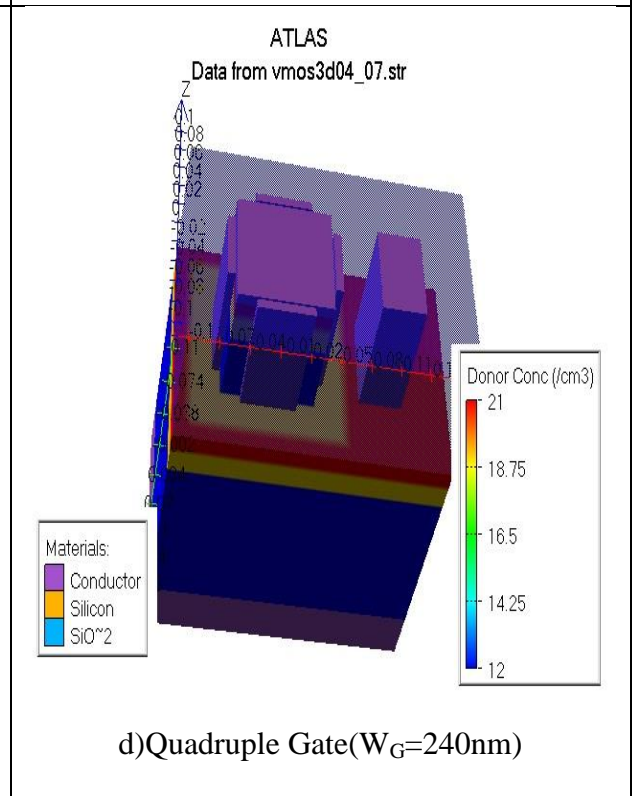
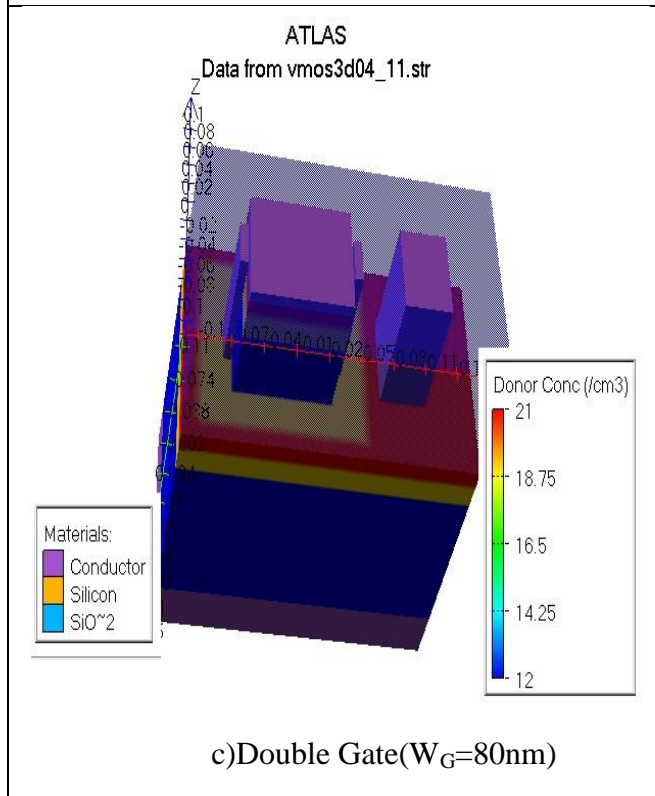
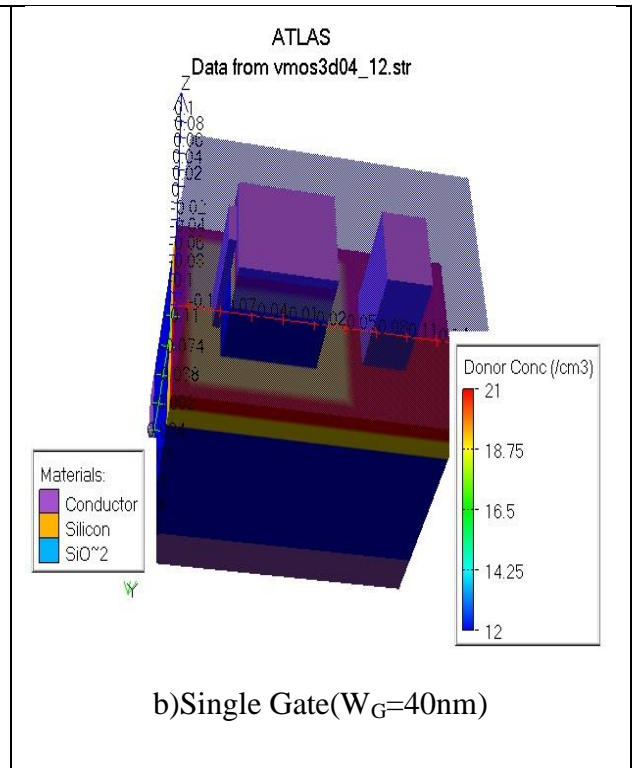
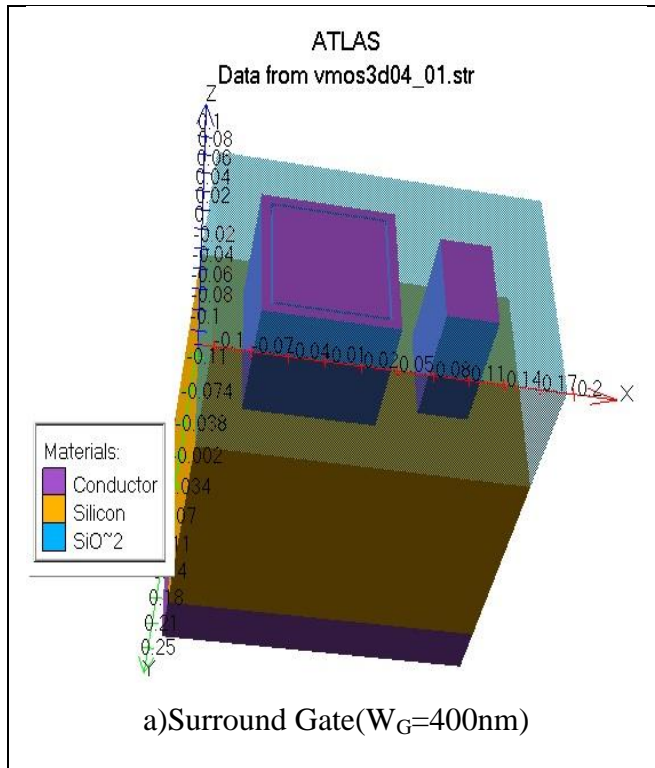
Result and analysis

4.1 Simulation Results

The have an effect on of gate structure and gate width on the short channel consequences and the transistor's performance inside the subthreshold regime and investigated and analyzed. Unique interest is given to the have an effect on of the corner gate structure almost about off-state current and drive current capability of the transistor. Finally, comparisons are made with reference to other gate structure to work the seriousness of the consequences of the corner on the transistor's overall performance.

4.2 Structure and Mesh Density

The structures of simulated gate in 3D square measure delineate in Figure 4.6 let's say the physical outlook of the outlined structures. The oxide layers are created clear for clarity. The structures of gate illustrated square measure below non-bias condition and therefore the doping concentrations square measure shown with DDD profile at the source or drain regions. The mesh density used throughout the simulations is additionally illustrated in Figure 4.2. It will be seen that finer mesh has been outlined close to the important space mentioned previously, whereas coarser mesh square measure outlined elsewhere.



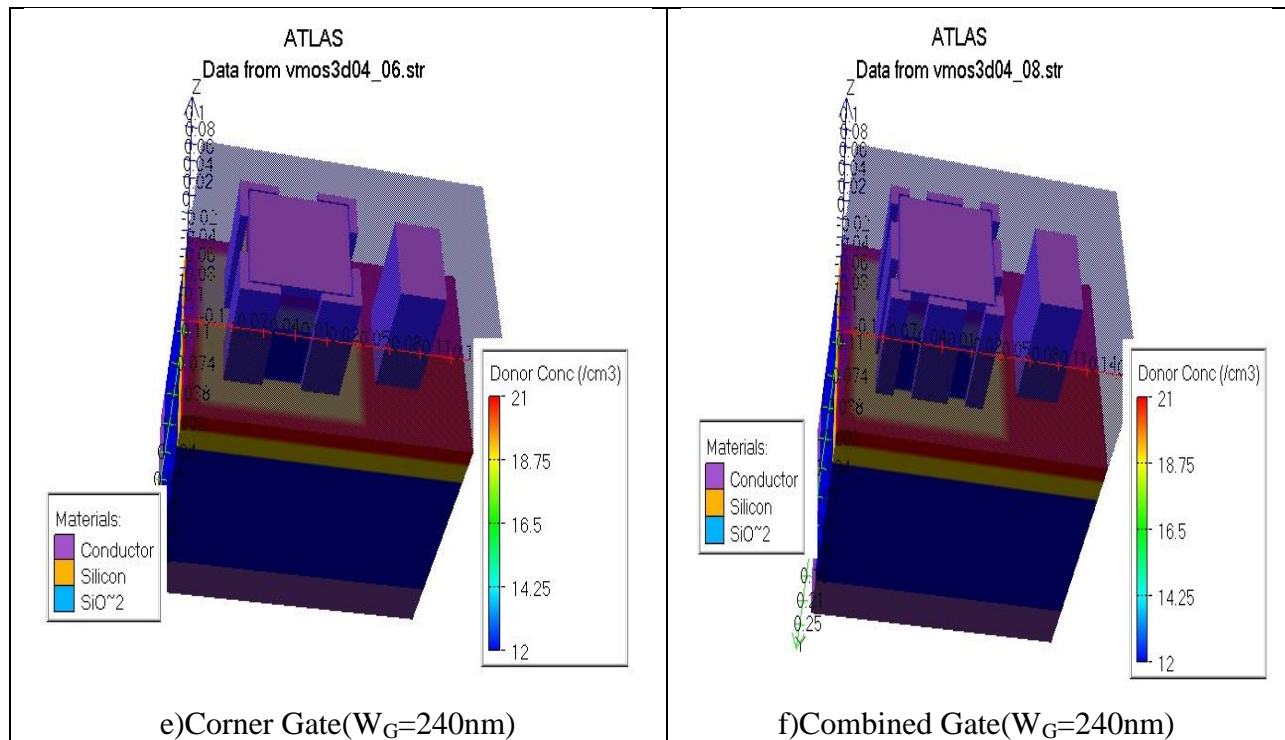


Figure 4.1: 3D view of various simulated gate structures. Oxide layer have been made transparent for clarity.

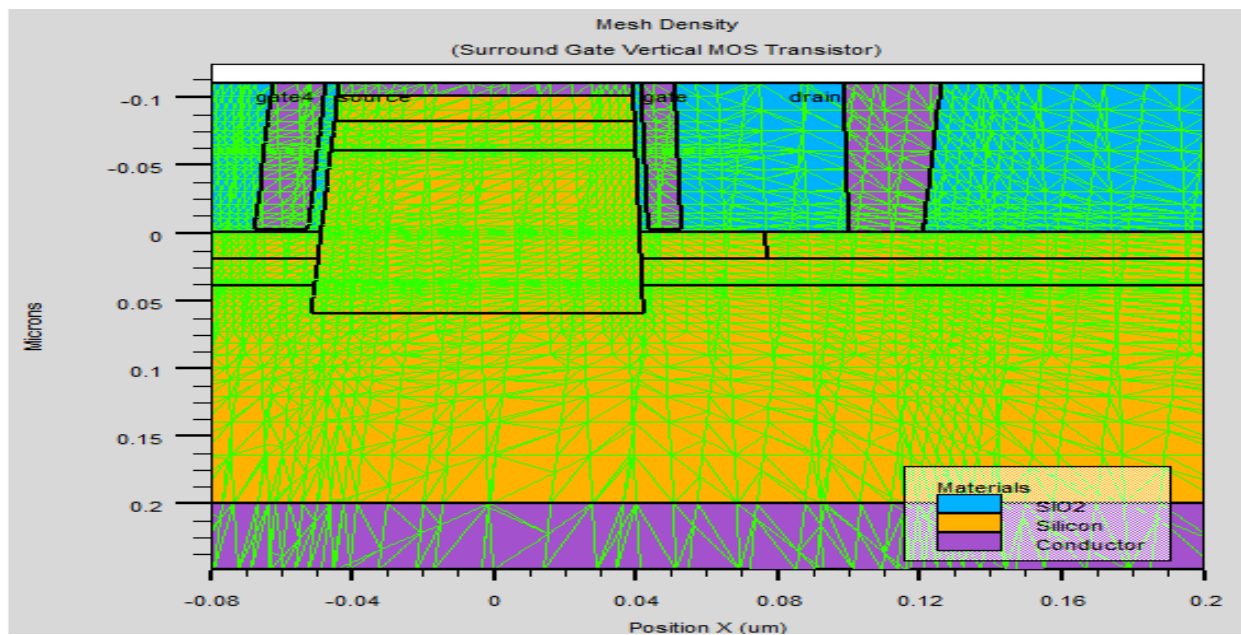


Figure 4.2: Cross-section view of surround gate vertical MOS transistor, displayed the mesh density used in the simulation.

4.3 Surround Gate Vertical MOS Transistor:

The surround gate structure simulation is based on gate width of 400nm where the pillar size is fixed at 100 nm×100nm×100nm. The output characteristics of the surround gate is simulated where the drain current, I_{DS} simulation has a unit of Ampere[A] due to 3D simulation instead of Ampere per micron [A/ μm] in 2D normalize simulation. Where $V_{ds}=0.1\text{V}$ the subthreshold slope, S is 66.08mV/dec and for $V_{ds}=1.0\text{V}$ subthreshold slope, S is 65.81mV/dec where $\text{DIBL}=22.6\text{mV}$. At $V_G=2.0\text{V}$, convergence issue occurred when ramping V_{DS} from 0V to 2V. Convergence issues also occurred at lower gate voltages. The simulator stopped to converge at $V_{DS}=1.4\text{V}$, after a number of iteration with bias update reduction had been performed. By managing automatic bias step reduction convergence problem may overcome. The device have been fully depleted when subthreshold characteristics are found to be near ideal.

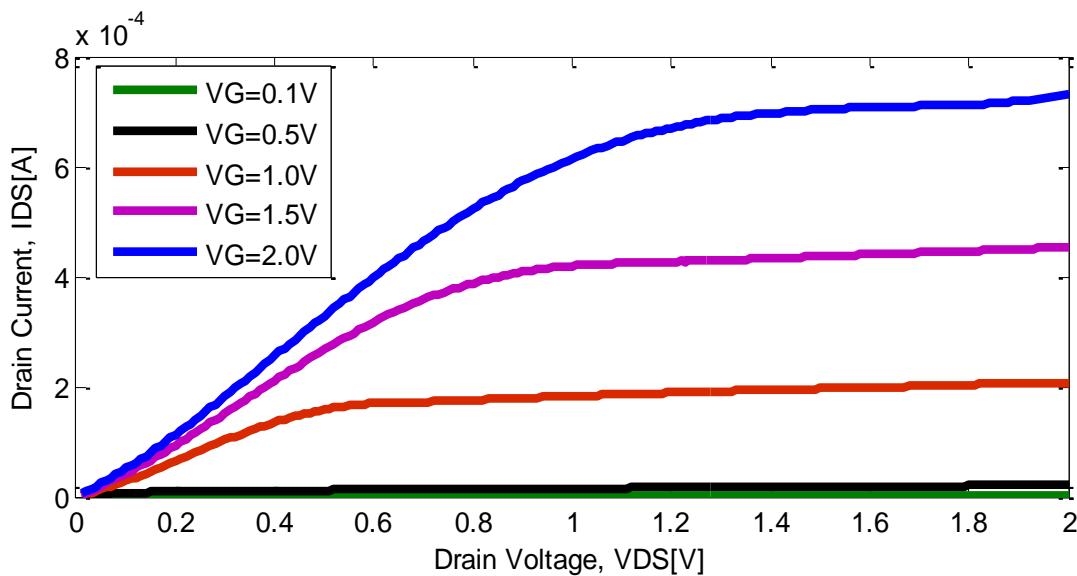


Figure 4.3: Simulated output characteristics of a Surround Gate Vertical MOS transistor in linear scale with gate Width of 400nm

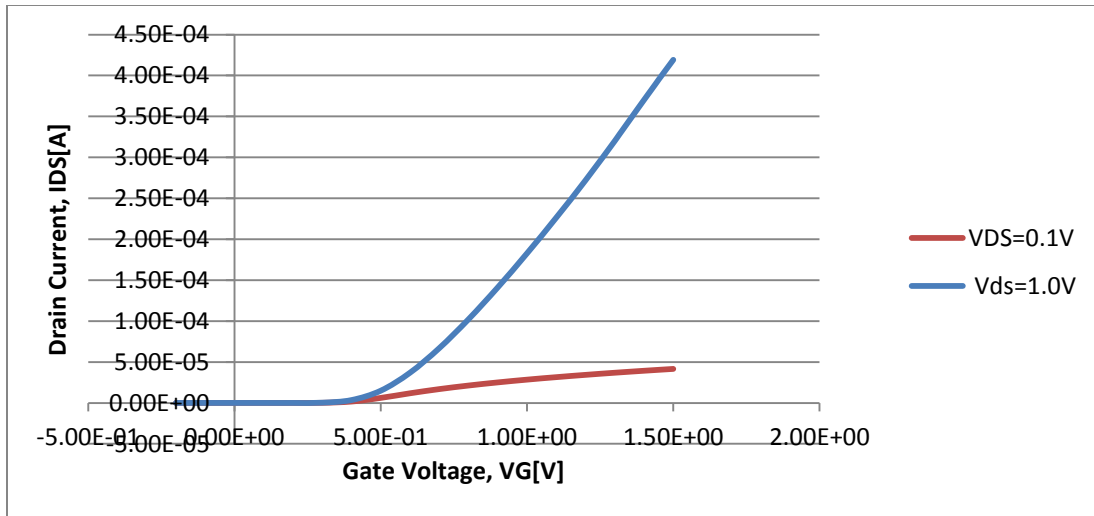


Figure 4.4: Simulated subthreshold characteristics of a surround gate vertical MOS transistor in linear scale with gate width of 400nm, for 400nm, for $V_{DS}=0.1V$ and $1.0V$

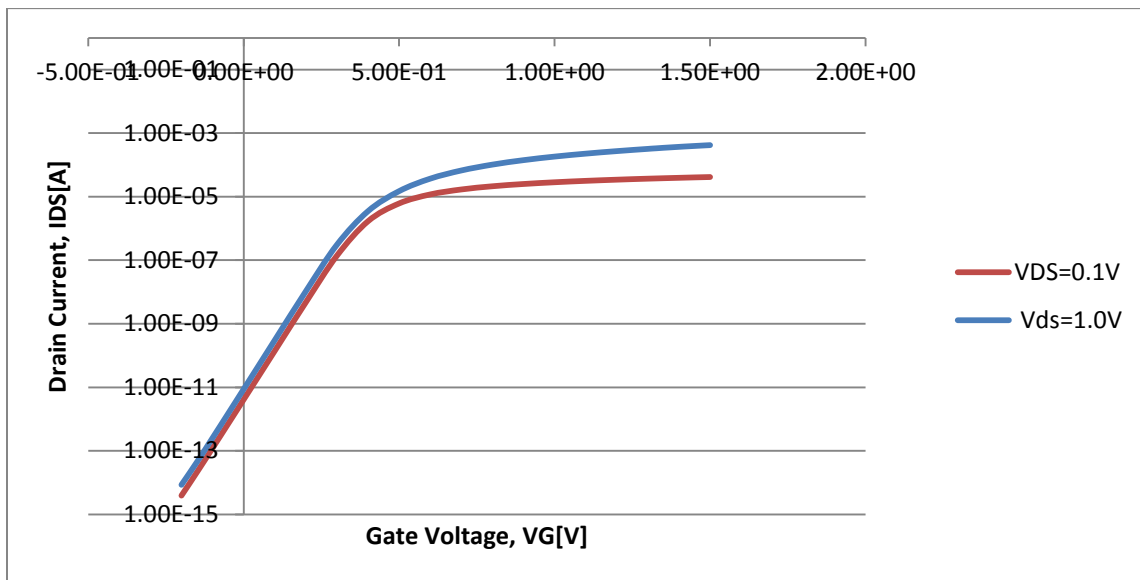


Figure 4.5: Simulated subthreshold characteristics of a surround gate vertical MOS transistor in log scale with gate width of 400nm, for 400nm, for $V_{DS}=0.1V$ and $1.0V$.

Three cut-lines have been made on the simulated 3D structure; one providing the cross sectional view of the device, the alternative one illustrates the top view, and the last one provides the diagonal view across the corners. The cross sectional cut is made at the midpoint through the pillar; the top view cut is made at the middle of the channel perpendicular to the pillar while the diagonal view cut is made at the 45° across the pillar, cutting both the opposite corners.

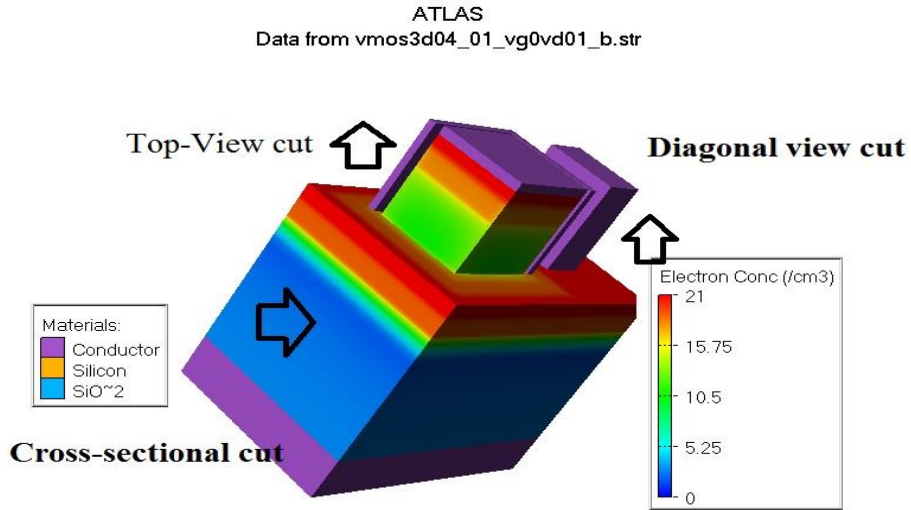
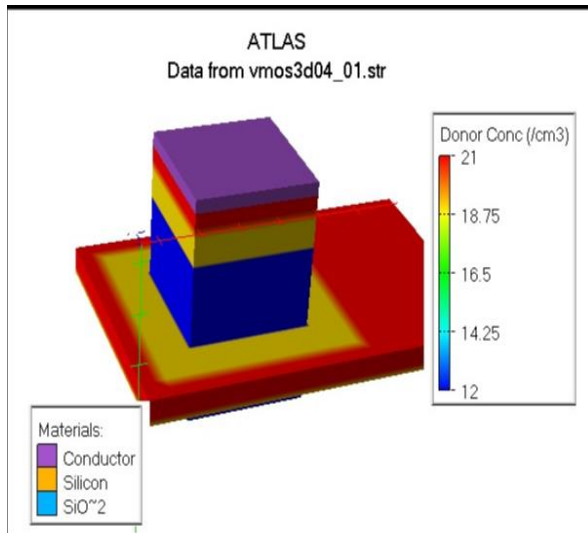
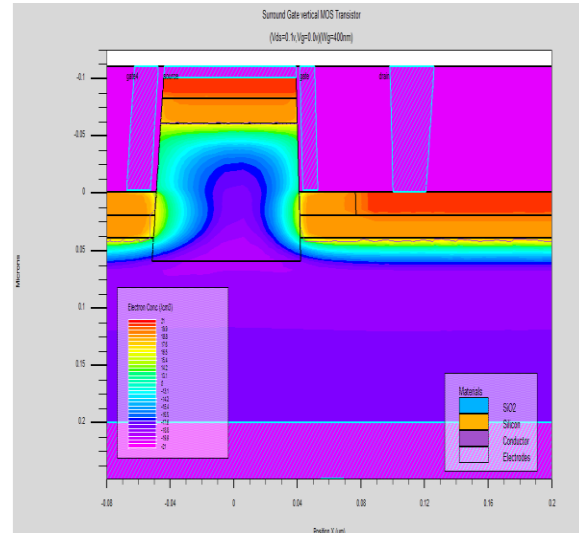


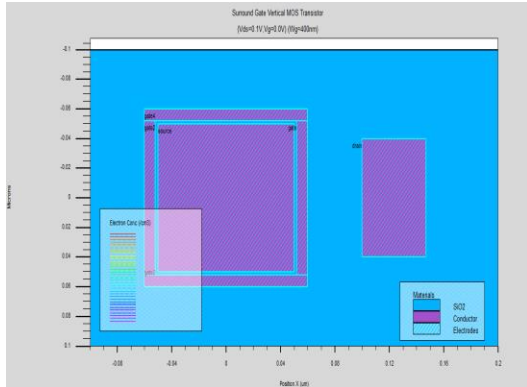
Figure 4.6: 3D zoomed view of electron concentration of the simulated surround gate vertical MOS transistor at $V_G=0.0V$ and $V_{DS}=0.1V$ oxide layer have been hidden for clarity and also made the cross sectional view, top view and the diagonal view.



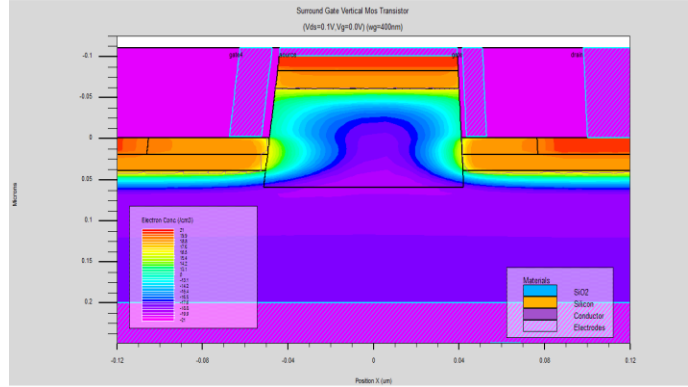
(a) 3D zoomed view of the pillar



(b) Cross-sectional View



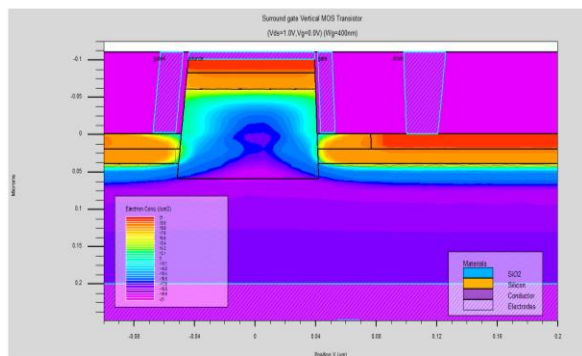
(c) Top View



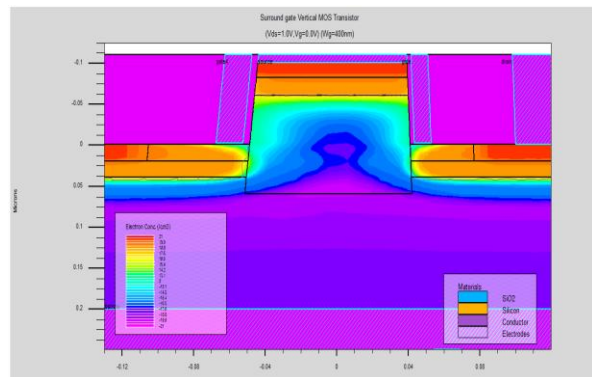
(d) Diagonal View

Figure 4.7: The a) 3D zoomed view of the pillar,(b) Cross-sectional View, (C) Top View (d) Diagonal View of the simulated surround gate vertical MOS transistor at $V_G=0.0V$ and $V_{DS}=0.1V$.

Figure 4.7 depicts the electron concentration of the structure at $V_G=0.0V$ and $V_{DS}=0.1V$. At this off-state region, the device is started to show weak inversion behaviour and the electron concentration has built-up and reached $10^{14}cm^{-3}$ at the corner as opposed to $10^{12}cm^{-3}$ at the non-corner part. The depletion layer has formed with increase of V_{DS} to 1.0V where $V_G=0.0V$. Leakage current has increased significantly and the electric field is estimated to be fairly high in the drain region and may cause band-to-band tunnelling which is not supported by ATLAS3D.



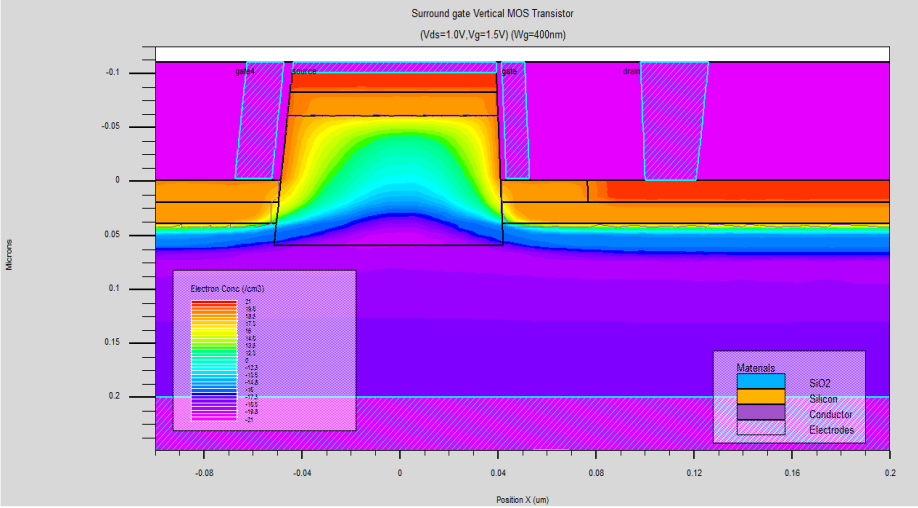
(a)Top View



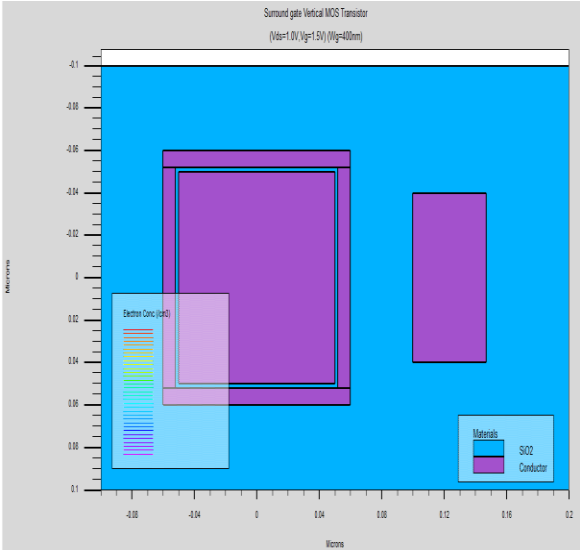
(b) Diagonal View

Figure 4.8: The a) Top View , (b) Diagonal View of the simulated surround gate vertical MOS transistor at $V_G=0.0V$ and $V_{DS}=0.1V$.

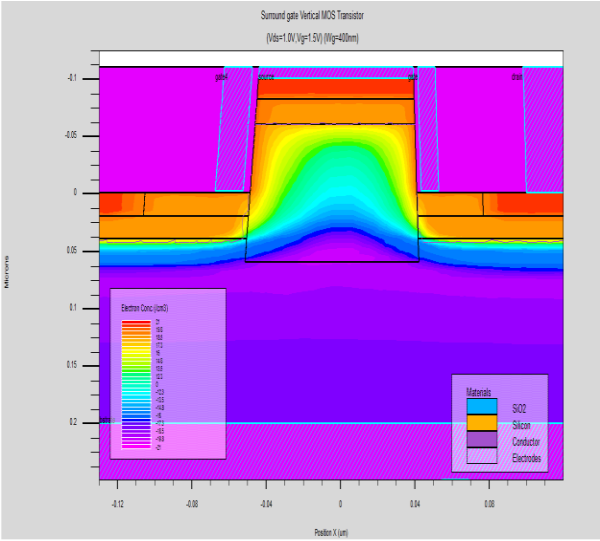
At $V_G=1.5V$ and $V_{DS}=1.0V$, the transistor is turned on and operates near the saturation region. By increasing the drain voltage, the depletion region will extend and create “depletion isolation effect” where the pillar is very thin [70], [71].



(a) Cross-sectional View

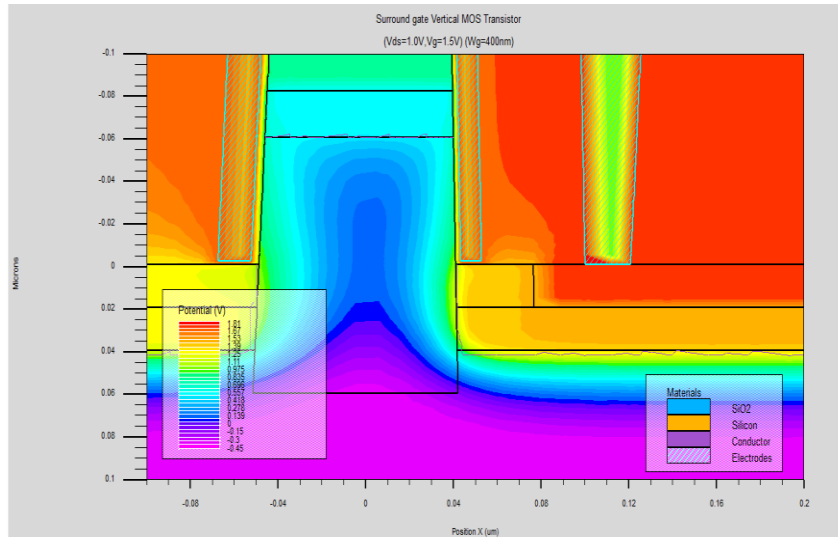


(b) Top View

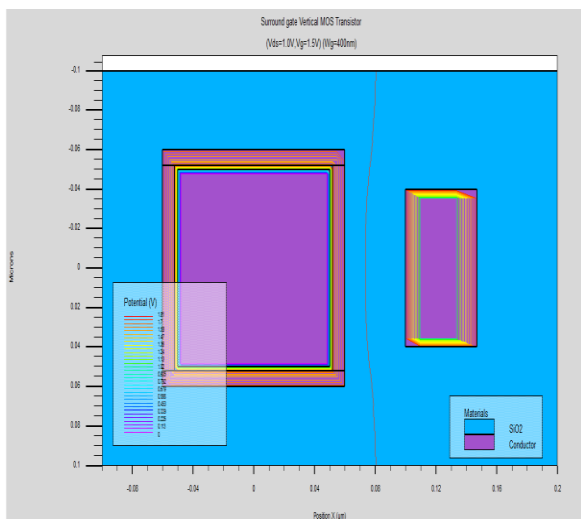


(c) Diagonal View

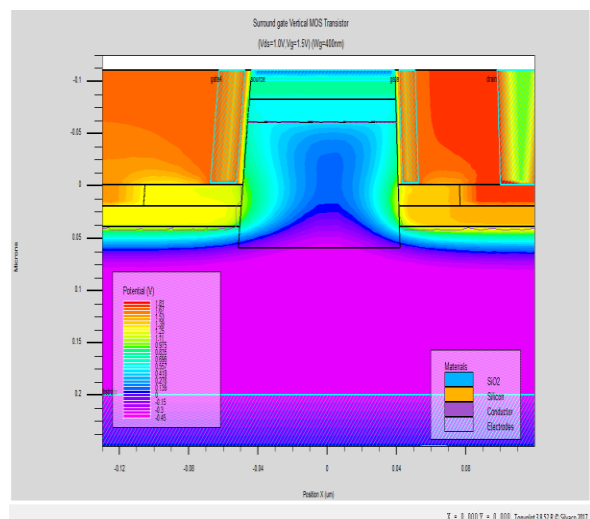
Figure 4.9: The a) Cross-sectional View b) Top View , C) Diagonal View of the simulated surround gate vertical MOS transistor at $V_G=1.5V$ and $V_{DS}=1.0V$.



(a) Cross-sectional view



(b) Top View



(c) Diagonal View

Figure 4.10: The a) Cross-sectional View b) Top View , c) Diagonal View of the simulated surround gate vertical MOS transistor at $V_G=1.5V$ and $V_{DS}=1.0V$.

Here, figure 4.10 illustrates that the potential line is higher at the corner because the threshold voltage is lower in the corners compared to the non-corner part.

4.4 Quadruple Gates Vertical MOS Transistor:

The quadruple gate structure was simulated with different gate widths like 400nm, 368nm, 320nm, 240nm and 160nm. To compare with the surround gate structure the gate widths of 400nm has been used. Quadruple gate structure design helps to eliminate the corner arrangement. While investigating the performance of transistor we noted that both transistor has performed very similarly and effectively emulate the effect of the corners. We can verify the result with near identical subthreshold curves. Figure 4.11 illustrate the similarities in subthreshold characteristics of both the surround gate and the 400nm quadruple gate structures.

The gate width of the quadruple gate structure is then varied and the simulated results were plotted. The width edge effect start to increase when the gate width started to decrease and the effects become clearer when the gate width is around 240nm and below. However, for the gate width of 368nm, the effects of corner still represent as they are next to each other. When the gate width is 240nm the quadruple gate operated individually because of the distance of adjacent gate increases. As a result the gate fringing field increases and accumulate at the edge of the gate. The threshold curves also show the analysis as the hump-like behaviour illustrated in the figure 4.13 and 4.14. Moreover it is notable that the subthreshold turn was lowest for the shortest gate width of quadruple gate structure with the lowest current drive. The drive current stays constant for the normalized drain current. When normalized but offset current increases linearly then the width of the gate is reduced exponentially down to 160nm. When V_{DS} is at 0.1V and drain current being normalized, however a strange behaviour was observed, where the increase of gate width doesn't correspond to expected increase in normalized drive current. Figure 4.15 and figure 4.16 both at $V_{DS} = 0.1V$ illustrate the subthreshold curves and the drain current.

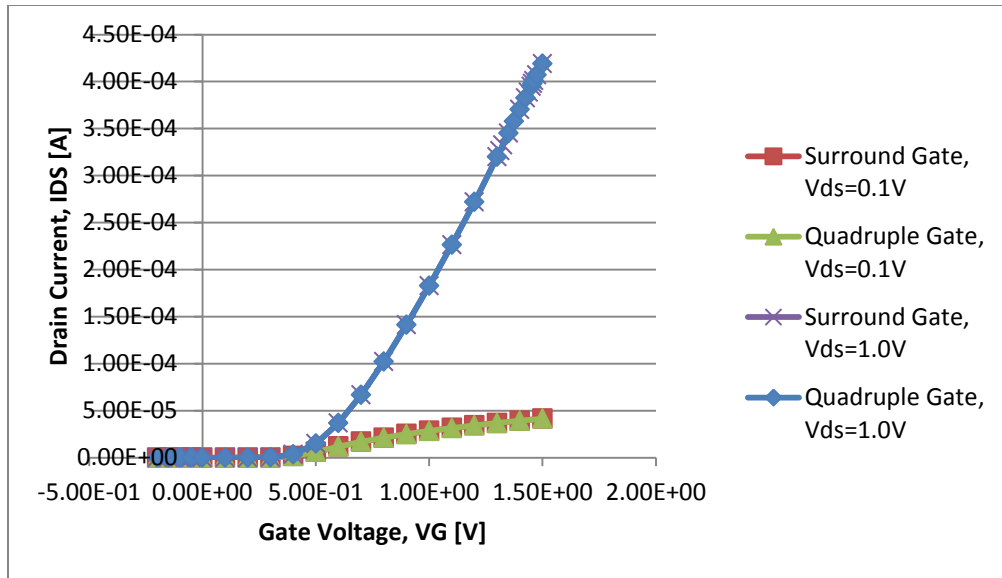
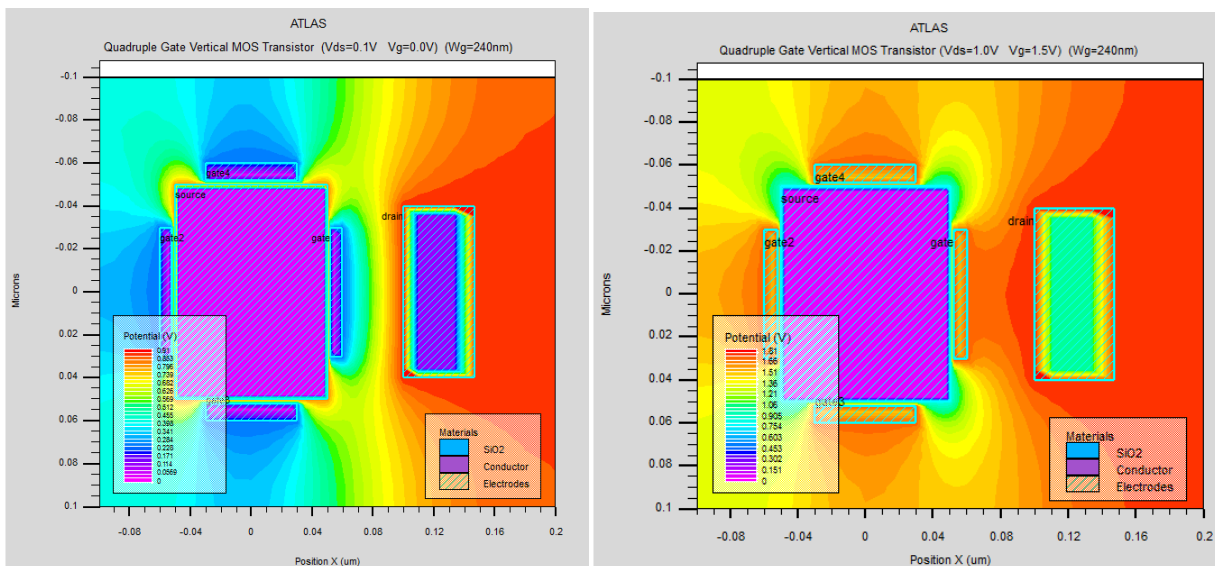


Fig 4.11: Simulated subthreshold characteristics of both the surround gate and quadruple gate vertical MOS transistor in linear scale with gate width of 400nm for V_{DS} is set at 0.1V and 1.0V



a) $V_g=0.0V$ and $V_{ds}=0.1V$

b) $V_g=1.5V$ and $V_{ds}=1.0V$

Fig 4.12: the top view of potential distribution of the simulated 240nm wide quadruple gate vertical MOS transistor at a) $V_g=0.0V$ and $V_{ds}=0.1V$ b) $V_g=1.5V$ and $V_{ds}=1.0V$

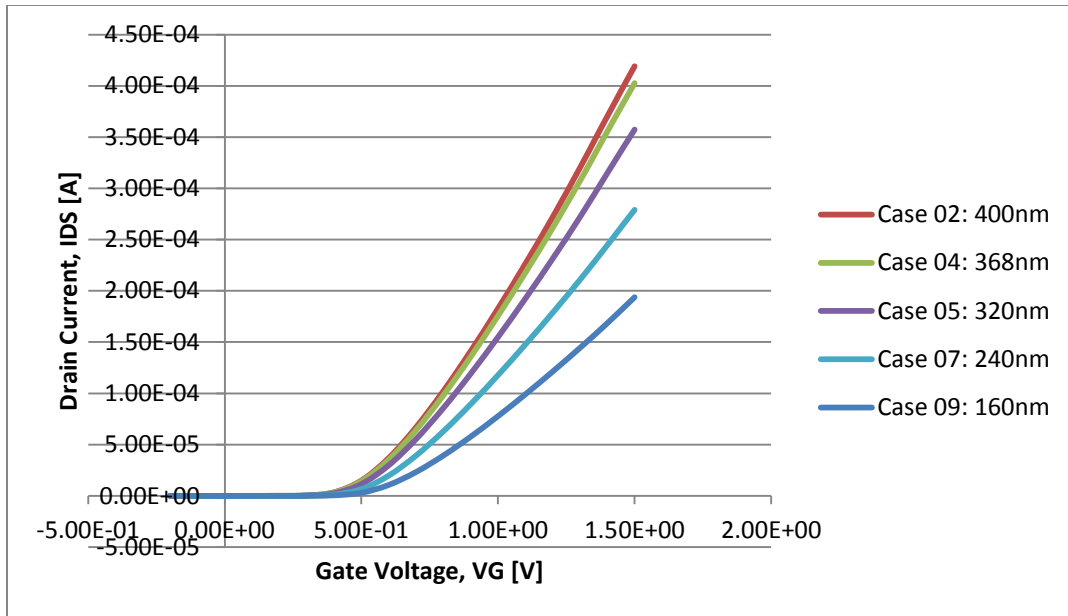


Fig 4.13: Simulated subthreshold characteristics of quadruple gate vertical MOS transistor in linear scale with various gate width when V_{DS} is set at 1.0V.

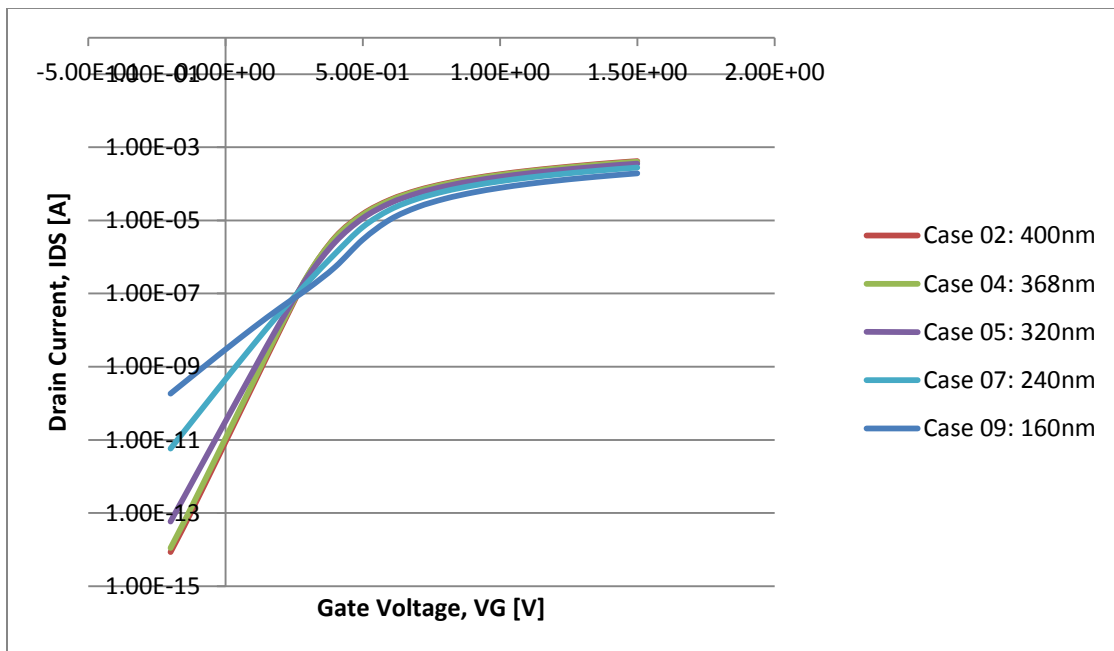


Fig 4.14: Simulated subthreshold characteristics of quadruple gate vertical MOS transistor in log scale with various gate width when V_{DS} is set at 1.0V.

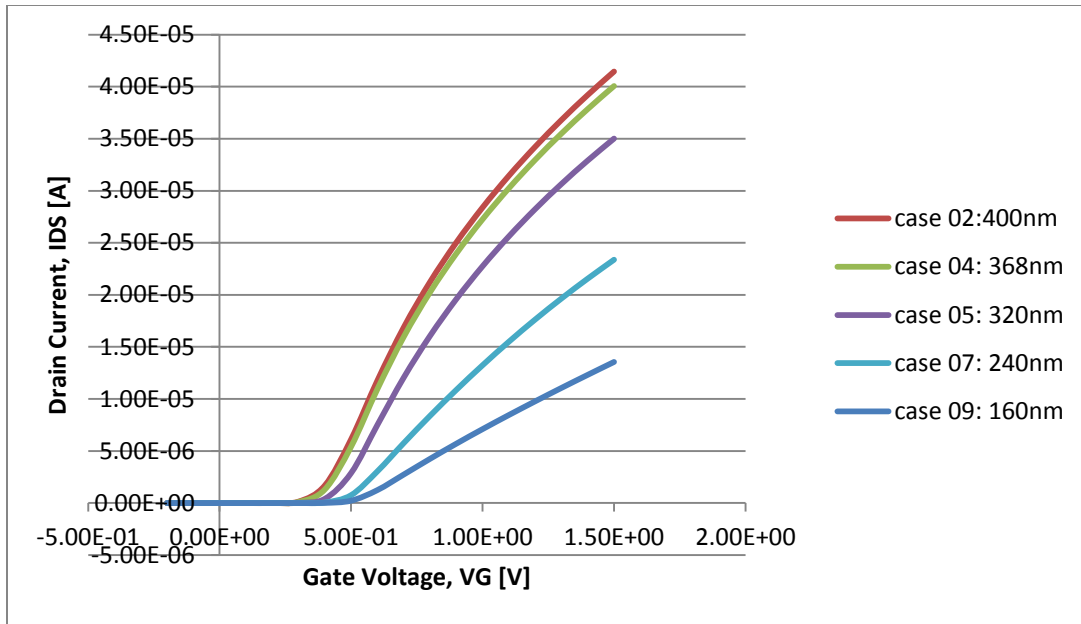


Fig 4.15: Simulated subthreshold characteristics of quadruple gate vertical MOS transistor in linear scale with various gate width when V_{DS} is set at 0.1V.

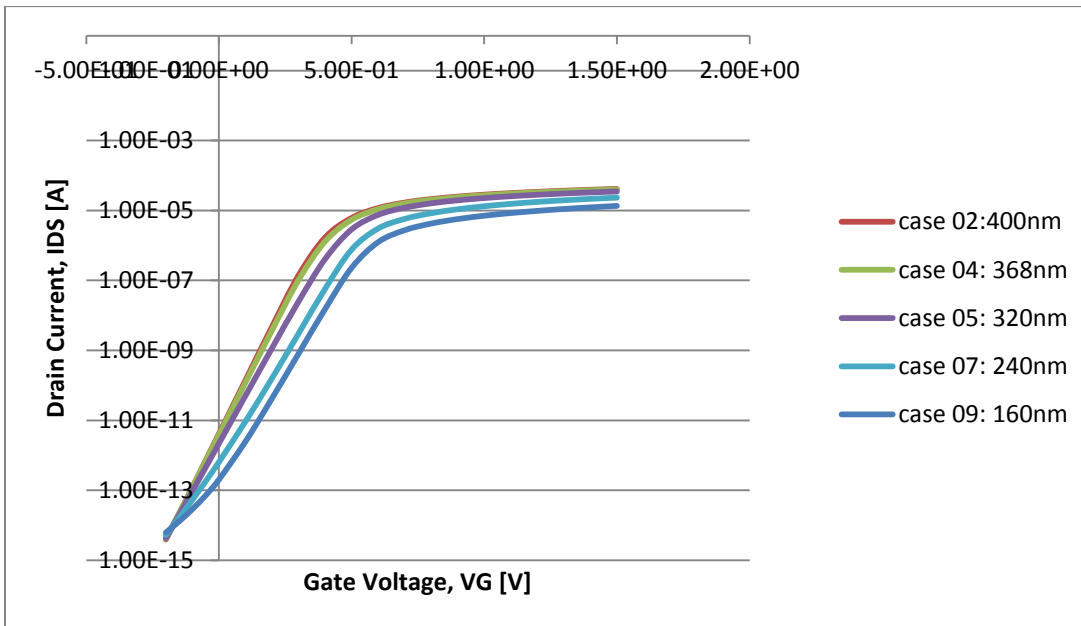


Fig 4.16: Simulated subthreshold characteristics of quadruple gate vertical MOS transistor in log scale with various gate width when V_{DS} is set at 0.1V.

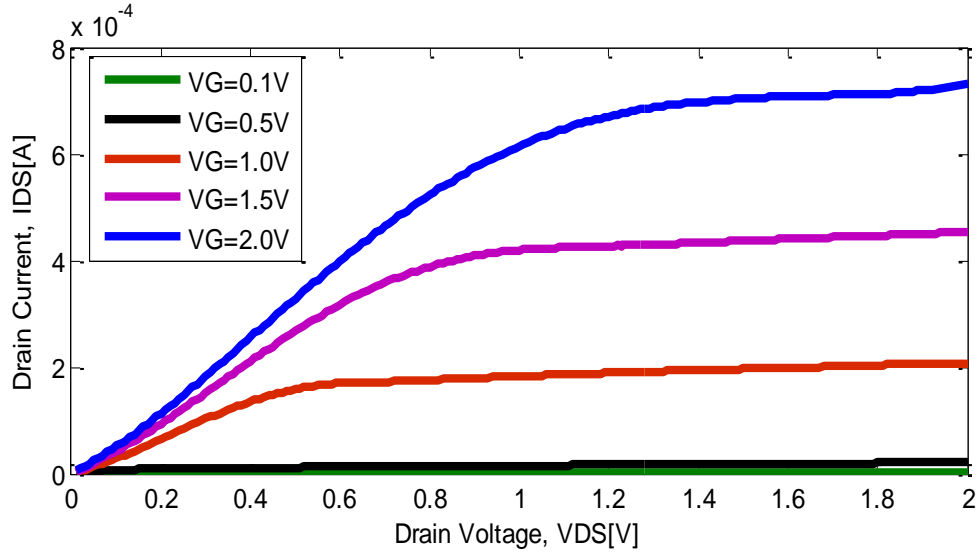


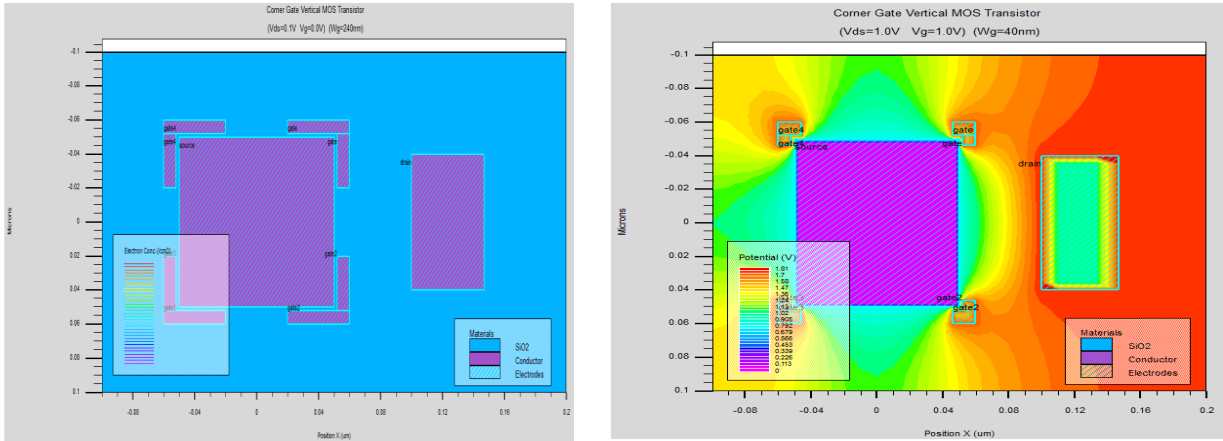
Figure 4.17: Simulated output characteristics of a Quadruple Gate Vertical MOS transistor in linear scale with gate Width of 400nm

Gate Width [nm]	V_{DS} [V]	S [mV/dec]
400	0.1	66.08
	1.0	65.82
368	0.1	67.56
	1.0	66.98
320	0.1	73.81
	1.0	75.42
240	0.1	81.78
	1.0	110.4
160	0.1	86.35
	1.0	132.06

Table 4.1: Subthreshold Slope of quadruple gate vertical MOS transistors with Various gate widths.

4.5 Corner Gates Vertical MOS Transistor:

Corner gate structure with various gate width of 240nm, 160nm, 80nm, 32nm were simulated and analysed. The transistor with smaller gate width is more reliable compared to larger gate width transistors for proximity of adjacent gates. The objective is to be able to isolate the corners from the non-corner part of the device, and analysed the subthreshold characteristics based on that.

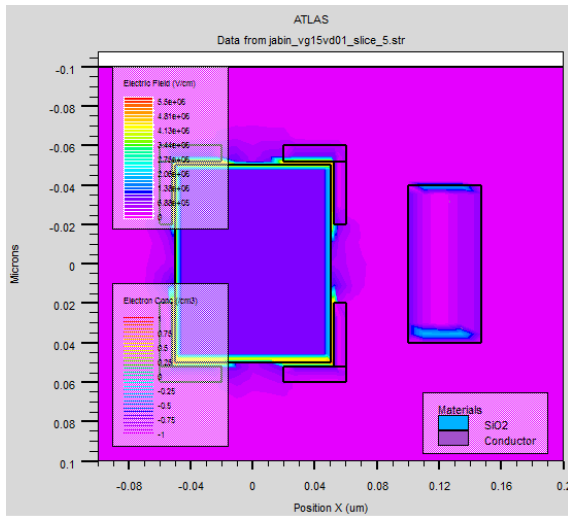


(a) $W_G=32\text{nm}$

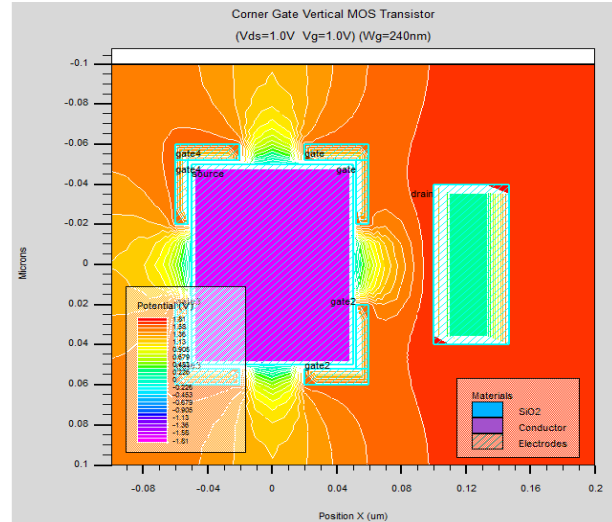
(b) $W_G=240\text{nm}$

Figure 4.18: The Top View of electron concentration of the simulated corner gate vertical MOS transistor at $V_G=0.3\text{V}$ and $V_{DS}=0.1\text{V}$,for gate width of a)32nm and b) 240nm

Figure 4.18, depicts the electron concentration of the corner gate transistors viewed from top, for transistors with gate width of 32nm and 240nm. V_{DS} of 0.1V is applied, while V_G is kept to zero. The wider gate width structure attracts more crowding of electrons at the corners.



(a) $W_G=32\text{nm}$



(b) $W_G = 240\text{nm}$

Figure 4.19: The Top View of electron concentration of the simulated corner gate vertical MOS transistor at $V_G=0.3\text{V}$ and $V_{DS}=1.0\text{V}$, for gate width of a) 32nm and b) 240nm

Figure 4.19 depicts the contribution of width edge effect compared to the corners of wider gate width transistor.

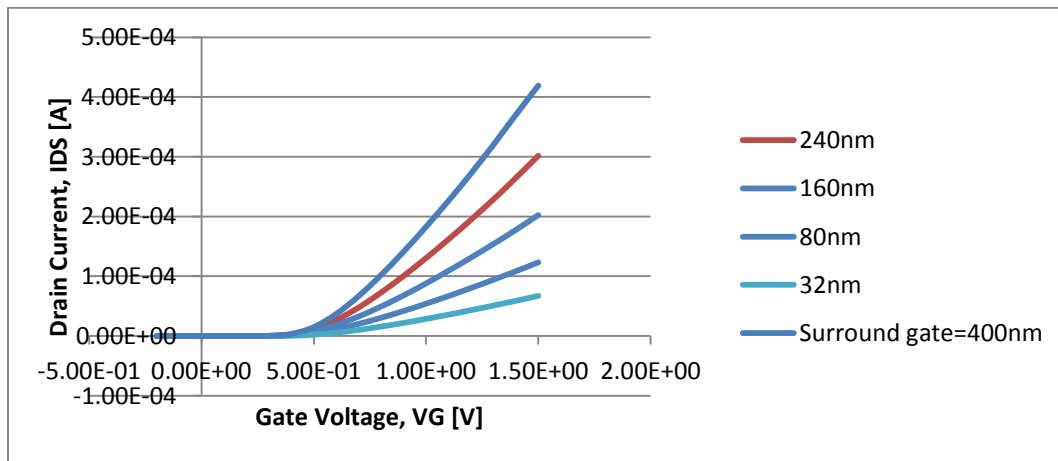


Figure 4.20: Simulated subthreshold characteristics of corner gate vertical MOS Transistors in linear scale with various gate widths, V_{DS} is set at 1.0V.

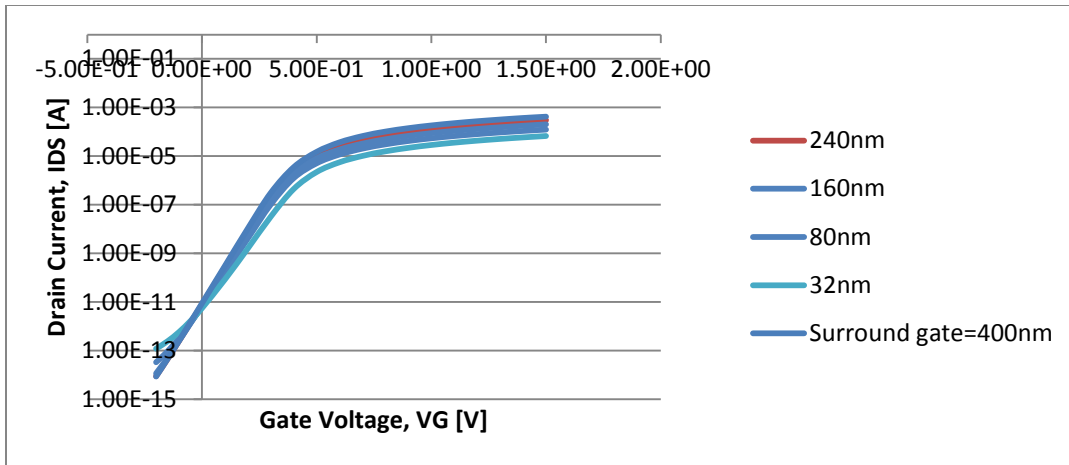


Figure 4.21: Simulated subthreshold characteristics of corner gate vertical MOS Transistors in log scale with various gate widths, V_{DS} is set at 1.0V.

The subthreshold curves in figure 4.20 and figure 4.21 illustrate the dependencies of drain current on gate width at $V_{DS}=1.0V$. The surround gate structure with a steeper subthreshold swing still out-performs the corner gate transistor. Though the corner device has a higher current drive per micron, suffer from heavy leakage at V_G lower than zero. At V_{DS} of 0.1V the corner devices has a higher current drive per micron, suffer from lower leakage at V_G . The reverse corner effect has negative V_G and higher V_{DS} .

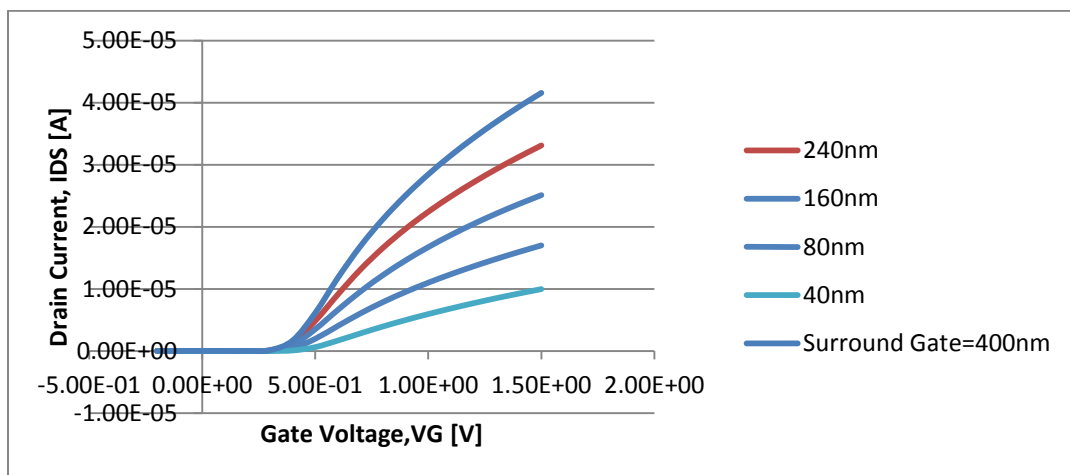


Figure 4.22: Simulated subthreshold characteristics of corner gate vertical MOS Transistors in linear scale with various gate widths, V_{DS} is set at 0.1V.

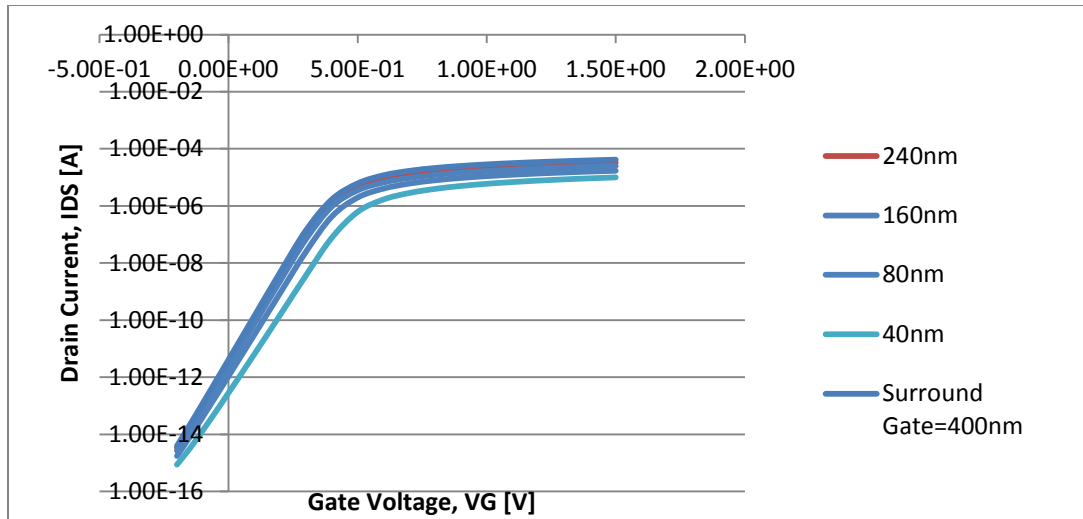


Figure 4.23: Simulated subthreshold characteristics of corner gate vertical MOS Transistors in log scale with various gate widths, V_{DS} is set at 0.1V.

The corner gate plays a vital role in transistor. Loosely we can say that the surround gate can be defined as the addition of the corner gate structure (corner part) and quadruple gate structure (non-corner part) though practically might not be direct addition.

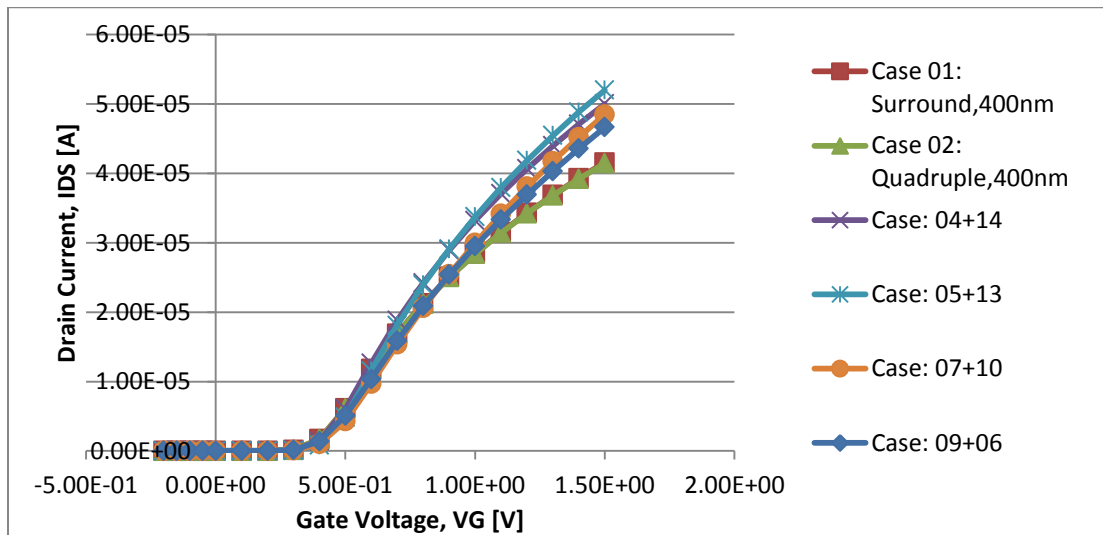


Figure 4.24: Simulated subthreshold characteristics of combination of joined Quadruple and corner gate vertical MOS transistor for an equivalent gate width of 400nm is at 0.1V.

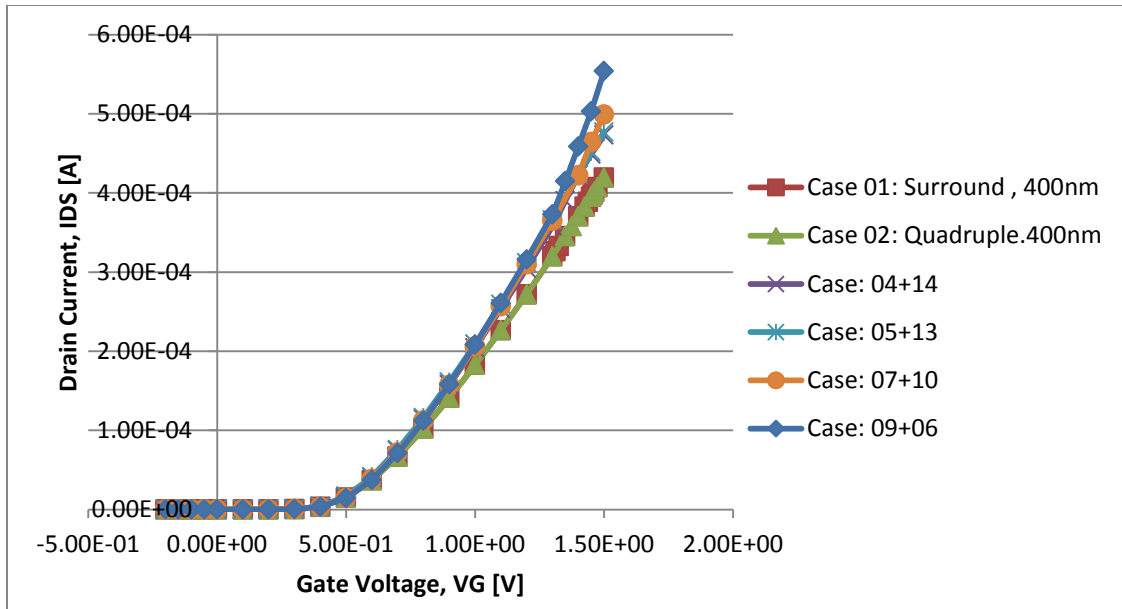


Figure 4.25: Simulated subthreshold characteristics of combination of joined Quadruple and corner gate vertical MOS transistor for an equivalent gate width of 400nm is at 1.0V.

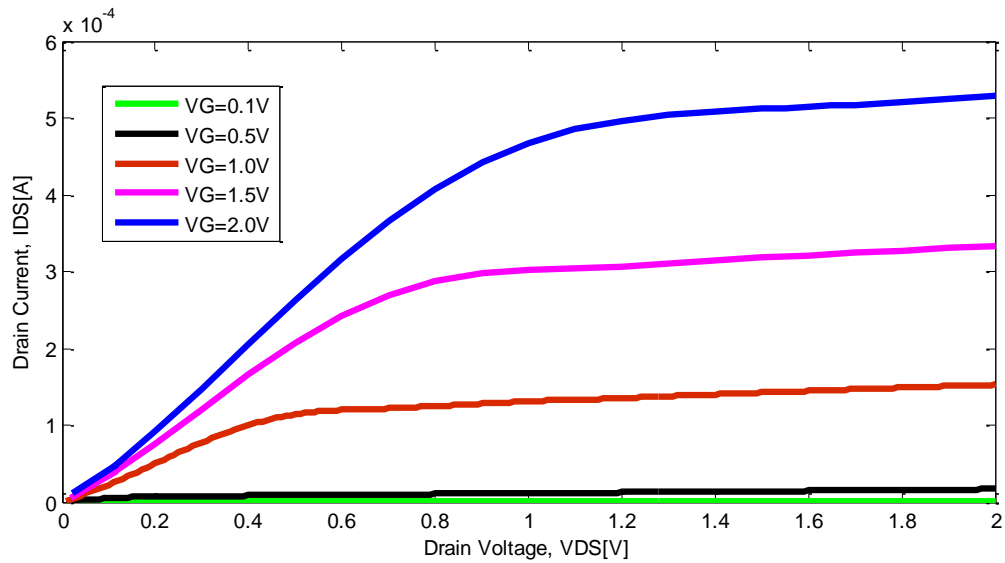


Figure 4.26: Simulated output characteristics of a Corner Gate Vertical MOS transistor in linear scale with gate Width of 240nm

Gate Width [nm]	V _{DS} [V]	S [mV/dec]
240	0.1	66.34
	1.0	66.42
160	0.1	67.06
	1.0	67.85
80	0.1	68.25
	1.0	71.81
32	0.1	73.19
	1.0	82.86

Table 4.2: Subthreshold Slope of corner gate vertical MOS transistors with Various gate widths.

The subthreshold curves illustrate that as the gate width of quadruple gate is decreased, the corner gate width increased and the leakage current is also increased when V_{DS} at 1.0V. The gate width of the corner gate used should be adequately small as to only consist of the influence from the corners and not inclusive the possible effect from the non-corner parts. In figure 4.27 indicates the contribution of drain current by the corner part and the non-corner part is analysed. With corner section occupying 240nm of the gate width, and the non-corner section taking 240nm, at 0.1V the drain current contribution of corner section is estimated to be 36.75% and at 1.0V the drain current contribution of corner section is estimated to be 2.30% founded on physical ratio. In figure 4.28 with corner section occupying 160nm of the gate width, and the non-corner section taking 160nm, at 0.1V the drain current contribution of corner section is estimated to be 85.43% and at 1.0V the drain current contribution of corner section is estimated to be 3.46% founded on physical ratio. In figure 4.29 corner gate and double gate taking 80nm at 0.1V the drain current contribution of corner section is estimated to be 97.44% and at 1.0V the drain current contribution of corner section is estimated to be 6.20% founded on physical ratio. The percentage contribution of corner part to drain current decreases as the gate voltage decreases and becomes least when V_G is at 0.3V, near the threshold voltage. If V_G is decreased, the percentage contribution of corner part increases.

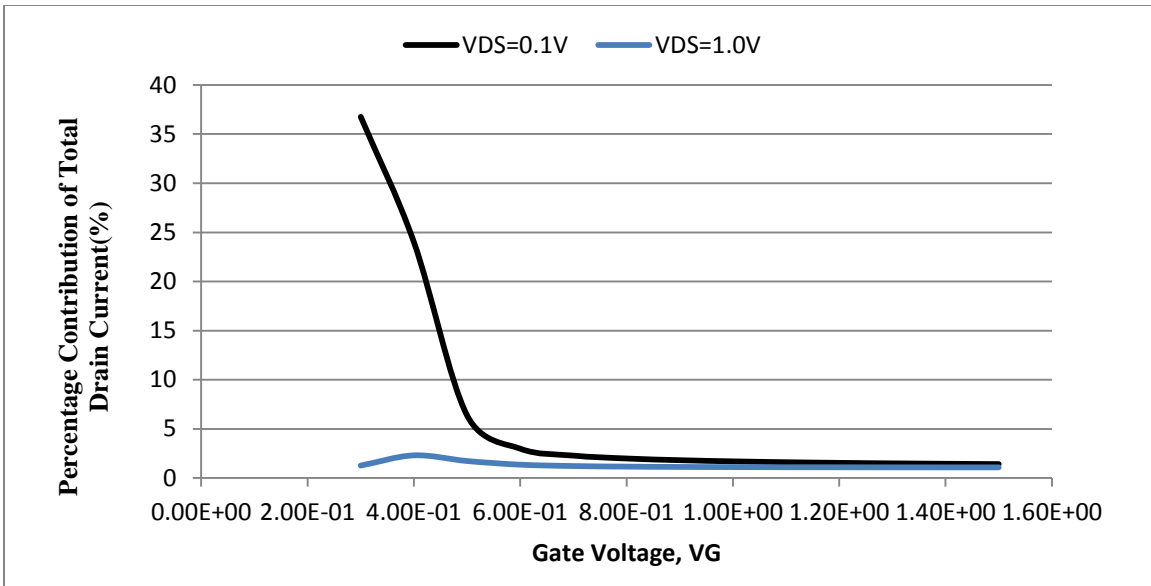


Figure 4.27: Percentage contribution of corner gate MOS with respect to quadruple gate MOS when gate structure is 240nm

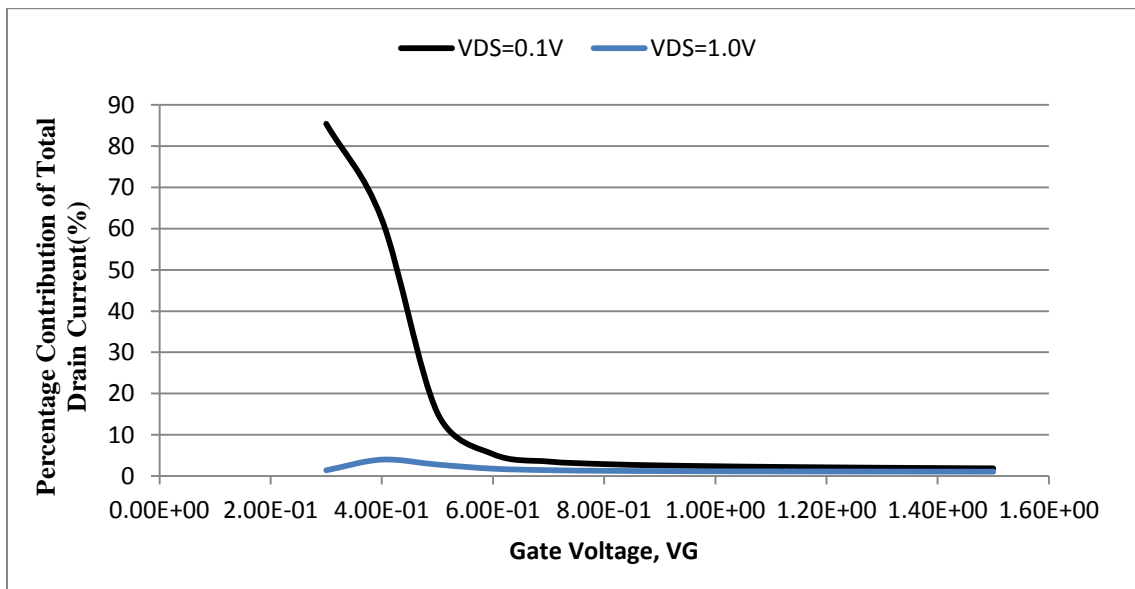


Figure 4.28: Percentage contribution of corner gate MOS with respect to quadruple gate MOS when gate structure is 160nm

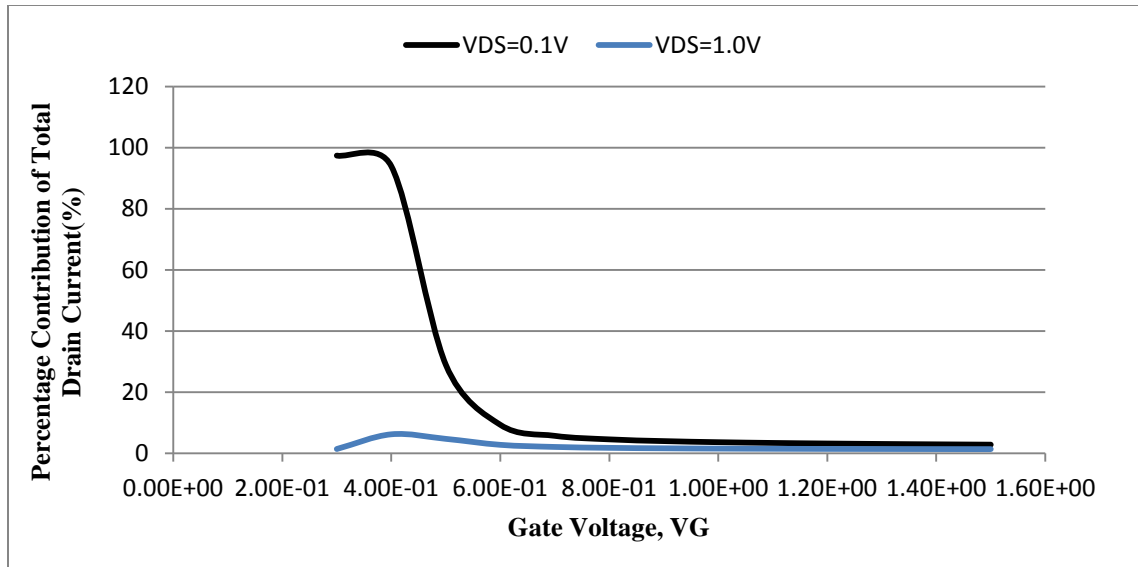


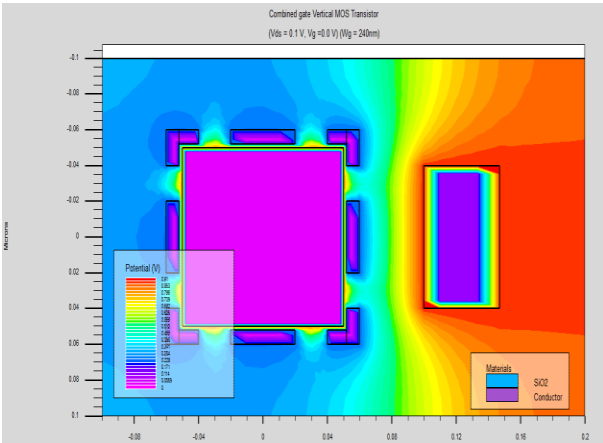
Figure 4.29: Percentage contribution of corner gate MOS with respect to double gate MOS when gate structure is 80nm

4.6 Combined Gates Vertical MOS Transistor

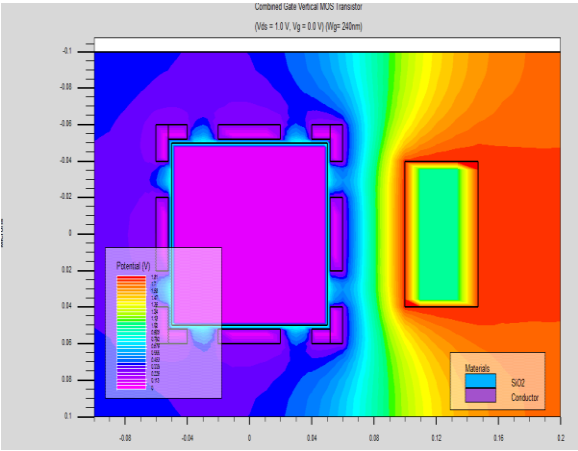
Shortly looking at the combined gate structure for comparison between quadruple and corner gate structure vertical transistors, can find an interesting result. The combined gate structure is comparatively impractical to be fabricated and is predicted to possess a raised edge result owing to raised proximity of adjacent gates. In figure 4.30 illustrated the top view of the potential distribution of a combined gate structure, at varied gate and drain voltages.

The structure of combined gate in figure 4.30 consists of 160nm wide of quadruple gates and 80nm wide of corner gates, thus giving a combined gate dimension of 240nm. Again in figure 4.31 depicts the subthreshold curves of the 160nm wide quadruple gates (case 09), the 80nm wide corner gates (case 13), the adding of the 2 gates (case 09 + 13), and the 240nm wide combined gate structure (case 06). The overall characteristic of the 2 gate structure is not additive.

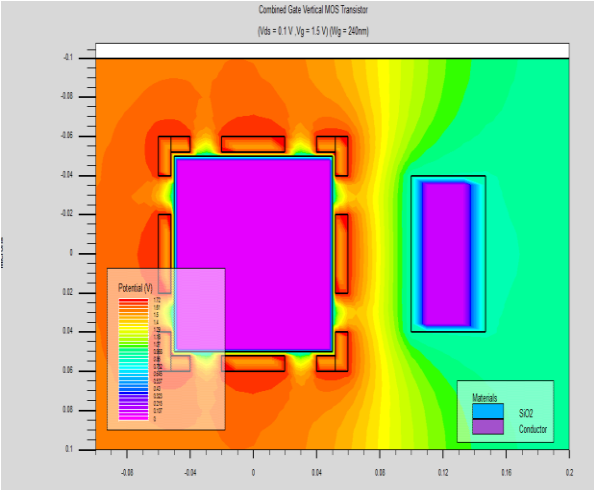
Figure 4.31 depicts the quadruple, corner and combined gate structures simulated at gate width of 240nm. The structure of corner gate provides a much better subthreshold characteristic with the simplest subthreshold swing. The structure of combined gate is appreciate corner gate structure, which could recommend that the corner half has been preponderantly the contributor to the drain current.



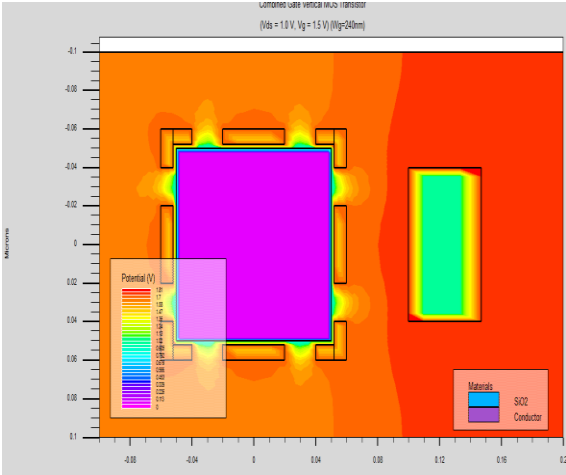
a) $V_{DS} = 0.1 \text{ V}$, $V_G = 0.0 \text{ V}$



b) $V_{DS} = 1.0 \text{ V}$, $V_G = 0.0 \text{ V}$



c) $V_{DS} = 0.1 \text{ V}$, $V_G = 1.5 \text{ V}$



d) $V_{DS} = 1.0 \text{ V}$, $V_G = 1.5 \text{ V}$

Figure 4.30: The top view of potential distribution of the simulated combined gate vertical MOS transistor at a) $V_{DS} = 0.1 \text{ V}$, $V_G = 0.0 \text{ V}$, b) $V_{DS} = 1.0 \text{ V}$, $V_G = 0.0 \text{ V}$, c) $V_{DS} = 0.1 \text{ V}$, $V_G = 1.5 \text{ V}$, d) $V_{DS} = 1.0 \text{ V}$, $V_G = 1.5 \text{ V}$.

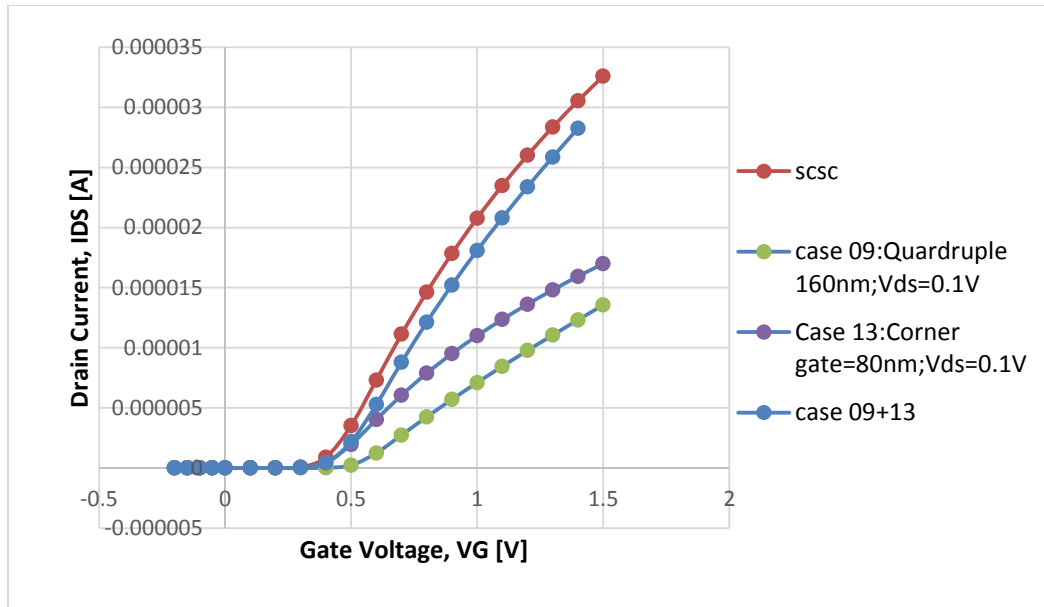


Figure 4.31: Simulated subthreshold curves in linear of the 160nm wide quadruple gates, the 80nm corner gates, the sum of the two, and the 240nm wide combined gate structure at $V_{DS} = 0.1$ V.

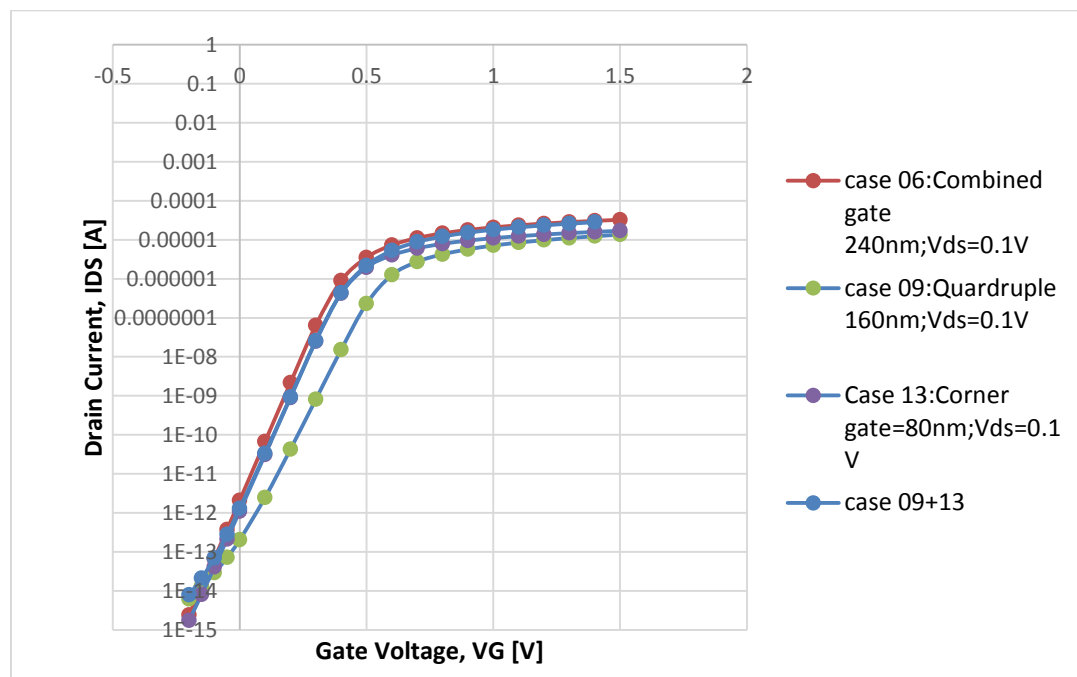


Figure 4.32: Simulated subthreshold curves in log of the 160nm wide quadruple gates, the 80nm corner gates, the sum of the two, and the 240nm wide combined gate structure at $V_{DS} = 0.1$ V.

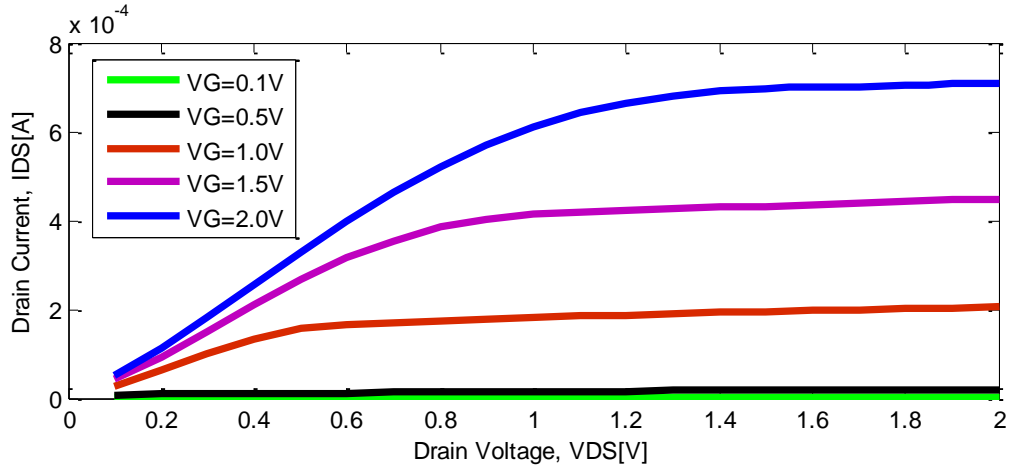


Figure 4.33: Simulated output characteristics of a Combined Gate Vertical MOS transistor in linear scale with gate Width of 368nm

Gate Width [nm]	V_{DS} [V]	S [mV/dec]
368	0.1	65.9
	1.0	66.17
240	0.1	66.86
	1.0	67.18

Table 4.3: Subthreshold Slope of combined gate vertical MOS transistors with various gate widths.

4.7 Single and Double Gates Vertical MOS Transistor:

Single, double and quadruple gate structures are simulated and compared to research the impact of the multiple gate to the subthreshold performance of the transistors. The structure of single gate has a gate width of 40nm, with the structure of double gate effectively doubled to 80nm wide, and therefore the structures of quadruple gate quadrupled to 160nm wide. In figure 4.34 depicts the subthreshold curves normalized to gate width, for the single, double and quadruple gate structures at $V_{DS} = 0.1$ V. The doubling impact is somewhat evident because the double gate structure has effectively doubled the drain current as that of single, shown by the nearly identical normalized I_{DS} . However, once the gate has been quadrupled, the effective drain current increased more than four times, possible due to effective contribution from adjacent gates.

In figure 4.38 and in figure 4.39 depict the top views of the single and double gate, with electron concentration and potential distribution severally, once the transistors are totally turned on. It is interesting to look at that the structures do have an impact on the corners of the pillar, particularly the structure of single gate, despite being isolated or separated so much apart. The alternative 2 corners of the structure of single gate appears to be crowded with electrons and switch on earlier, that is peculiar because the space opposite to the single gate must not be turned on in any respect, as there is no gate settled in this space. One possible reason can be the proximity of the drain contact that is barely 50nm apart and is biased at VDD of 1.0 V. However, this result is not evident all told the previous analysis, and should not be a true risk once there are gate contacts nearer to it space, hindering the drain contact to own any essential contributions to the drain current, as illustrated in Figure 4.39 with a $V_{DS}=0.1$ V and $V_G = 1.5$ V.

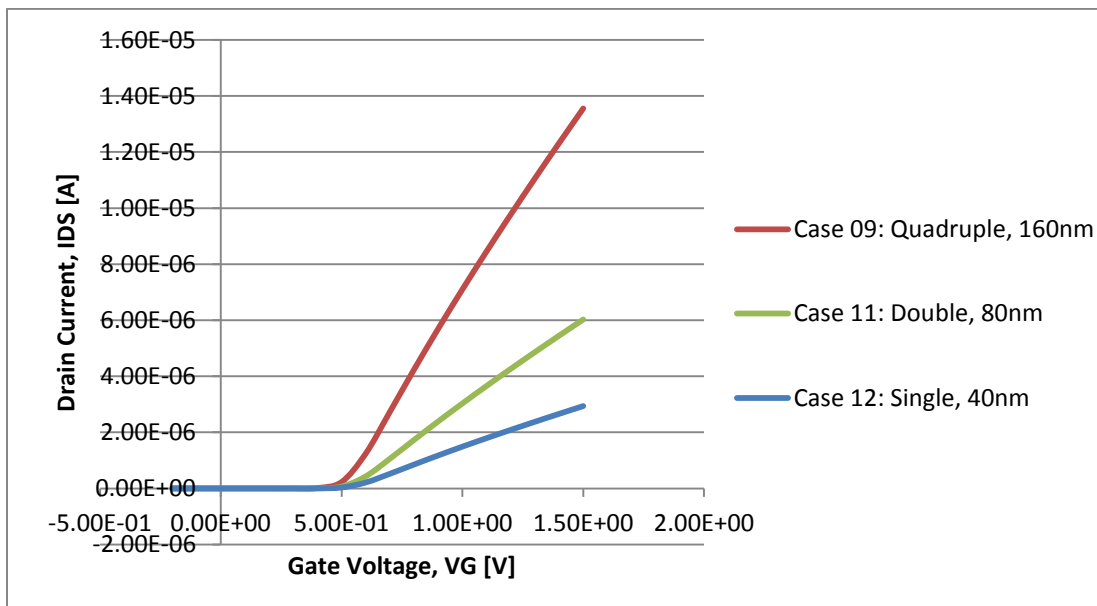


Figure 4.34: Simulated subthreshold characteristics of single, double and quadruple gate vertical MOS transistor in linear scale V_{DS} is at 0.1 V

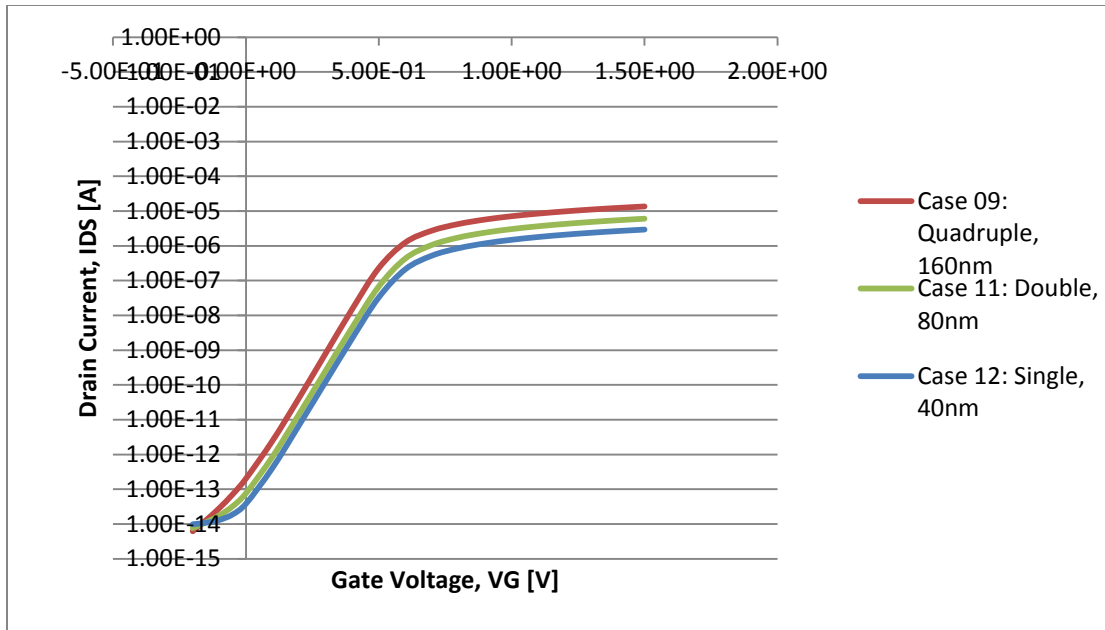


Figure 4.35: Simulated subthreshold characteristics of single, double and quadruple gate vertical MOS transistor in log scale V_{DS} is at 0.1 V

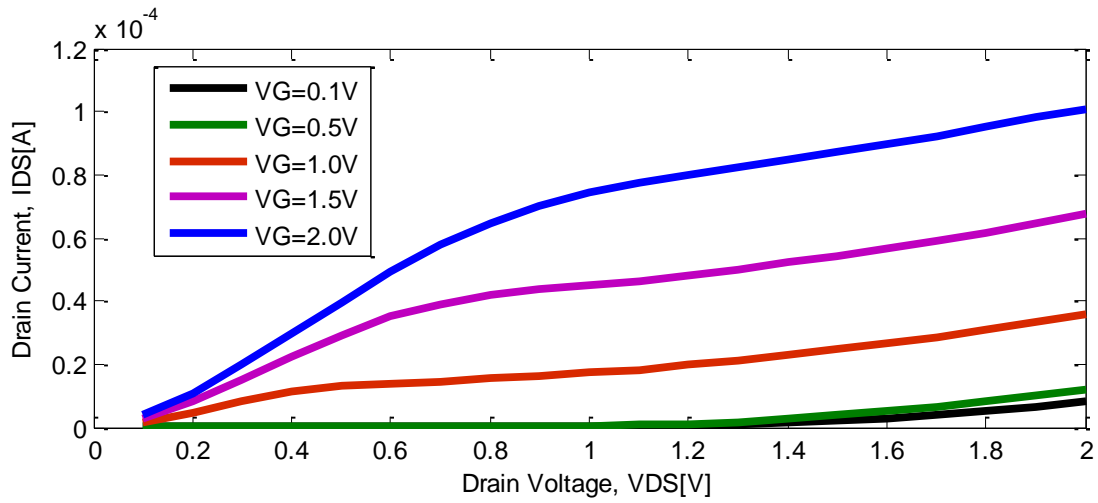


Figure 4.36: Simulated output characteristics of a Single Gate Vertical MOS transistor in linear scale with gate Width of 40nm

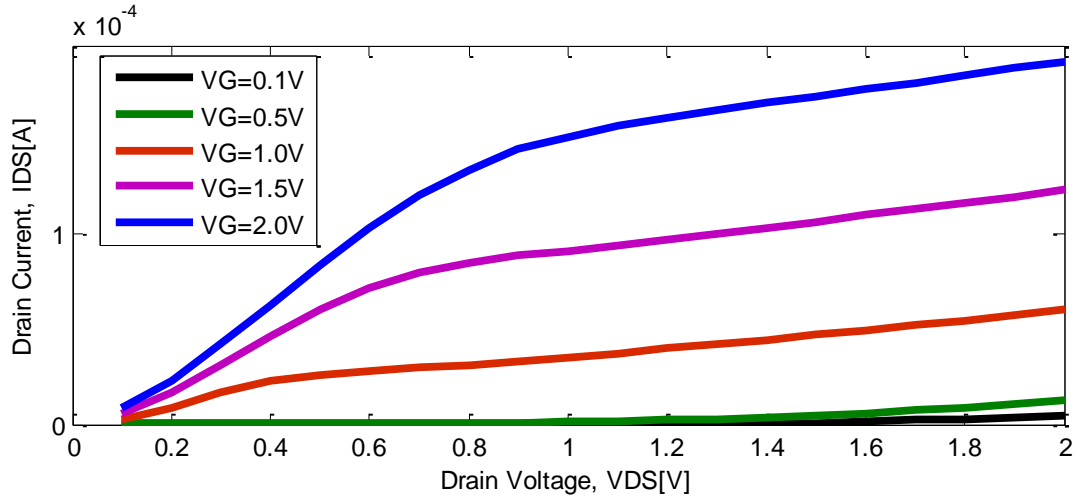
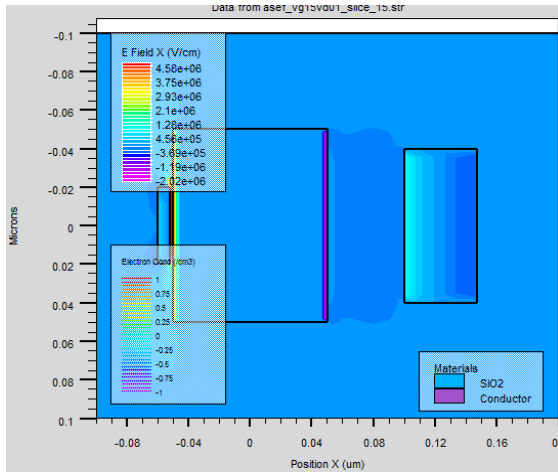


Figure 4.37: Simulated output characteristics of a Double Gate Vertical MOS transistor in linear scale with gate Width of 80nm

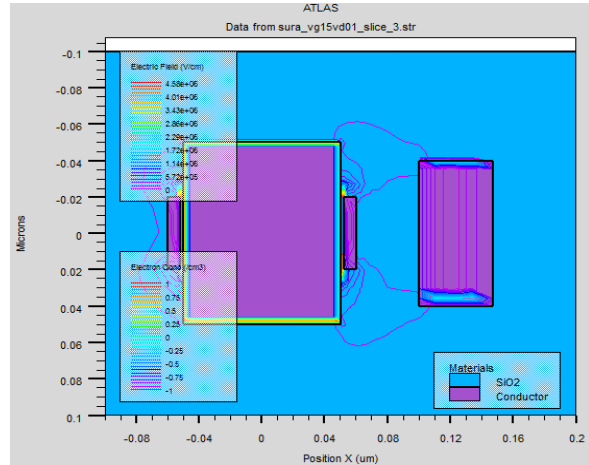
Single gate			Double gate		
Gate Width [nm]	V_{DS} [V]	S [mV/dec]	Gate Width [nm]	V_{DS} [V]	S [mV/dec]
40	0.1	88.87	80	0.1	87.49
	1.0	154.29		1.0	150.4

Table 4.4: Subthreshold Slope of single and double gate vertical MOS transistors.

The structure of double gate, despite having 2 gates separated fairly way apart, still shows a considerable corner impact. This, then, might counsel that the corners do get simply affected attributable to its convex physical nature. Hence, it is essential to hold out additional work to verify the role of the proximity of adjacent gates in moving the behaviour of the corners of the pillar, Effectively, ways in which of dominant the corners is advised, probably by rounding error the corners, or by means that of threshold voltage maintain at the corners exploitation corners implant or strategic placement of the gates.

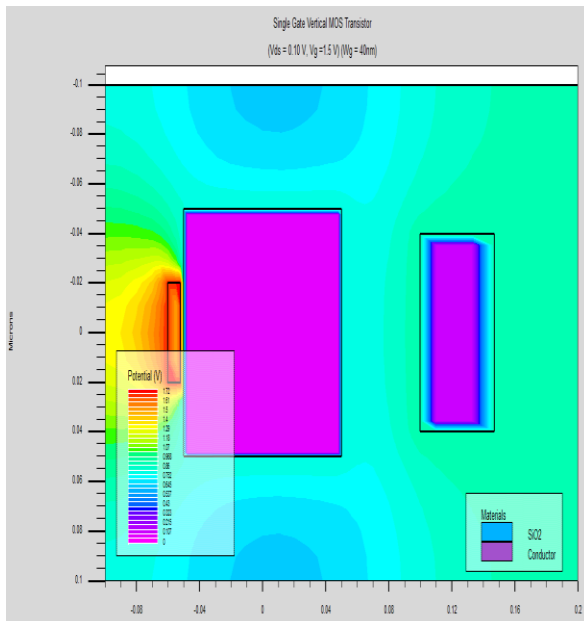


a)Single Gate

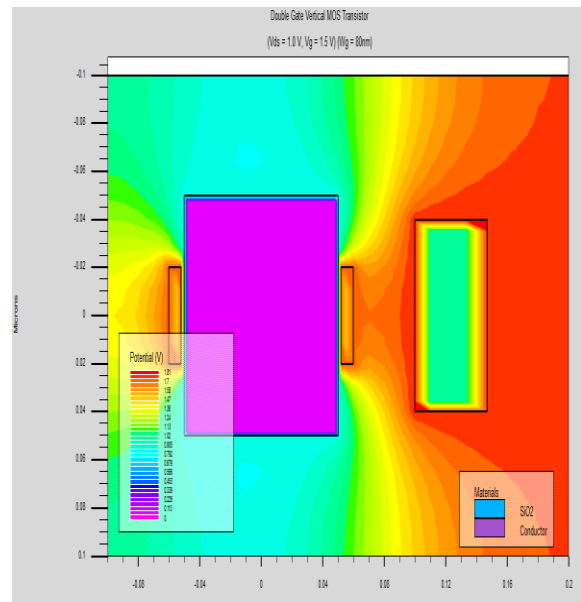


b) Double Gate

Figure 4.38: The top view of electron concentration of the simulated a)Single Gate and b) Double Gate vertical MOS transistor at $V_G = 0.3 \text{ V}$ and $V_{DS} = 0.1 \text{ V}$.

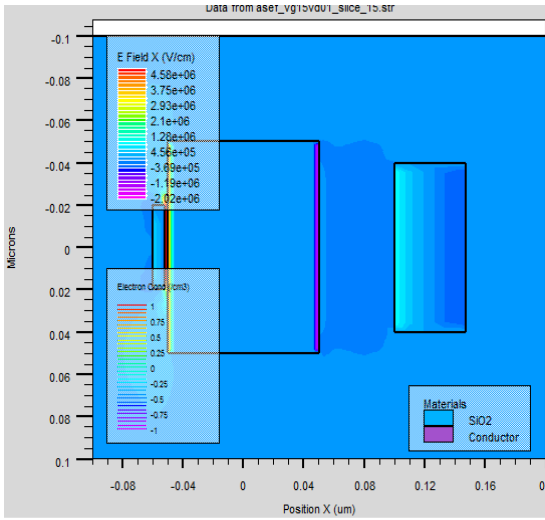


a)Single Gate

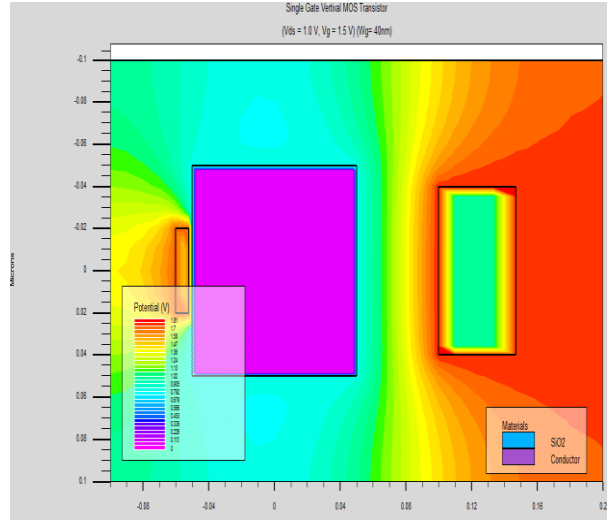


b) Double Gate

Figure 4.39: The top view of potential distribution of the simulated a)Single Gate and b) Double Gate vertical MOS transistor at $V_G = 1.5 \text{ V}$ and $V_{DS} = 1.0 \text{ V}$.



a) Single Gate



b) Double Gate

Figure 4.40: The top view of the simulated Single Gate vertical MOS transistor at $V_G = 1.5$ V and

$V_{DS} = 1.0$ V, for a) electron concentration and b) potential distribution.

Chapter 5

Conclusion

We have investigated the possible corner effects of vertical MOS transistor by using 3-dimensional device simulator, ATLAS3D from Silvaco TCAD with simplified device features. Different types of gate structure and gate width have been simulated and investigated. The gate length, L_G was kept constant 60nm, the gate oxide of 2nm thick and pillar size of 100nm×100nm×100nm for all the simulation. The surround gate vertical MOS transistor with gate width of 400nm shown early turn on effect at the corners and exhibited a threshold voltage lowering at the corners.

The quadruple gate and corner gate vertical MOS transistor were simulated and analysed for corner effects and wide edge. When the gate width is increased, the current drive increases but the off state current decreases. The quadruple gate structure was joined with the corner gate structure result in 400nm wide surround gate structure. The combination of 368nm quadruple gate with 32nm corner gate which results in similarity with the simulated 400nm surround gate structure. From the corner and non-corner parts the contribution of total drain current was estimated. With corner section occupying 240nm of the gate width, and the non-corner section taking 240nm, at 0.1V the drain current contribution of corner section is estimated to be 36.75% and at 1.0V the drain current contribution of corner section is estimated to be 2.30% founded on physical ratio. With corner section occupying 160nm of the gate width, and the non-corner section taking 160nm, at 0.1V the drain current contribution of corner section is estimated to be 85.43% and at 1.0V the drain current contribution of corner section is estimated to be 3.46% founded on physical ratio. In corner gate and double gate taking 80nm at 0.1V the drain current contribution of corner section is estimated to be 97.44% and at 1.0V the drain current contribution of corner section is estimated to be 6.20% founded on physical ratio. The corner of the pillar turned on earlier than the non-corner part which results in a significant contribution of total drain current when the device is biased above the threshold voltage.

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Chapter 6

Appendix A

A.1 Surround Gate Vertical MOS Transistor

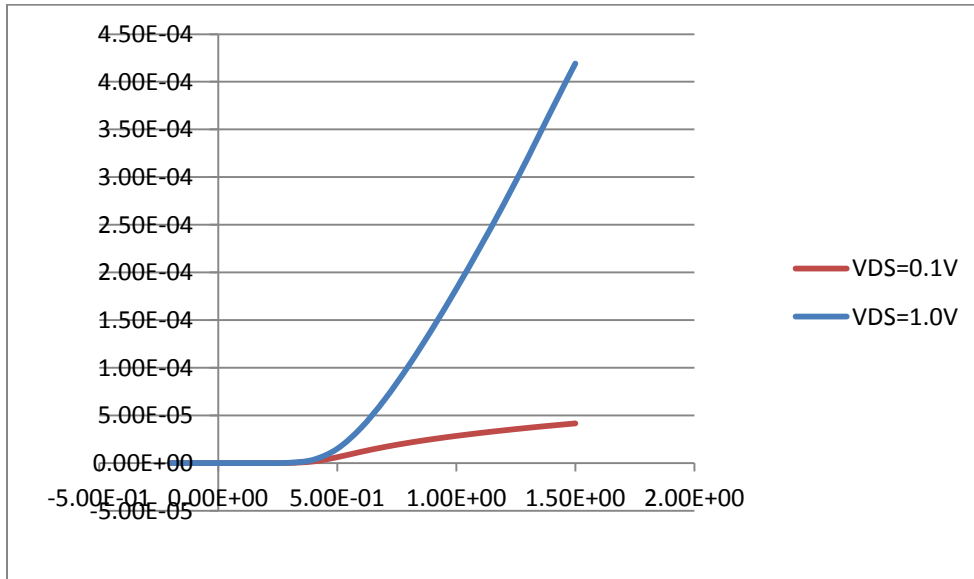


Fig 01: I_{ds} vs V_{gs} curves(linear)

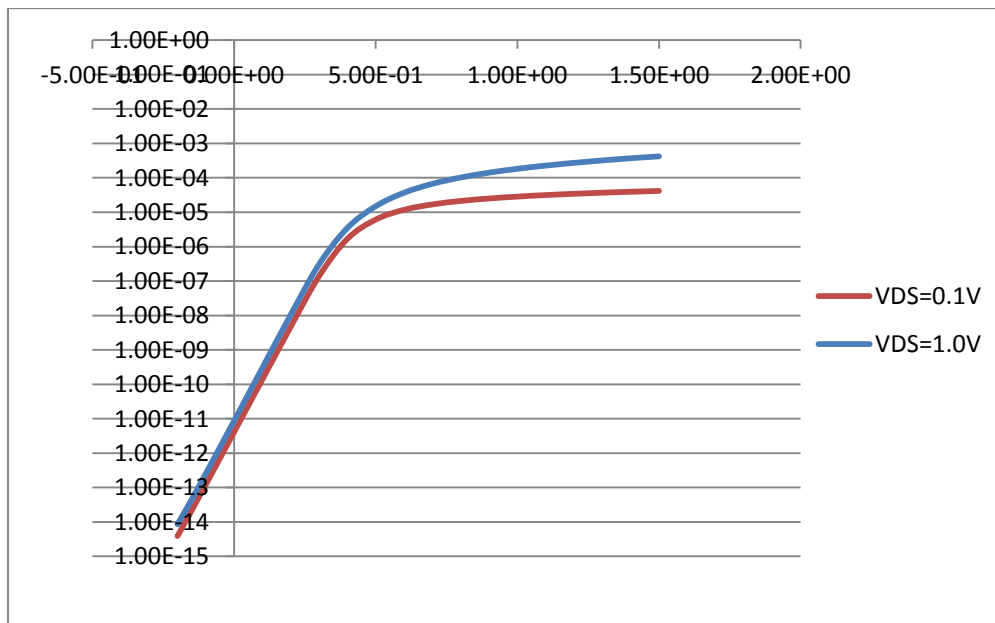


Fig 02: I_{ds} vs V_{gs} curves(log)

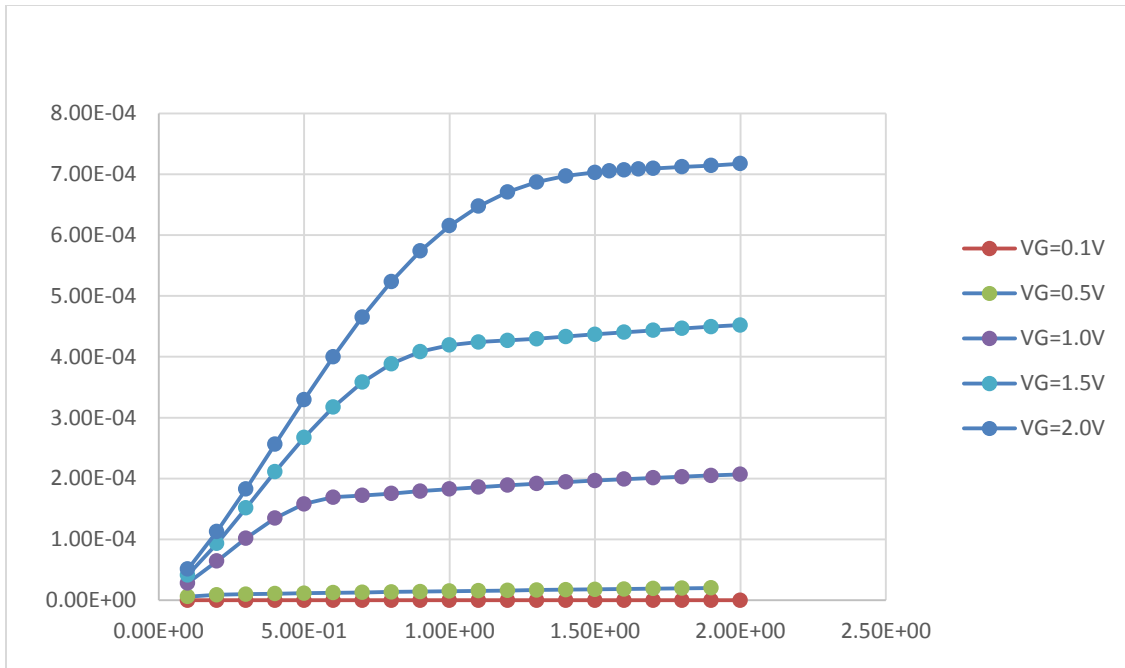


Fig 03: Ids vs Vds curves

A.2 Quadruple Gate Vertical MOS Transistor

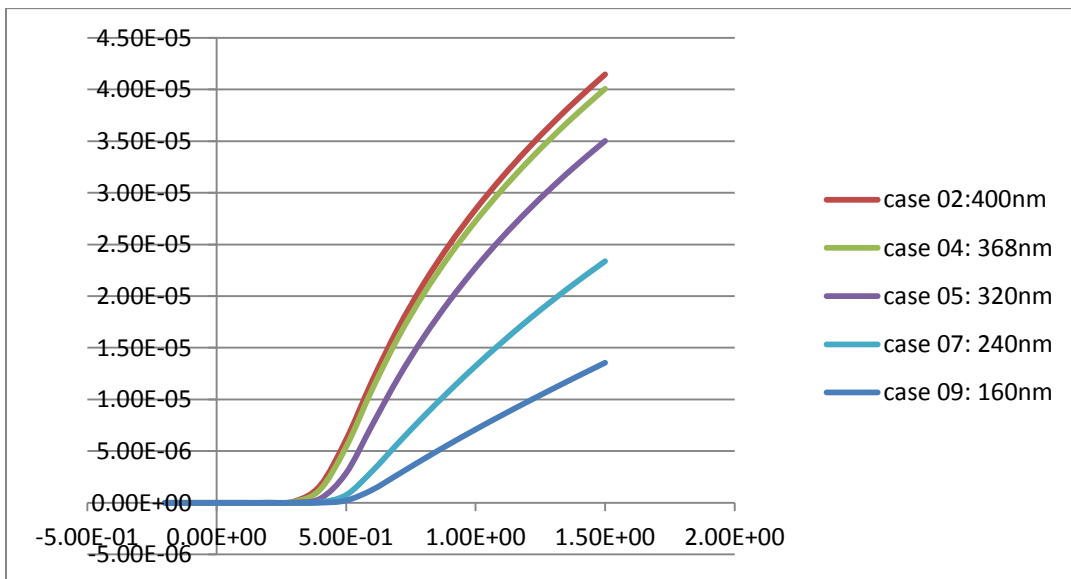


Fig 04: Ids vs Vgs curves for $V_{DS}=0.1V$ (linear)

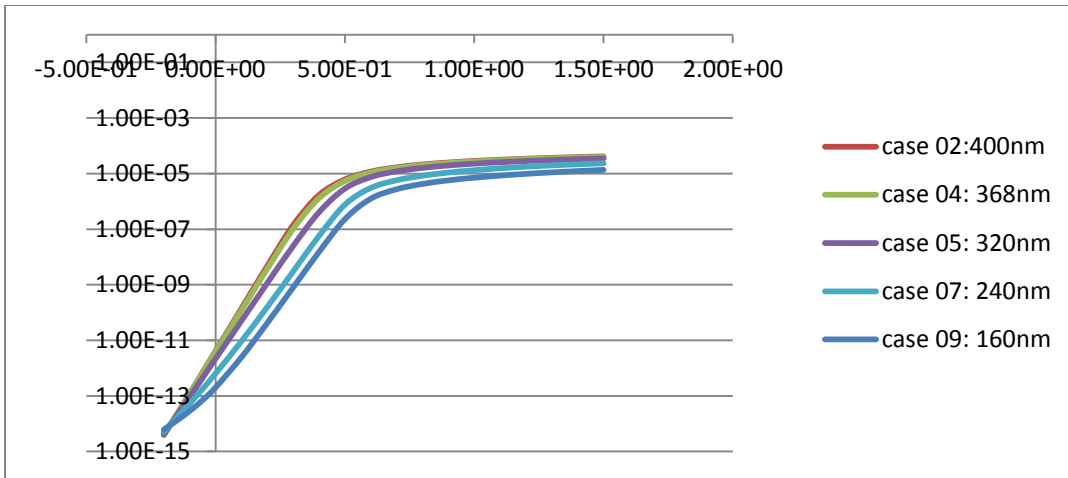


Fig 05: Ids vs Vgs curves for $V_{DS}=0.1V$ (log)

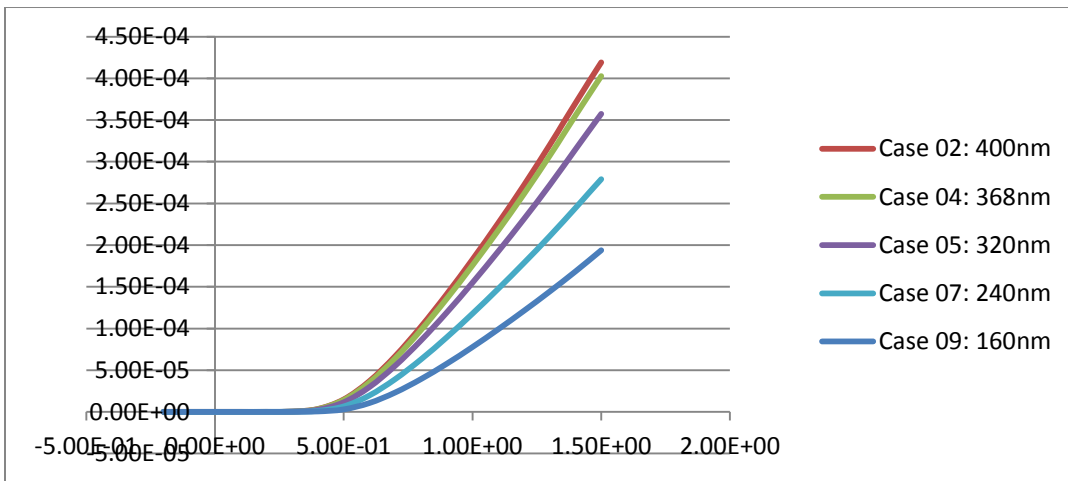


Fig 06: Ids vs Vgs curves for $V_{DS}=1.0V$ (linear)

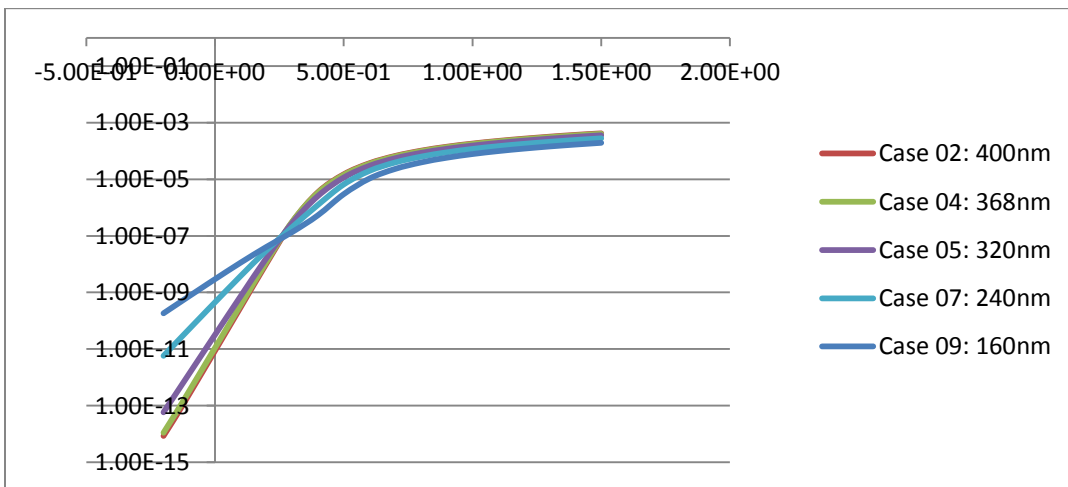


Fig 07: Ids vs Vgs curves for $V_{DS}=1.0V$ (log)

A.3 Corner Gate Vertical MOS Transistor

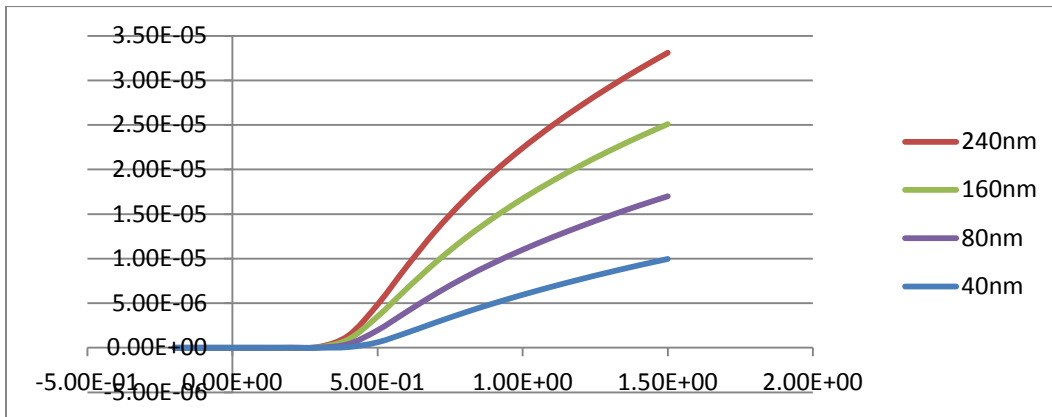


Fig 08: Ids vs Vgs curves for $V_{DS}=0.1V$ (linear)

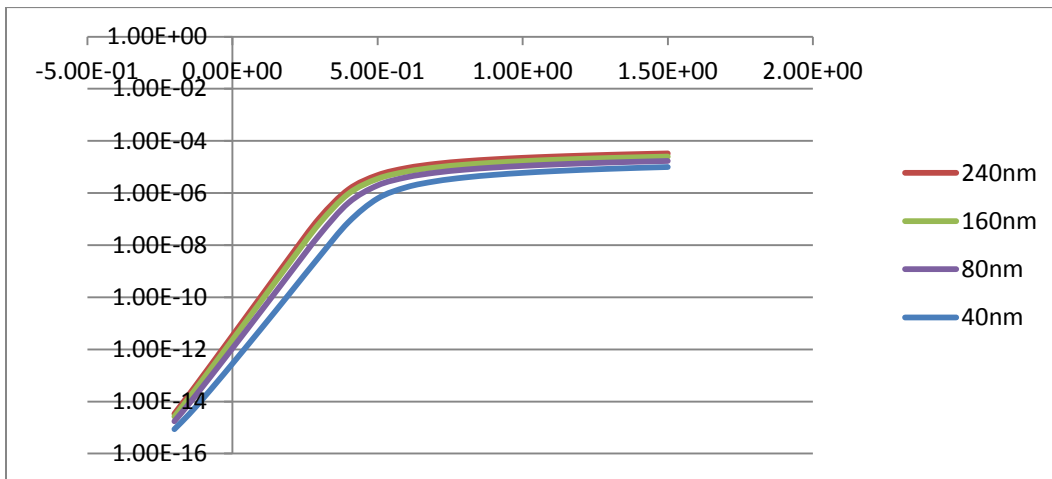


Fig 09: Ids vs Vgs curves for $V_{DS}=0.1V$ (log)

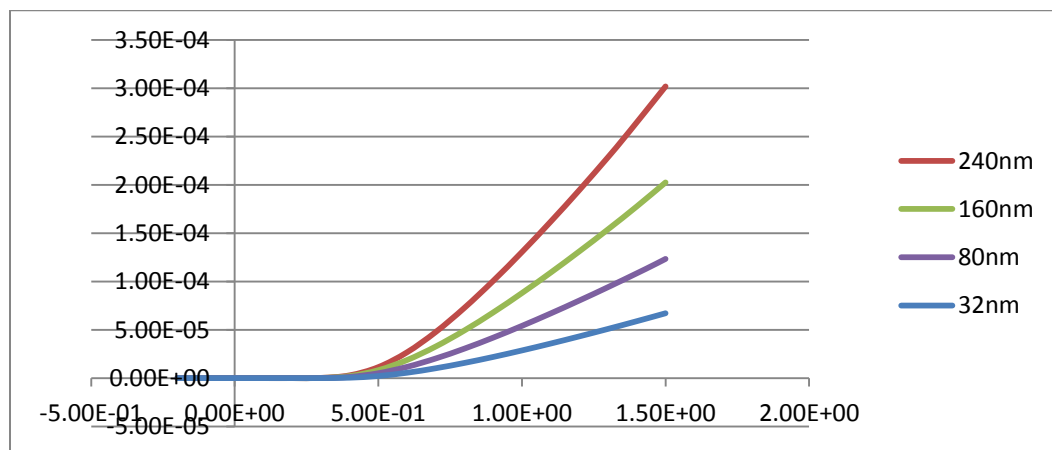


Fig 10: Ids vs Vgs curves for $V_{DS}=1.0V$ (linear)

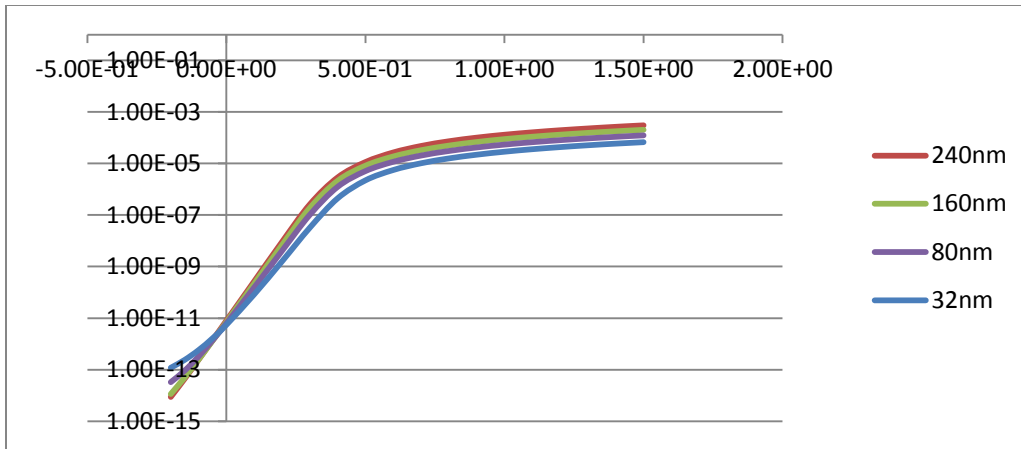


Fig 11: Ids vs Vgs curves for $V_{DS}=1.0V$ (log)

A.4 Combined Gate Vertical MOS Transistor

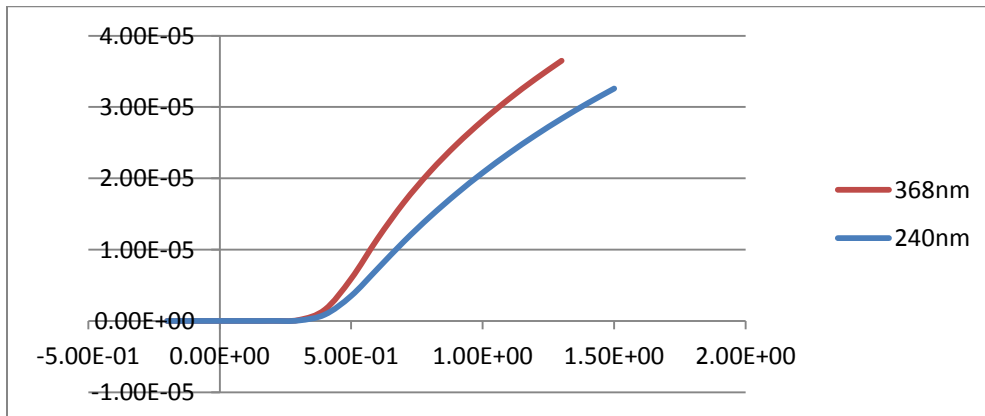


Fig 12: Ids vs Vgs curves for $V_{DS}=0.1V$ (linear)

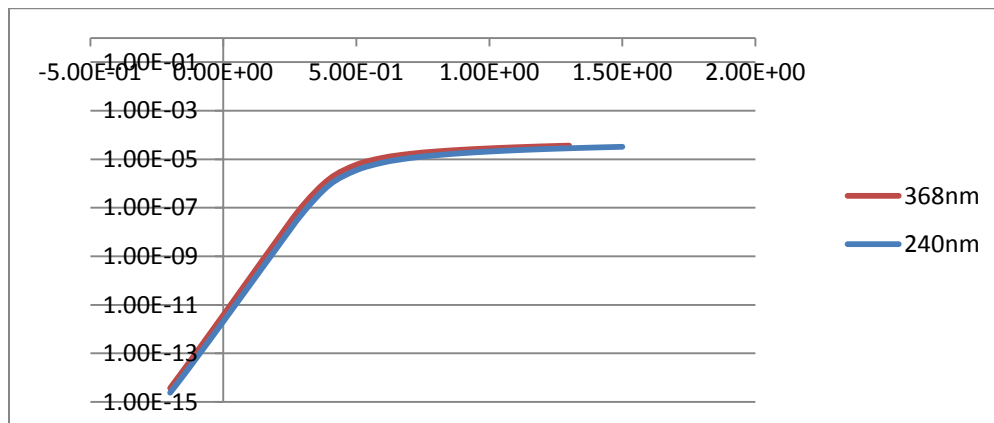


Fig 13: Ids vs Vgs curves for $V_{DS}=0.1V$ (log)

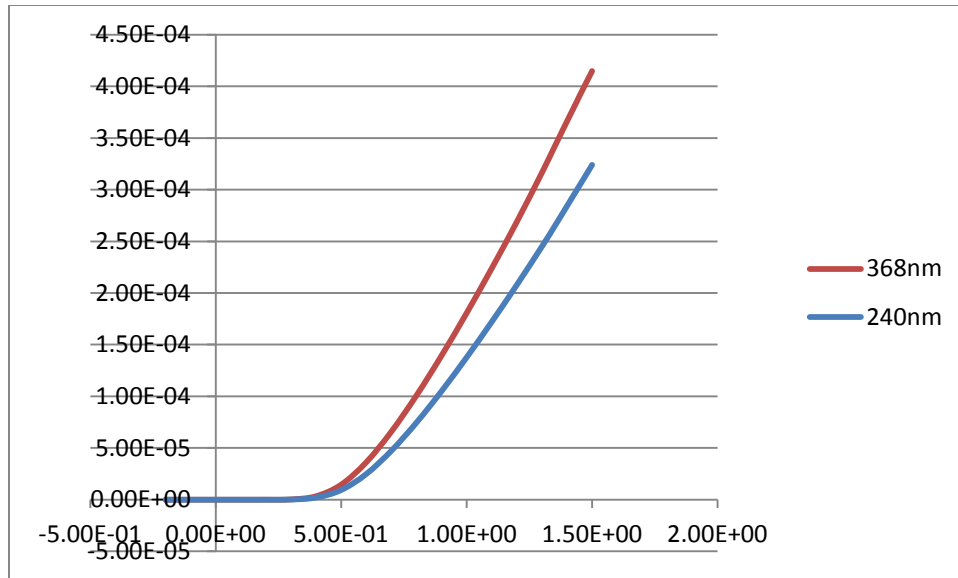


Fig 14: I_{ds} vs V_{gs} curves for V_{DS}=1.0V(linear)

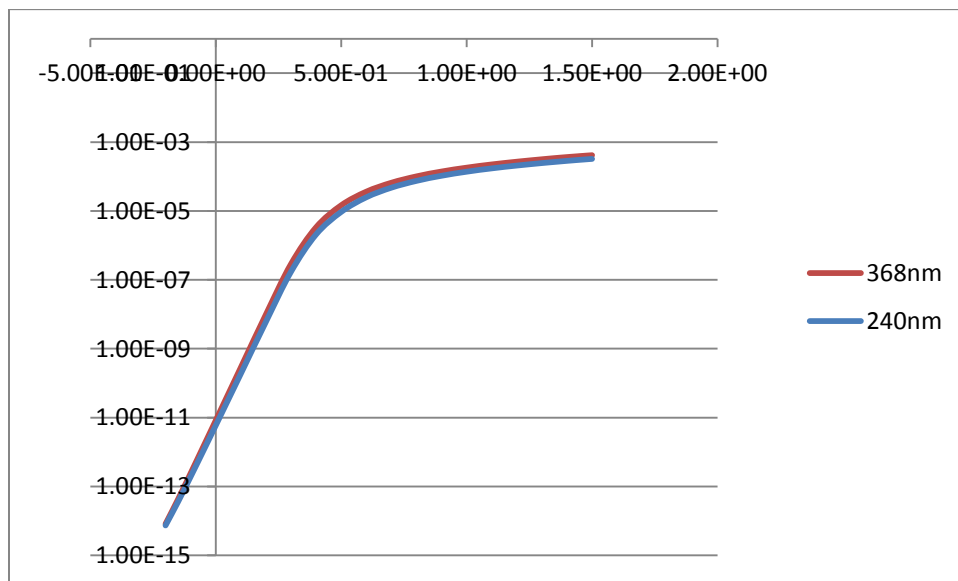


Fig 15: I_{ds} vs V_{gs} curves for V_{DS}=1.0V(log)

A.5 Single & Double Gate Vertical MOS Transistor

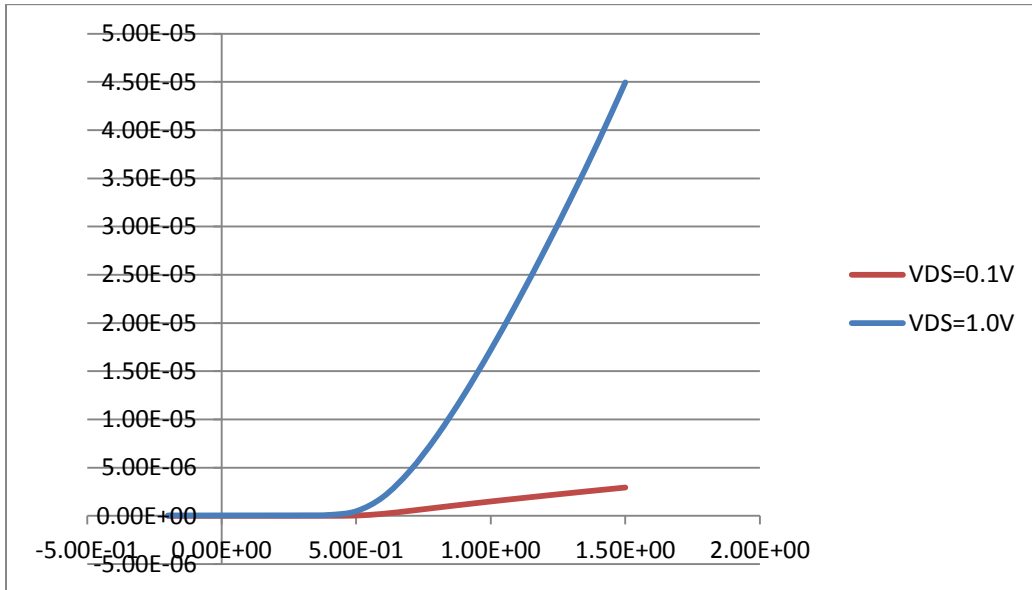


Fig 16: I_{ds} vs V_{gs} curves of Single gate for 40nm

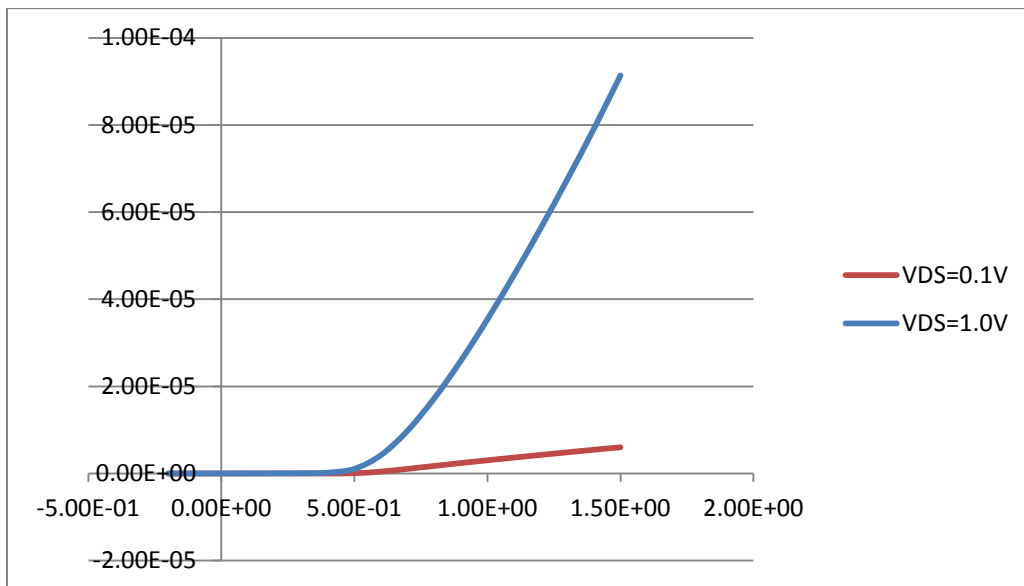


Fig 17: I_{ds} vs V_{gs} curves of Double gate for 80nm