Assimilation of negative feedback in Bandgap reference circuits for subsiding the variation of reference voltages over the temperature range from -55^0C to $+165^0$C

By

Syed Ziaul Haque

Md.Rashed Uzzaman

Abdullah-Al-Mamun

Submitted to

The Department of Electrical and Electronic Engineering

Faculty of Science and Engineering

East West University

In partial fulfillment of the requirements for

The degree

Of

Bachelor of Science in Electrical & Electronics Engineering

(B.Sc. in EEE)

Fall, 2011

APPROVAL

The project titled "Assimilation of negative feedback in Bandgap reference circuits for subsiding the variation of reference voltages over the temperature range from -55^0C to $+165^0$C." submitted by Syed Ziaul Haque (2008-1-80-061), Md.Rashed Uzzaman (2008-1-80-035) and Abdullah-Al-Mamun (2008-1-80-067), has been accepted as satisfactory in partial fulfillment of the requirements for the degree of Bachelor in Science in Electrical and Electronic Engineering on Fall 2011.

S. M. Shahriar Rashid (Supervisor)

Lecturer

Department of Electrical and Electronic Engineering,

East West University, Dhaka.

22.01.2012

Dr. Anisul Haque

Professor & Chairperson

Department of Electrical and Electronic Engineering

East West University, Dhaka.

AUTHORIZATION

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Countersigned

S. M. Shahriar Rashid (Supervisor)

Lecturer

Department of Electrical and Electronic Engineering,

East West University, Dhaka.

Signature of the students

Syed Ziaul Haque

Md.Rashed Uzzaman

Abdullah-Al-Mamun

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ACKNOWLEDGEMENTS

We are heartily thankful to our supervisor, S. M. Shahriar Rashid, Lecturer, East West University whose encouragement, guidance and support from the initial to the final level enabled us to develop an understanding of the subject. His profound knowledge about our research topic has displayed an effective way to achieve our goal.

Our gratitude extends to our chairperson & professor, Dr. Anisul Haque and all the faculty members of EEE department specially Mr. Khondker Zakir Ahmed for developing a basic basement about the research topic that later proved helpful.

Next, we offer our regards and blessings to our family and friends who supported us in any respect during the completion of the project.

Finally, we bow our heads to Al-mighty Allah, the most gracious and merciful, for HIS approbation about the completion of our thesis.

ABSTRACT

Latest technologies demand for low voltage and low power in designing both analog and digital integrated circuits. The purpose is to incorporate as much devices as possible into a single chip and to operate them in low voltage in order to minimize power loss. On the other hand, many electronic blocks such as oscillator, data converter (A/D or D/A) etc. require a precise reference voltage so as to work properly even when there is supply, process and temperature variations. A Bandgap reference circuit (BGR) plays a vital role, in this case, that provides a low reference voltage that is exempt to temperature, process and supply variations.

In this project, a 1.2V CMOS Bandgap reference circuit with supply voltage range of 1.8V to 2V in associated with active regulated circuits is proposed. The reference circuit is designed to operate at an ambient temperature of 27^0C with line regulation of 177.5mV/V and a temperature coefficient of 241ppm/^{0}C. The reference circuit composed of a supply independent block (which is basically a common-gate-Op Amp) that keeps the reference immune to supply variation to some extent. Another part of the reference circuit is the temperature independent block that is designed in such a way that the reference has negligible impact with temperature variation and also it debilitates the effect of process variation with temperature. An equation is derived for the clear understanding of how process variation is affecting the reference voltage. Lastly, the values obtained from the design simulation are compared with the other proposals.

A two stage operational amplifier with a gain of around 70dB is designed to demonstrate the adverse effect of varying reference on its gain. Owing to its high open loop dc gain, the Op Amp shows a significant change due to small change in its biasing voltage. The gain of the Op Amp varies from 13%-15% due to variation in temperature and 60%-130% due to the variation in supply. So active regulated circuits are proposed that incorporate negative feedback mechanisms, in order, to subside the reference voltage to 1.2V, for a wide range of temperature from -55^0C to +165^0C. The analyses are carried out in Advanced Design System (ADS) software using TSMC 0.18um technology.

CHAPTER I

1 Introduction

1.1 Motivation

In modern era of science and technology, as the drastic development of contemporary communication and consumer products such as web servers, cellular phones and various PDA products, high quality power supply that provides them suitable power are in great demand. As a result, the research on power management ICs has become a new hot spot for IC designers. And voltage reference, as one of key modules in the power management ICs, is responsible for offering a precision reference voltage to other internal blocks such as linear regulator, comparators, data conversions blocks like A/D (analog-to-digital) and D/A (digital-to-Analog) converters, charge pumps, OSC (oscillator), current source etc. are the few most common examples.

There is no doubt that at present, the cutting-edge technologies demand for low voltage and low power. This has brought new challenges for circuit designers to superpose these criteria into the design of both analog and digital systems. However, it is possible to design various architecture of Bandgap reference (BGR) that can fulfill the demands but an important concern about BGR circuits is their temperature dependency. In order to achieve as much temperature immunity as possible much work has been developed recently [1-3]. Modern chips tend to dissipate a considerable amount of heat and this fact represents a source of deviation in the performance of reference circuit. The atmospheric temperature variations can also degrade the performance.

Circuit functionality is critically influenced by process variations [4] depending on the technology. It is usually necessary to trim the circuit at the time the wafer [5] is being tested so that the measurement results are close to simulation ones. The current-mirror mismatch is one such dominant source of error and it causes a mismatch in collector currents of the bipolar transistors. Moreover, in typical implementations, the emitter-base voltage spread of the bipolar, lambda effect; threshold mismatch; resistor mismatch and early voltage are also sources of mismatch.

Apart from process & temperature dependency the supply dependent reference is also a critical issue that must be taken into account while designing. Voltage references find applications in a variety of circuits and systems, power converter and other circuits requiring an accurate reference voltage. So an ideal reference voltage must be, inherently, well-defined and its output voltage should be independent of power supply variation.

1.2 Literature review

A BGR circuits are those whose output is immune to temperature, process and power supply variations. These circuits are widely used in integrated circuits [6] usually with an output voltage around 1.25V, close to the theoretical value of 1.22eV (Bandgap of silicon at zero Kelvin) [7]. This circuit concept was first published by David Hilbiber in 1964 [8]. Bob Widlar [9] followed up with other commercially successful versions.

The first BGR approach [10] originally proposed a way of obtaining a reference voltage that was not based on Zener diodes [11] or on the threshold voltage [12] difference between an enhancement transistor [13], and a depletion transistor [14]. The architecture proposed in [10], although very simple, suffers from temperature compensation and from weak performance considering power supply rejection ratio [15]. The Brokaw Cell [16] proposes two additional features compared to the first BGR: the complementary to absolute temperature (CTAT) and proportional to absolute temperature (PTAT) voltages [17] are generated by the same bipolar transistors making the object more reliable and easy. Moreover, the base currents have less influence in the overall performance of the reference because the transistors gain is less important. The disadvantages of this second solution consist on requiring an error amplifier, which imposes higher current consumption and on collector-emitter voltages dependency on the supply voltage and on the voltage drop across the resistors.

As a matter of fact, that after 40 years of the invention of BGR circuit, the demand for the circuit, in terms of operation, is not the same. There is no doubt, that at present, low voltage and low power are two important criteria that must be fulfilled by the designers to reach their goal. The designers have faced numerous new challenges to accomplish their mission. Consequently, even sub 1V CMOS BGR has been proposed [10] without introducing any special devices and technology. Some of them are constitutes by the use of parasitic vertical bipolar junction transistors (BJT) [10]. And others are based on the research of Filanovsky and Allam in 2001 [18]. But due to the limit of technology and fluctuations of the process, not all these theories became practice.

1.3 Thesis Objective

Our objective here is to design and simulate a typical BGR circuit which is capable of producing a reference output of 1.2V at room temperature (around 27°C). The circuit should produce a reference that is independent of supply, process and temperature.

The reference circuit would utilize an error amplifier [19] in order to make the reference output independent of supply variation. The concept of positive and negative temperature coefficient [17] would be applied to make the reference circuit immune to temperature fluctuations. If the circuit is made temperature independent, then one can consider it to be a process independent as well. Moreover, the design of the reference circuit would be such that the process variation would have negligible effect on the reference output.

Next, our analysis would focus on the effect of the reference variation with respect to temperature & process on other circuits. In order to make the effect more splashing, we shall design a two-stage amplifier with a gain of around 70dB. This high gain of amplifier would sense the small change in the reference output and produce a significant variation in its output. The purpose of designing this amplifier would be to support our point, that even a small variation in reference can have a significant impact on the other circuits such as Op Amp, oscillator etc.

Finally, we would propose some topologies that could be added with the typical BGR circuit in order to arrive at even less sensitive reference output. The proposals would be discussed theoretically to justify our goal of achieving a process, supply & temperature independent reference voltage.

1.4 Overview

This report is divided into five different chapters. The first chapter includes the introduction which is sub-divided into four different sections: the motivation, literature review, thesis objective and overview of the report. This chapter discussed the need of BGR circuit in the design of both analog & digital circuits. It also recognizes the work and study on BGR that had been carried out early in the past. A discussion is made based on our objective on the analysis of a basic BGR circuit and finally the chapter is terminated through a short overview of report that may act as guide line for readers.

The second chapter describes the basic concepts of a BGR circuit. It includes several topologies to make a reference voltage independent of supply, process & temperature. Finally, short description is made based on our designed reference circuit and the simulation results are also discussed.

In chapter three, the negative impact of varying reference output is discussed. For this, a relatively high gain amplifier is designed and the effect of changing reference on the gain of the amplifier is presented through the help of simulation results.

The proposal to improve the BGR circuit is discussed elaborately in chapter four and finally in chapter five the report is terminated by drawing out a conclusion & a detail description about ADS software.

CHAPTER II

2 Bandgap Reference Circuit

2.1 Introduction

Almost every analog integrated circuit utilizes a reference which could be either voltage or current. For instance, Bandgap reference (BGR) circuits [17] provide popular high performance reference circuits, implementing components with positive temperature coefficient and negative temperature coefficient and add the voltages or current of these components in a predetermined proportion to generate a value independent of temperature, the value output as a reference. Conventional BGR circuits use bipolar technology to create a stable low reference voltage of around 1.2V, almost equal to the silicon energy gap measured in electron volts.

The purpose of reference generation is to establish a dc voltage or current that is independent of the supply and process and has a well-defined behavior with temperature. If the reference is temperature independent then it is process independent as well, since most process parameters vary with temperature.

This chapter deals with the design of reference generators in CMOS technology, focusing on well-established Bandgap techniques. First, we studied supply-independent biasing technique and then we described temperature-independent references. Finally, the concepts of supply and temperature independent reference along with the result of simulations are used to describe the actual circuit of concern.

2.2 Supply-independent Biasing

The supply-independent reference refers to voltage/current which is independent of supply voltage (V_{DD}).The study below shows how a reference current is generated and how this reference is used to make output current, of a reference circuit, independent of supply voltage. In this study, the channel-length modulations of MOS devices are neglected. The circuit in fig: 2.1 assumes that a golden reference current (I_{Ref}) is available,

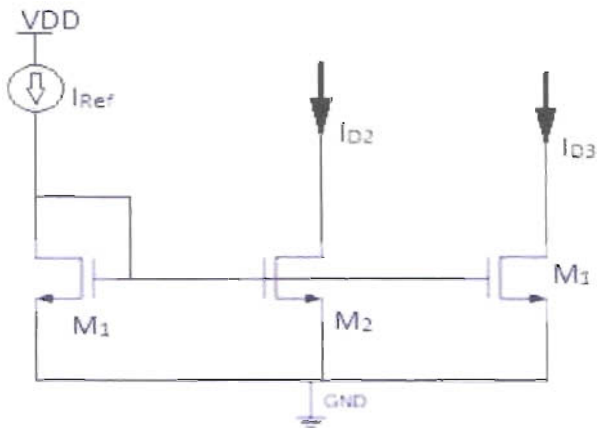

Figure 2-1: Current biasing using an ideal current source.

If I_{Ref} is independent of VDD then I_{D2} & I_{D3} will also be independent of V_{DD}. But how to generate I_{Ref}? The set-up of fig: 2.2 shows the generation of I_{Ref}.

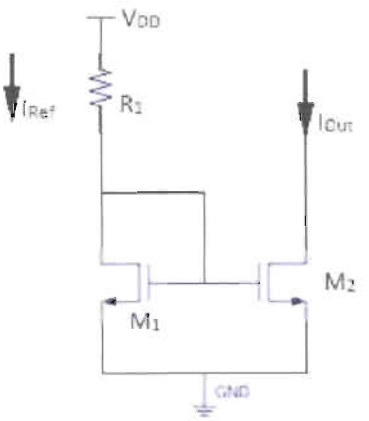

Figure 2-2: Current mirror biasing using a resistor.

As an approximation of a current source, the ideal current source in fig: 2.2 is replaced by a resistor (R_1).From the concept of mirror circuit we have,

$$\frac{\Delta I_{out}}{\Delta I_{Ref}} = \frac{(W/L)_2}{(W/L)_1}$$

Hence,

$$\Delta I_{Ref} = \frac{\Delta V_{DD}}{R_1 + 1/g_{m1}} \cdot \frac{(W/L)_2}{(W/L)_1}$$

The above equation shows that the output current is quite sensitive to V_{DD}. In order to arrive at a less sensitive solution the set-up in fig: 2.3 could be useful.

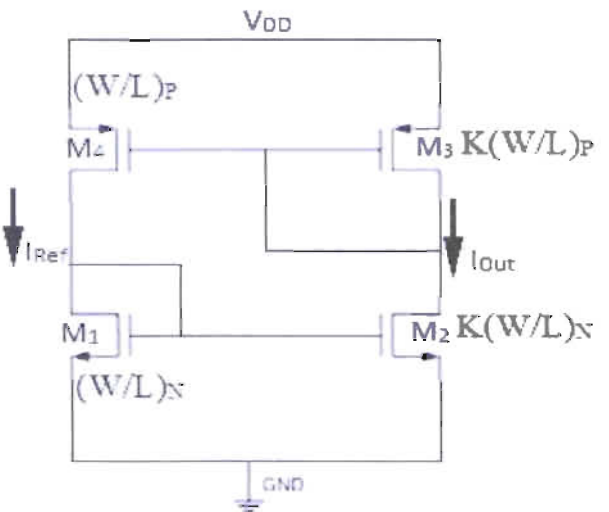

Figure 2-3: Simple circuit to establish supply-independent currents.

Since each diode connected device [17] feeds from a current source hence I_{out} & I_{Ref} are relatively independent of V_{DD}. So the magnitudes of the current should be defined by other parameters like W/L ratio. The governing equation for the current can be expressed as,

$$\Delta I_{out} = kI_{Ref}$$

2.3 Temperature-independent references

Temperature-independent reference refers to the voltage/current that is independent of temperature / process. The idea here is that if two quantities (let say voltages V_1 and V_2), having opposite temperature coefficients (TCs), are added with proper weighting, the result displays a zero TC. Like if V_1 and V_2 vary in opposite direction with temperature then,

$$\alpha_1 \frac{\partial V_1}{\partial T} + \alpha_2 \frac{\partial V_2}{\partial T} = 0$$

Where α_1 and α_2 are constants and $\frac{\partial V_1}{\partial T}$ and $\frac{\partial V_2}{\partial T}$ are temperature coefficients of V_1 and V_2 respectively. Thus,

$$V_{Ref} = \alpha_1 V_1 + \alpha_2 V_2 \text{ (zero TC reference)}$$

The objective here is to design a circuit which will add two quantities that vary in opposite direction with temperature.

2.3.1 Negative- TC voltage

As shown in fig: 2.4, an n-p-n transistor is feed from an ideal current source with collector current, I_C.

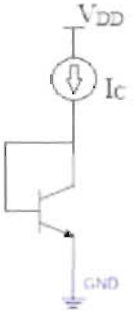

Figure 2-4: Set up for negative TC.

If the reverse saturation current in the BJT is I_S with base-emitter voltage V_{BE} then collector current can be expressed as,

$$I_c = I_s e^{V_{BE}/V_T}$$

Here,

$$V_T = \frac{KT}{q}$$

$$I_s \propto \mu K T n_i^2$$

$$\mu \propto \mu_0 T^m$$

$$n_i \propto T^3 e^{-E_g/KT}$$

where, μ represents mobility of minority carrier, n_i represents intrinsic minority carrier concentration, K represents Boltzman constant, T represents temperature in Kelvin, m is a device parameter with a value of -3/2, E_g represents Bandgap energy of silicon(1.12eV), and q is the electronic charge.

Thus, $$I_s = bT^{(4+m)} e^{-E_g/KT} \quad (2.1)$$

From the expression of I_C

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) \quad (2.2)$$

Since TC of V_{BE} is $\frac{\partial V_{BE}}{\partial T}$

Hence, $$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln\left(\frac{I_C}{I_S}\right) - \frac{V_T}{I_S}\frac{\partial I_S}{\partial T} \quad (2.3)$$

I_C is considered as temperature independent for simplicity, indeed it is not temperature independent. We shall deal with the temperature coefficient of I_C after a short while. The equation (2.1) can be partially differentiate with respect to temperature as,

$$\frac{\partial I_S}{\partial T} = b(4+m)T^{3+m} e^{\frac{-E_g}{kT}} + bT^{3+m} e^{\frac{-E_g}{kT}} \left(\frac{E_g}{kT}\right)$$

So, $$\frac{V_T}{I_S}\frac{\partial I_S}{\partial T} = (4+m)\frac{V_T}{T} + \frac{E_g}{kT} V_T \quad (2.4)$$

And $$\frac{\partial V_T}{\partial T} = \frac{k}{q} = \frac{V_T}{T} \quad (2.5)$$

Substituting equation (2.4) and equation (2.5) in equation (2.3) we have,

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_T}{T} \ln\left(\frac{I_C}{I_S}\right) - (4+m)\frac{V_T}{T} - \frac{E_g}{kT} V_T$$

$$= \frac{V_{BE}}{T} - (4+m)\frac{V_T}{T} - \frac{E_g/q}{T}$$

Therefore,

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - E_g/q}{T} \quad (2.6)$$

The equation (2.6) reveals that the TC of V_{BE} ($\frac{\partial V_{BE}}{\partial T}$) is inversely related with temperature. If we insert some typical values let say,

$$V_{BE} = 750mV \text{ and T= 300K}$$

Then,

$$\frac{\partial V_{BE}}{\partial T} = \frac{750m - \left(4+\frac{3}{2}\right)(0.026) - {}^{1.12eV}/_{q}}{300^{0}k} = -1.5\text{mV}/^{0}\text{K}$$

From above analysis we obtained a negative TC parameter i.e. V_{BE} as shown in fig: 2.5.

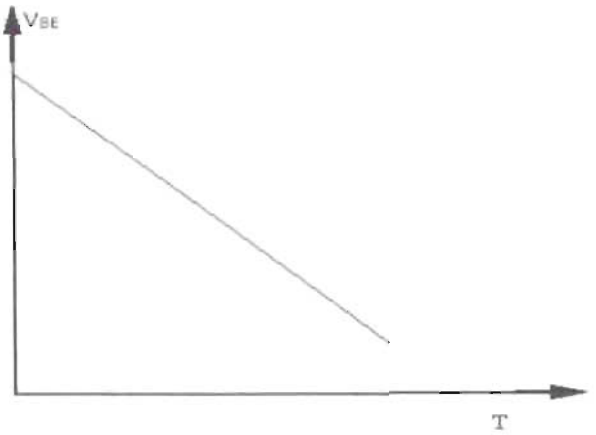

Figure 2-5: Negative sloping line for the TC of V_{BE}.

2.3.2 Positive-TC Voltage

If two bipolar transistors operate at unequal current densities, then the difference between their base-emitter voltages is directly proportional to the absolute temperature.

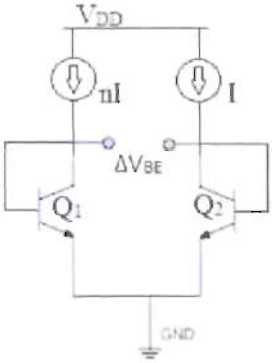

Figure 2-6: Generation of PTAT voltage.

The fig: 2.6 shows the two identical transistors (i.e. $I_{S1} = I_{S2}$) are biased at collector currents of nI and I and if their base currents are negligible, then

$$\Delta V_{BE} = V_{BE1} - V_{BE2}$$

$$= V_T \ln\frac{nI}{I_{S1}} - V_T \ln\frac{I}{I_{S2}}$$

So,

$$\Delta V_{BE} = V_T \ln n \qquad (2.7)$$

$$= \frac{kT}{q} \ln n$$

Therefore,

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln n \qquad (2.8)$$

The equation (2.8) shows that V_{BE} difference exhibits a positive TC and this TC is independent of the collector currents. [The non-idealities in the characteristic of bipolar transistor introduce small temperature dependence in TC ofΔV_{BE}] .The positive temperature coefficient of the ΔV_{BE} is shown in fig: 2.7.

Figure 2-7: Positive sloping line for the TC of ΔV_{BE}.

2.3.3 Bandgap Reference

With the negative and positive TC voltages obtained above, we can now develop a reference having nominally zero TC.

$$V_{Ref} = \alpha_1 V_{BE} + \alpha_2 \Delta V_{BE}$$

$$V_{Ref} = \alpha_1 V_{BE} + \alpha_2 V_T \ln n$$

At room temperature, $\frac{\partial V_{BE}}{\partial T} \simeq$ -1.5 mV/^{0}K and $\frac{\partial V_T}{\partial T} \simeq$ +0.087mV/^{0}K.

Now for $\frac{\partial V_{Ref}}{\partial T}$ to be zero,

$$\alpha_1 \frac{\partial V_{BE}}{\partial T} + \alpha_2 \frac{\partial V_{BE}}{\partial T} = 0$$

$$\propto_1 (-1.5) + \propto_2 \frac{\partial V_T}{\partial T} \ln n = 0$$

If $\propto_1 = 1\ (chosen)$ then $\propto_2 \frac{\partial V_T}{\partial T} \ln(\propto) = 1.5$

$$\propto_2 \ln n\,(0.087) = 1.5$$
$$\propto_2 \ln n = 17.2$$

Therefore,

$$V_{Ref} = V_{BE} + 17.2 V_T$$

If V_{BE} = 750mV and V_T = 0.026 are at room temperature then,

$$V_{Ref} = 750m + 17.2\,(0.026)$$
$$= 1.2V \text{ [this is the value of } V_{Ref} \text{ for zero TC]}$$

Now we need to device a circuit that adds V_{BE} to 17.2 V_T as shown in fig: 2.8

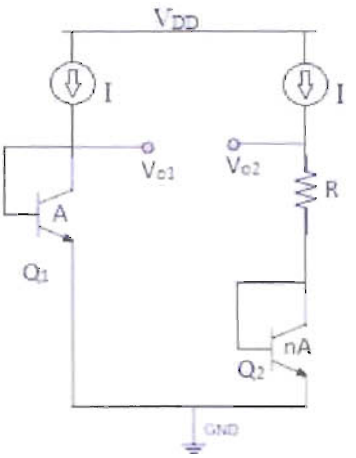

Figure 2-8: Conceptual generation of temperature-independent voltage.

Here Q_2 consists of n unit transistors and Q_1 is a unit transistor.

If V_{01} and V_{02} are forced to be equal then,

$$V_{BE1} = RI + V_{BE2}$$
$$RI = V_{BE1} - V_{BE2}$$
$$RI = \Delta V_{BE}$$
$$RI = V_T \ln n \text{ [from equation (2.7)]}$$

So, $$V_{02} = V_{BE2} + RI$$

Therefore, $$V_{02} = V_{BE2} + V_T \ln n \qquad (2.9)$$

The equation (2.9) suggests that V_{02} can serve as temperature independent reference if $\ln(n) \approx 17.2$ (while V_{01} and V_{02} remain equal). The circuit suggested in fig: 2.8, requires two modifications to become practical. Firstly, it requires a mechanism that guarantees $V_{01} = V_{02}$. Secondly, since ln (n) = 17.2, it states that n is very large.

So the term RI = V_T ln (n) must be scaled up by a reasonable factor in order to make the value of n small. The circuit as shown in fig: 2.9 fulfills the above two requirements.

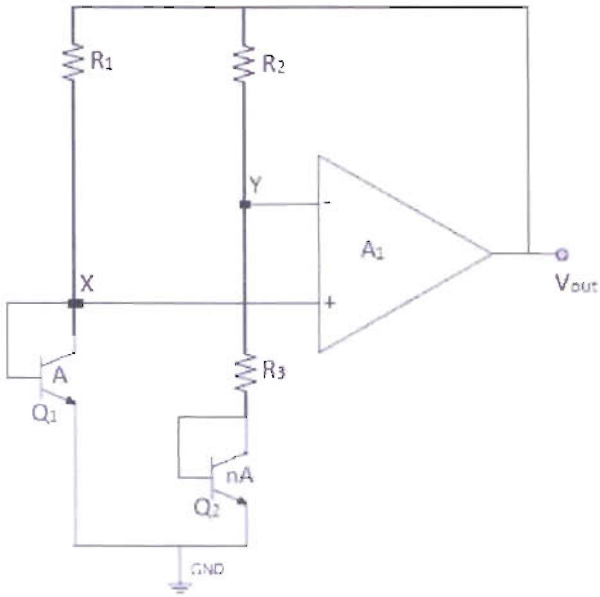

Figure 2-9: Actual implementation of the Conceptual generation of temperature-independent voltage.

Here, amplifier A_1 senses V_X and V_Y, driving the top terminals of R_1 and R_2 (R_1=R_2) such that X and Y settle to approximately equal voltages. The reference voltage is obtained at the output of the amplifier rather than at node of Y.

We have,

$$V_{out} = V_{BE2} + V_{R3} + V_{R2}$$

Since current through the branch where R_2, R_3 and Q_2 are connected is

$$I = \frac{V_{R3}}{R_3} = \frac{\Delta V_{BE}}{R_3} = \frac{V_T \ln n}{R_3} \qquad (2.10)$$

Then,

$$V_{out} = V_{BE2} + \frac{V_T \ln n}{R_3}(R_3 + R_2)$$

$$V_{out} = V_{BE2} + V_T \ln n \left(1 + \frac{R_2}{R_3}\right)$$

For zero TC, $\left(1+\frac{R_2}{R_3}\right)\ln n \simeq 17.2$ and if $\left(1+\frac{R_2}{R_3}\right) = 10$ [chosen]

Then $$\ln(n) = 1.7$$

or $$n = 5.4 \simeq 6$$

Hence the number of transistor has scaled down to 5 from 29 million transistors what would be the case when only ln(n) = 17.2 were considered.

2.3.4 Collector current Variation

The circuit of fig: 2.9 violate one of our earlier assumptions (i.e. the collector current is temperature independent); the collector currents of Q_1 and Q_2 given by $\frac{V_T \ln n}{R_3}$ are proportional to T, whereas $\frac{\partial V_{BE}}{\partial T} \simeq -1.5\text{mV}/^0\text{K}$ was derived for a constant current. So, incorporating the temperature coefficient of I_C in the equation (2.3) gives,

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} ln\left(\frac{I_C}{I_S}\right) + V_T\left(\frac{1}{I_C}\frac{\partial I_C}{\partial T} - \frac{1}{I_S}\frac{\partial I_S}{\partial T}\right)$$

From equation (2.9),

$$\frac{\partial I_C}{\partial T} = \frac{\ln n}{R_3}\frac{\partial V_T}{\partial T} = \frac{k}{qR_3}\ln n = \frac{V_T \ln n}{R_3 T}$$

So,

$$\frac{\partial I_C}{\partial T} \simeq \frac{I_C}{T}$$

Hence,

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} ln\left(\frac{I_C}{I_S}\right) + \frac{V_T}{T} - \frac{V_T}{I_S}\frac{\partial I_S}{\partial T}$$

$$= \frac{V_T}{T} ln\left(\frac{I_C}{I_S}\right) + \frac{V_T}{T} - (4+m)\frac{V_T}{T} - \frac{E_g}{kT^2}$$

$$= \frac{V_{BE}}{T} + \frac{V_T}{T}(-3-m) - \frac{E_g}{kT^2}V_T$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (3+m)V_T - \frac{E_g}{q}}{T} \qquad (2.11)$$

The equation (2.11) indicates that the TC is slightly less negative than -1.5mV/°K

2.4 Compatibility with CMOS Technology

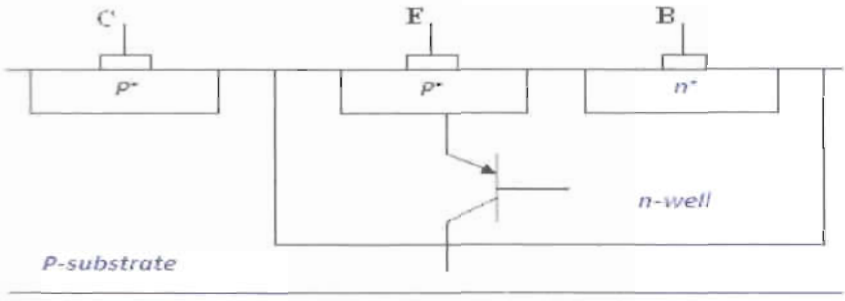

Figure 2-10: Realization of p-n-p bipolar transistor in CMOS technology.

In n-well process the p-n-p transistor can be formed as depicted in fig: 2.10. Here the p^+ in n-well acts as emitter and the n-well itself as the base and the p-substrate acts as collector. The collector is inevitably connected to most negative supply (usually ground). So fig: 2.9 can be modified as shown in fig: 2.11.

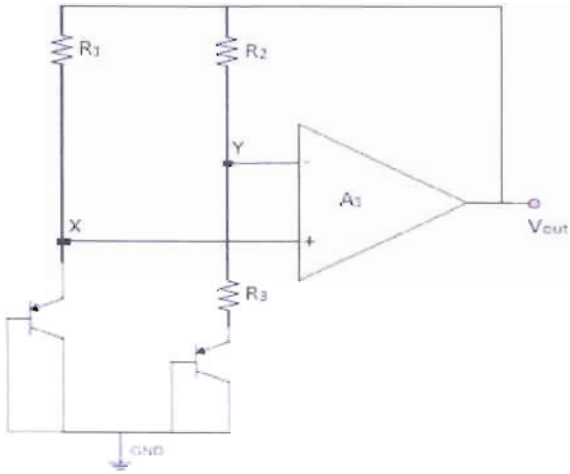

Figure 2-11: Conceptual generation of temperature-independent voltage with p-n-p transistors.

2.5 PTAT current Generation

Proportional to Absolute Temperature (PTAT) current can be generated from the Bandgap reference circuit. The knowledge that we have obtained so far can be coupled together to design a circuit which is capable to generate PTAT current. The topology is shown in fig: 2.12

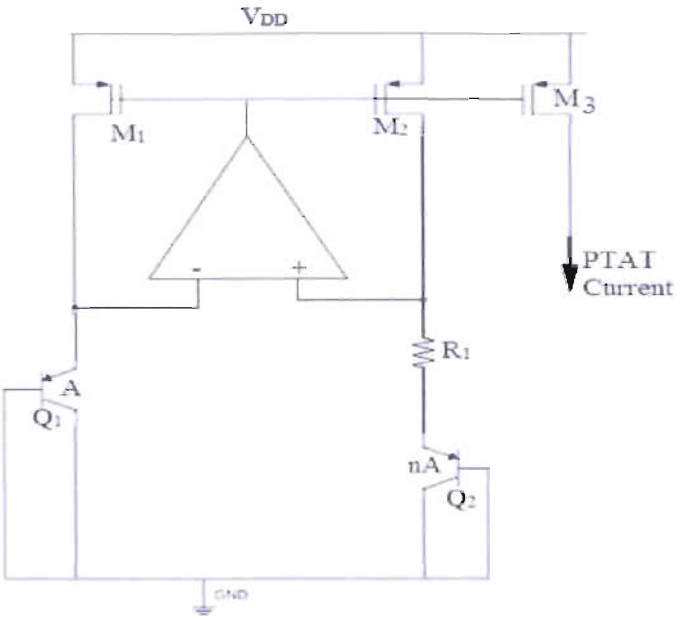

Figure 2-12: Generation of a PTAT current.

The operational amplifier keeps its input node voltage same (as if virtually shorted) which is the condition necessary for supply-independent biasing. The current in the second branch (i.e the current through Q_2) is copied into the third branch as PTAT current. Alternatively, the supply independent biasing scheme can be combined to generate PTAT as shown in fig: 2.13.

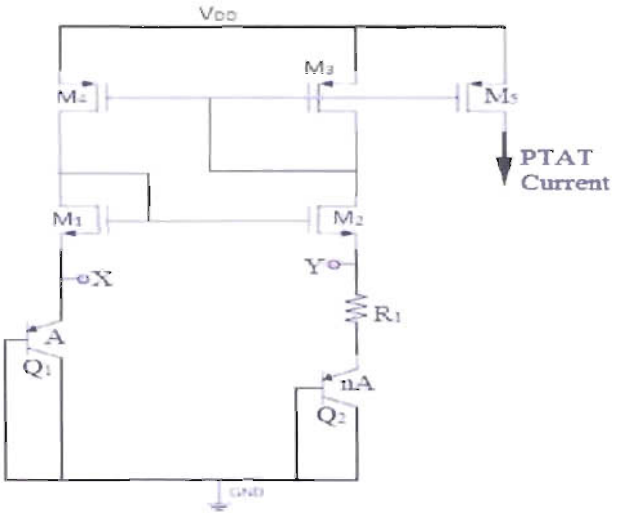

Figure 2-13: Generation of a PTAT current uses a simple amplifier.

For simplicity the MOS devices are considered identical and $I_{D1} = I_{D2} = \frac{V_T}{R_1} \ln(n)$ yielding the same behavior for I_{D5} (i.e. the current through M_5). But in practice, due to mismatch between the transistors and more importantly the temperature coefficient of R_1, the variation of I_{D5} deviates

from ideal equation. The fig: 2.13 can be modified to provide a temperature independent voltage (Bandgap reference voltage) as shown in fig: 2.14

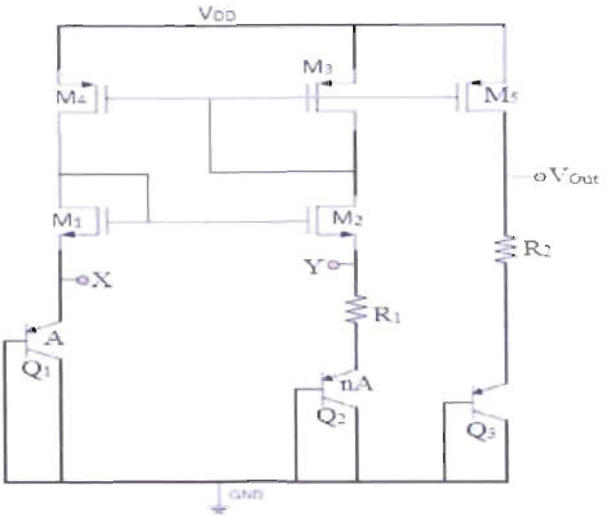

Figure 2-14: Generation of a temperature- independent voltage.

The idea here is to add a PTAT voltage, $I_{D5}R_2$ to the base-emitter voltage of the transistor Q_3.

So, $$V_{Out} = V_{Ref} = V_{BE3} + I_{D5}R_2$$

Therefore,

$$V_{Ref} = V_{BE3} + \frac{R_2}{R_1}V_T \ln(n) \qquad (2.12)$$

In the above derivation, all the PMOS devices are assumed to be identical. In reality, the mismatch of PMOS devices introduces error in V_{Ref}.

2.6 Bandgap Circuit and Simulation Result

2.6.1 General discussion

So far we have learnt that how different arrangements help to generate a supply, process & temperature independent reference voltage or current. Now we shall pay an intense look to our actual circuit of concern in order to understand how this Bandgap reference circuit works. Apart from the description of the circuit, the ADS simulation result will be discussed in this section of the report.

2.6.2 Circuit description

As shown in fig: 2.15, the gates of M_3& M_4 are shorted and that the sources are connected to VDD. Since source to gate voltages (V_{SG3}& V_{SG4}) of both M_3& M_4 are equal hence the currents I_1& I_2 must also be equal. Again, the gate voltages of M_1& M_2 are equal as they are connected together. In order to fulfill the requirement for currents (i.e. $I_1=I_2$), the gate-to-source voltages (V_{GS1}& V_{GS2}) of M_1& M_2 must be equal. Therefore the source voltages (V_{S1}& V_{S2}) of

M_1& M_2 must be equal. The diode connected MOS devices (M_2& M_4) are being feed by the same current source (M_3) hence the magnitude of current through the two branches (I_1& I_2) are independent of V_{DD} but depends on the aspect ratio of the MOS devices. In total, the loop formed by M_1 through M_4 is acting as a current stirring circuit (Current mirror) [20] which is in fact a common gate boot strapping [21] operational amplifier (op Amp) [22].

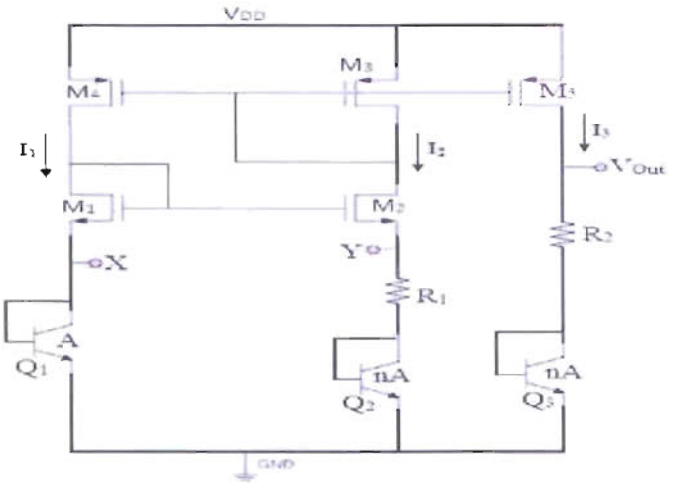

Figure 2-15: Bandgap Reference circuit.

In order to achieve a process & temperature independent reference voltage, the transistors (Q_1& Q_2) and resister (R_1) are connected underneath the common gate op Amp. The n-p-n transistors are used here in order to relate the reference voltage with temperature as the current through BJT is temperature dependent and so is its base-emitter voltage (V_{BE}).The current through Q_1 transistor is replicated into the third branch by using PMOS (M_5) as I_3 in order to scale down the number of transistors used for the fingering [23] purpose.

2.7 Simulation result

2.7.1 The effect of temperature variation in the reference output

The resistor R_2 has positive temperature coefficient, so it exhibits a positive sloping curve when it is allowed to vary with temperature as shown in the fig: 2.16

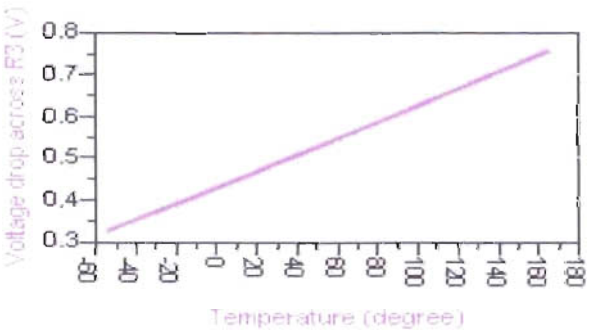

Figure 2-16: Voltage variation across R_2 with temperature

The gradient of the curve is positive owing to the fact that the voltage drop across the resistor is directly proportional to temperature.

The base-emitter voltage (V_{BE}) of BJT Q_3 has negative temperature coefficient, so it exhibits a negative sloping curve when it is allowed to vary with temperature as shown in the fig: 2.17

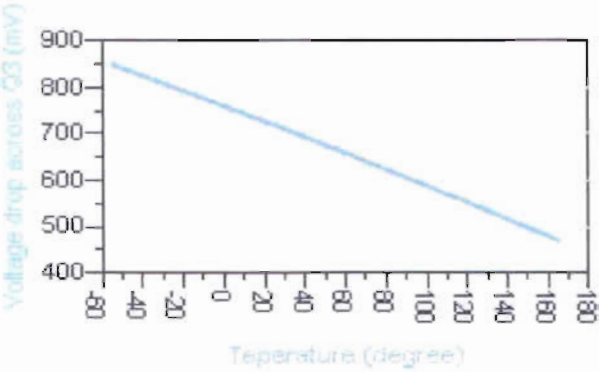

Figure 2-17: Voltage variation across Q_3 with temperature

From the graph of fig: 2.17, it can be observed that the gradient of the curve is less steep and negative. This is due to the fact that the voltage drop across the transistor is inversely related with the logarithmic term.

Finally the variation of the reference output is shown in the fig: 2.18. The reference output exhibits temperature dependency as depicted earlier and it has a positive sloping curve for a wide range of temperature (i.e. -55^{0}C to 165^{0}C). The reasons behind this curve are the temperature variations of base-emitter voltages and collector currents of the BJTs.

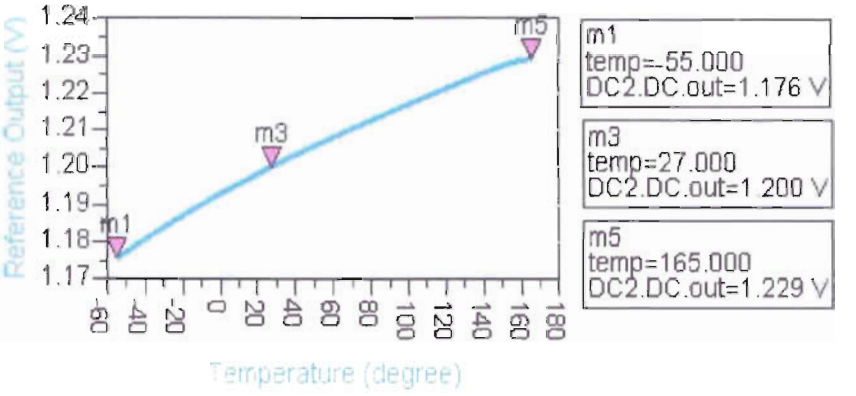

Figure 2-18: Variation of reference voltage with temperature

The positive sloping curve arises due to the fact that the TC of the resistor is dominating compare to the TC of the transistor (as the TC of the transistor is related with the logarithmic term) for the particular range of temperature. The data obtained from the plot of fig: 2.18 shows, for the temperature variation of -55^{0}C to 165^{0}C the output reference varies by 53mV which is equivalent to 241ppm/^{0}C. The variation can be minimized if a proper operating point is selected (in this case the operating temperature is 27^{0}C where the reference voltage is 1.2V).

2.7.1.1 *The effect of process variation in the reference output*

The term process variation refers to how the device parameter such as resistance varies with respect to other variables (in this case temperature). From our early knowledge, it is known that resistance varies ±25% with the variation of temperature. For simplicity, we varied the value of resistance and observe its effect in the reference output.

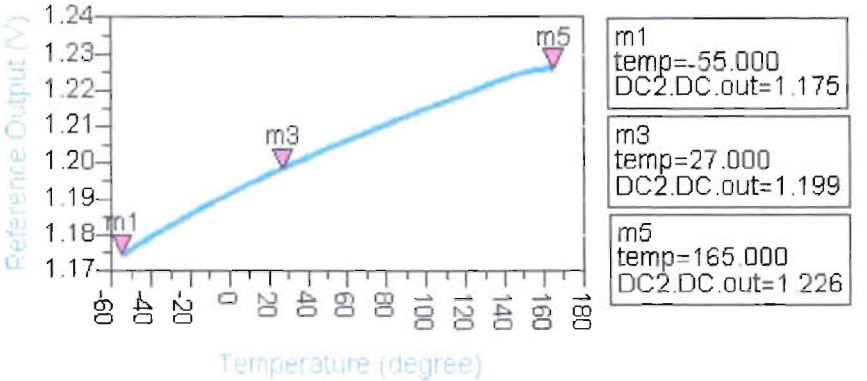

Figure 2-19: Variation of reference voltage with temperature when resistances are increased by 25%

The data collected from the plot of fig: 2.19, shows that the reference output decreases from 1.2V to 1.199V ($\Delta V = 1$ mV) at 27^0C i.e. the curve becomes flatter than before.

In order to understand why this happens, from equation (2.2) and equation (2.10) the equation (2.12) can be expressed as,

$$I_2 = \frac{V_T \ln n}{R_1} = I_3$$

$$I_3 = \left(\frac{k \ln n}{qR_1}\right).T$$

Now,

$$V_{Ref} = V_{BE3} + I_3 R_2$$

$$= V_T \ln \frac{I_3}{I_S} + \left(\frac{k \ln nR_2}{qR_1}\right).T$$

$$= \frac{kT}{q} \ln \left(\frac{k \ln n}{qR_1 I_S}.T\right) + \left(\frac{k \ln nR_2}{qR_1}\right).T$$

$$V_{Ref} = \frac{kT}{q} \ln \left(\frac{k \ln n}{qR_1 I_S}\right) + \frac{R_2}{R_1} V_T \ln n \qquad (2.13)$$

The equation (2.13) shows that when R_1 and R_2 are increased by 25% the gradient of the reference output is decreased so the curve becomes flatter. And when the resistances are lowered

the curve becomes steep as shown in fig: 2.20. So the reference output increases from 1.2V to 1.203V (ΔV =3mV) at 27^0C

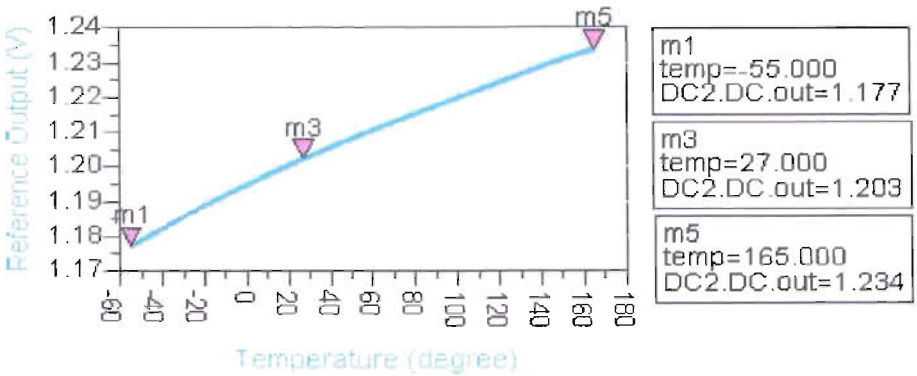

Figure 2-20: Variation of reference voltage with temperature when resistances are decreased by 25%

From the simulation result, it is evident that the effect of process variation in the reference output is insignificant since the voltage variation is very small over a wide range of temperature.

2.7.1.2 The effect of supply variation in the reference output

The data obtained from the plot of fig: 2.21 show that when the supply voltage changes from 1.6V to 2.0V, the variation of the output voltage of 1.2V is within 71mV. That is to say, the line regulation is 177.5mV/V.

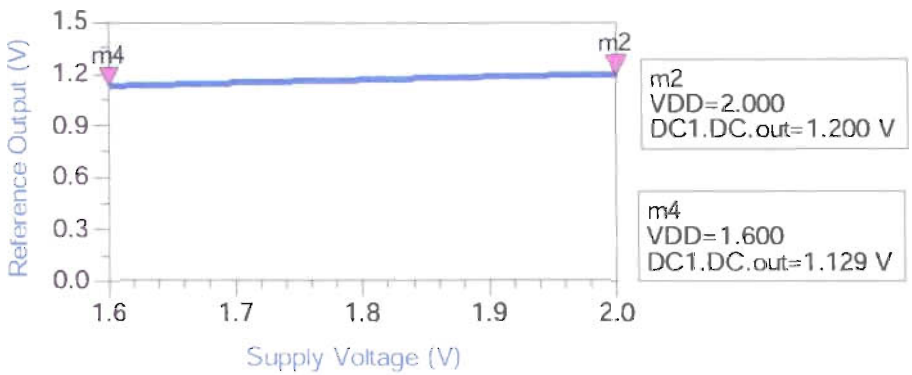

Figure 2-21: Reference output with varying supply voltage

This result evident a fact that the reference output still depends on the supply voltage. Obviously, this variation is very small compare to what would be the case if the common-gate op Amp was not used in the design.

The results obtained from our simulations are compared with the data obtained from the other Bandgap reference circuits that were proposed earlier are shown in table 2-1.

Table 2-1: Comparison between our design with other Bandgap reference circuit designs

	Design 1 [33]	Design 2 [34]	Design 3 [35]	Our design
Technology	0.25 µm CMOS	65nm CMOS	1.5µm BCD (Bipolar-CMOS-DMOS)	180nm TSMC
Supply voltage	0.8 V to 1.2 V	1.7V to 3.6V	6V to 18V	1.8V to 2V
Output reference voltage	238.2 mV	1.208V	2.5V	1.2V
Temperature range	-10 to +120 °C	-40°C to+125°C	-15°C to +85°C	-55°Cto+165°C
Temperature coefficient	58.1 ppm/°C at 0.85V supply	3ppm/°C at 1.7V supply	16.4ppm/°C 15V supply	241ppm/°C
Line regulation	-	-	26.7µV/V	177.5mV/V

2.8 Summary

A BGR circuit provides a low reference voltage that is independent of temperature, process and supply for a wide range of temperature of -55°C to +165°C. This chapter explored various topologies that were combined together to build a supply, process and temperature immune reference circuit. Firstly, a basic supply independent circuit with an active load was designed and realized. Secondly, this supply independent circuit is attached with components that work together to form a temperature independent circuit. A PTAT current is generated that is required to bias external circuitries.

Although it is practically impossible to build such circuits, but variations in reference voltage with supply, temperature and process can be minimized into a satisfactory level. From the simulation result, it was evident that the BGR circuit depends negligibly with process but it depends on supply & temperature to some extent. How much this reference varies with supply & temperature was compared with other proposals. The following chapters will elaborately discuss the impact of varying reference voltage with process, supply & temperature and how this variation can be subside to build a close to ideal BGR circuit.

CHAPTER III

3 Operational Amplifier

3.1 Introduction

This chapter focuses on the design of a differential amplifier circuit using CMOS technology. A differential pair or differential-amplifier configuration is the most widely used building block in analog integrated circuit design. Starting from low distortion Wien bridge oscillator [25] to multiple functions filters [26], the comparators [27], the integrators [28], the differentiators [29] and power boosters [30] employ the differential-amplifier to attain their respective purposes. This chapter shortly discussed the construction of a two stage differential-amplifier circuit [31]. The two stage amplifier with a gain of around 70dB is designed to demonstrate the adverse effect of varying reference output voltage on its dc open loop gain [32]. The change in the gain of the amplifier with the changing reference is verified through the simulation results. Finally, the chapter is terminated through the discussion on few issues that have severe impact regarding the change in the gain of the amplifier.

3.2 Two stage differential-amplifier

The first stage (also called input stage) is usually required to provide a high gain and also a high input resistance in order to avoid the loss of signal level when the amplifier is fed from a high resistance source. The second stage (also called the output stage) is used to provide a low output resistance in order to avoid loss of gain when a low-valued load resistance is connected to the amplifier. Also, the output stage should be able to supply the current required by the load in an efficient manner, that is, without dissipating an unduly large amount of power in the output transistors. One of the biggest benefits of the two-stage approach is that the net open loop gain can be achieved with two distinct stages, thereby eliminating much of the complexity involved in designing a single gain stage and leaving the distribution of gain in each stage up to the designer's discretion. Furthermore the first-stage does not have to drive the large capacitive load at the output of the second stage. The most logical approach would be to have a large gain in the first stage and a small gain and high swing in the second; the rational being that low second stage gain would not greatly amply first stage noise and high swing would give better dynamic range. One disadvantage of the two-stage approach is the decrease in speed and stability. This is attributable to the additional non-dominant pole introduced by cascading two stages.

3.3 Designing procedure

Usually the design of a two stage operational amplifier follows a basic procedure. The proper operating point (Quiescent point) is selected by first developing a single ended Op Amp. This single ended Op Amp gives the information of the biasing current to which the MOS devises operate in saturation. This condition is necessary because a MOS device acts an amplifier only it is operating in saturation. The next step is to add a replica of the single ended circuit as shown in the figure 3.1. The sources of the input MOS devises (M_1 and M_2) are

connected together and an active current source, M_5 is connected to ensure a constant current through it which is twice the operating current of the single ended circuit. The input MOS devises are connected with active (current source) loads, M_4 and M_3in order to achieve a much higher voltage gain as well as savings in chip area. Although almost every designers follow the same basic procedure to design an Op Amp but due to lack of time we developed the input stage altogether. Starting with the typical values of the W/L ratio of the MOS devises, we adjust the ratios to optimize the condition necessary for the devices being in saturation. To obtain our goal, fingering or in other word paralleling of the MOS devises is introduced in order to reduce the MOS resistance. The fingering of the devices is necessary owing to the fact that TSMC MOS device has a width limitation of 90 micrometer. If higher width is required for the design then fingering is essential. In our design, fingering is done with biasing current source, M_5 to keep this in saturation. Several adjustments such as W/L ratios, fingering and most importantly the input voltages of M_1, M_2 and $M_5$are made to meet the condition for MOS devices to be in saturation and to have a voltage of around 1V at the drains of M_3 and M_4. The fulfillment of this condition ensures that the Op Amp will have a good output swing (since V_{DD} = 2V).

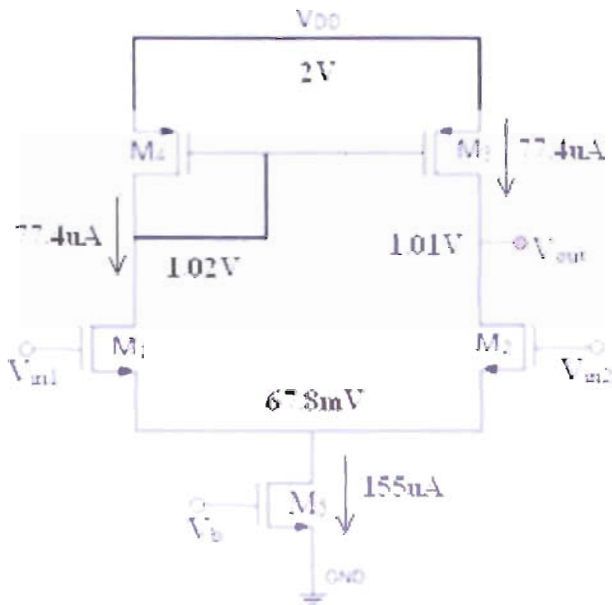

Figure 3-1: Input stage Op Amp

The next step is to add an output stage as shown in figure 3.2 to increase the overall open loop dc gain of the amplifier circuit. The MOS M_7 is biased from an external biasing circuit not shown in the figure. The MOS devices in the second stage are also needed to be in saturation so the W/L ratios and also the biasing voltage, V_{b2} are selected such so as to keep the devices in saturation. It is ensured that the output voltage, V_{out} node should be close to around 1V to ensure maximum swing. Although the optimization of the swing doesn't prove so helpful for our purpose at present, since we work with the open loop dc gain only, but this design will be used later for our future development purpose.

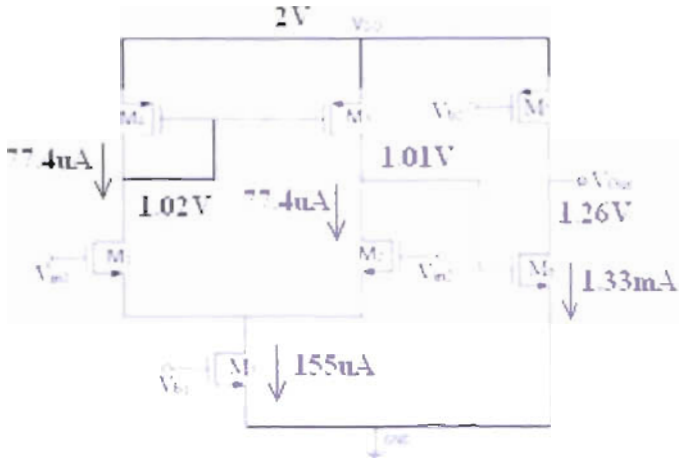

Figure 3-2: Two stage Op Amp.

3.4 Simulation results

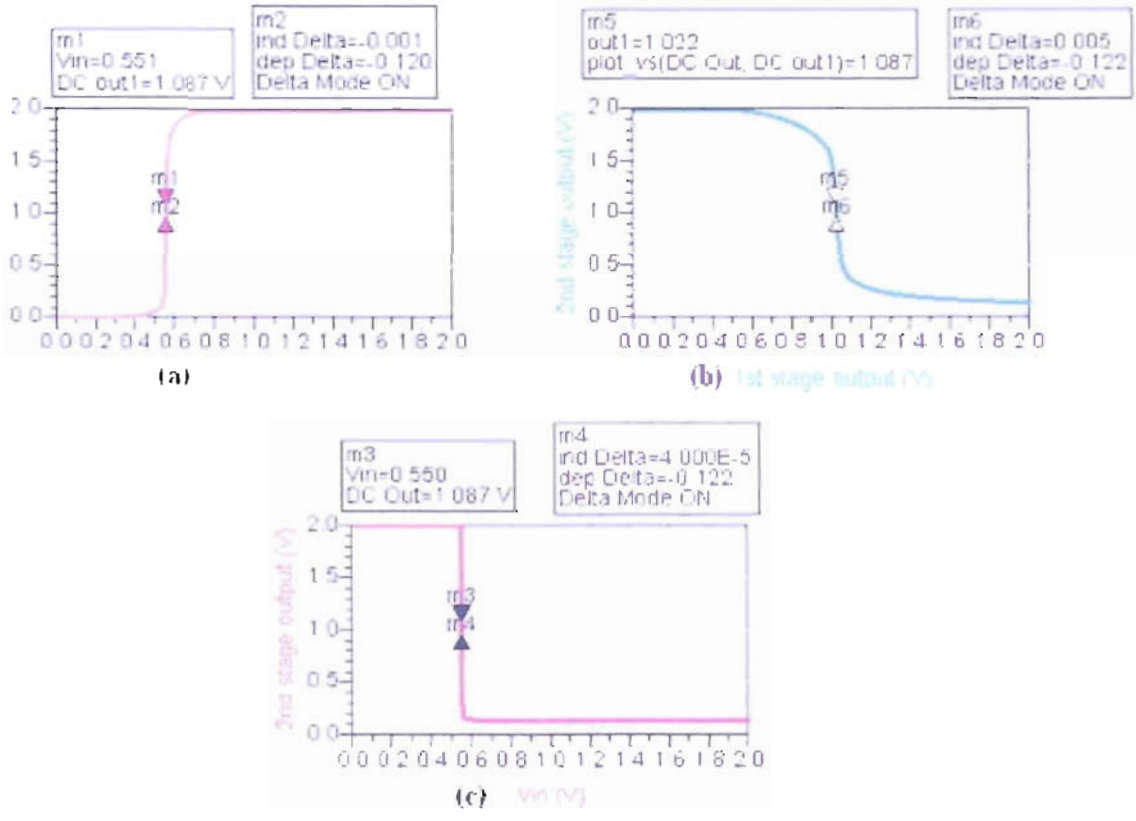

Figure 3-3: Variation of output voltages with respect to the inputs of different stages of the Op Amp for the biasing voltage of 1.2V at 27°C (a) 1st stage (b) 2nd stage (c) overall voltage variation

Table 3-1: Differential gain for biasing voltage of 1.2 V at 27^{0}C

	V/V Scale	dB Scale
1st stage gain	120	41.6
2nd stage gain	24.4	27.7
Overall gain	3050	69.7

The table 3-1 summarizes the gain of the Op Amp at different stages. For a reference voltage of 1.2V, the Op Amp has an open loop gain of around 70dB. The input stage has a gain of around 42dB and the gain stage or the output stage has a gain of around 28dB at ambient temperature.

3.4.1 Effect of Temperature variation

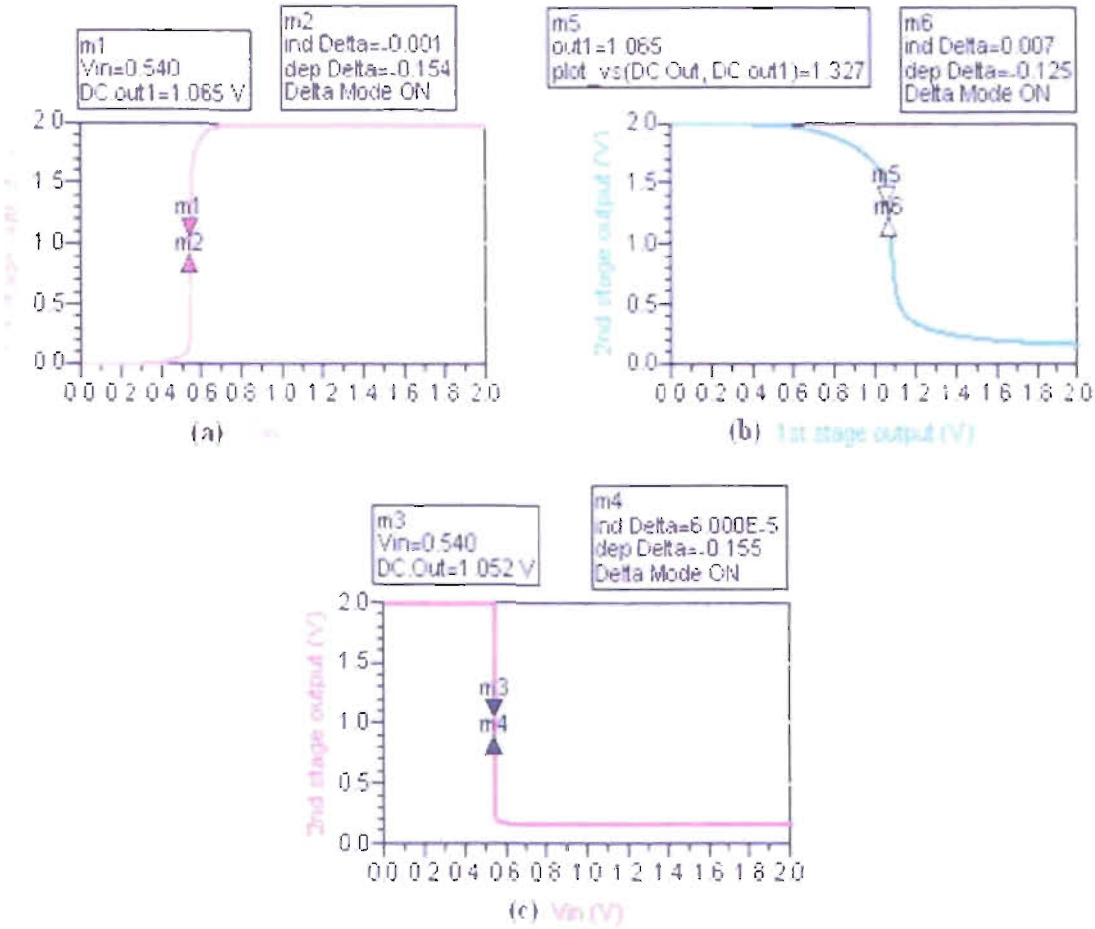

Figure 3-4: Variation of output voltages with respect to the inputs of different stages of the Op Amp for the biasing voltage of 1.229V at +165^{0}C (a) 1st stage (b) 2nd stage (c) overall voltage variation

Table 3-2: Differential gain for biasing voltage of 1.229 V at +165^{0}C

	V/V Scale	dB Scale
1st stage gain	154	43.8
2nd stage gain	17.9	25.04
Overall gain	2583.3	68.2

When the reference voltage has increased due to rise in temperature the open loop gain of the amplifier has dropped to around 68dB as can be seen from the table 3-2. In V/V scale, this variation is around 15%.This is the maximum possible variation in gain of the Op Amp when temperature rises from 27^{0}C to 165^{0}C.

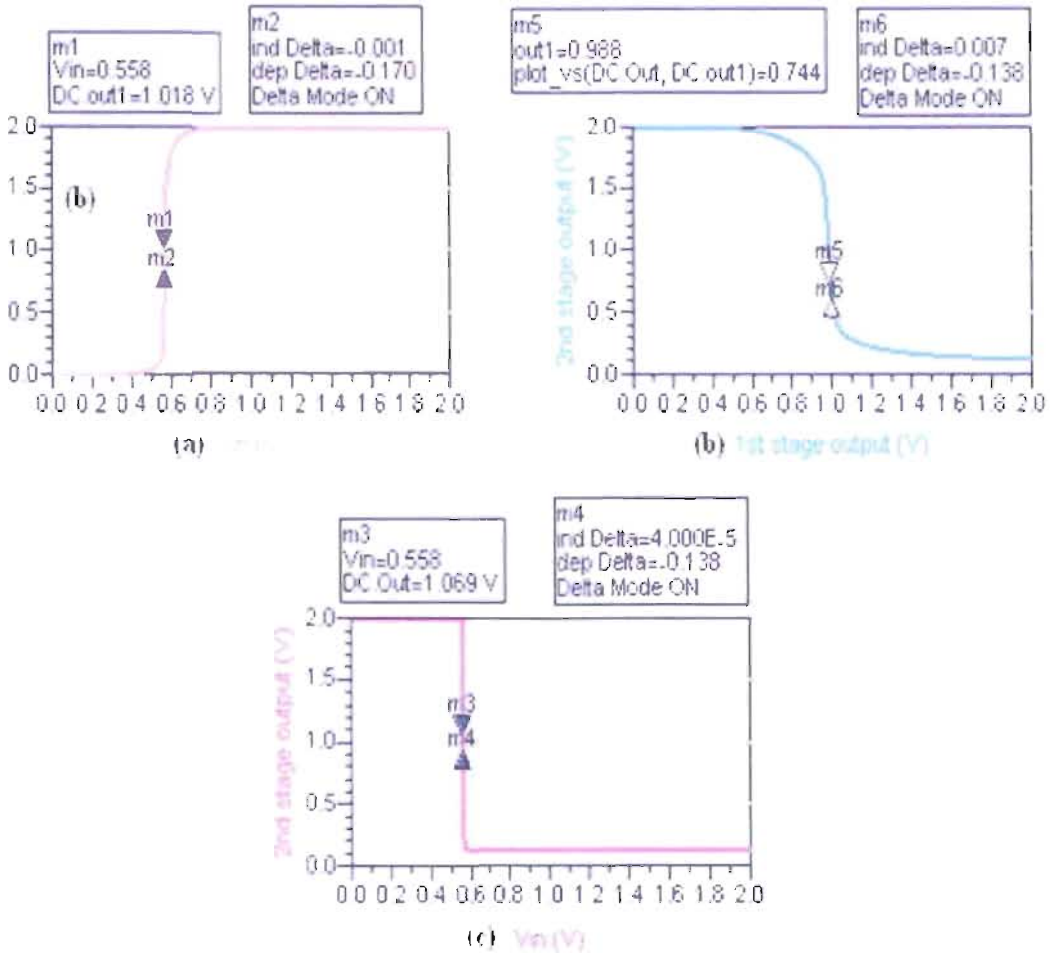

Figure 3-5: Variation of output voltages with respect to the inputs of different stages of the Op Amp for the biasing voltage of 1.176V at -55^{0}C (a) 1st stage (b) 2nd stage (c) overall voltage variation

Table 3-3: Differential gain for biasing voltage of 1.176 V at -55^{0}C

	V/V Scale	dB Scale
1st stage gain	170	44.6
2nd stage gain	19.7	25.9
Overall gain	3450	70.8

When the reference voltage has decreased due to fall in temperature the open loop gain of the amplifier has raised to around 71dB as can be seen from the table 3-3. In V/V scale, this variation is around 13%. This is the minimum possible variation in gain of the Op Amp when temperature decreases from 27^{0}C to -55^{0}C.

3.4.2 Effect of Supply variation

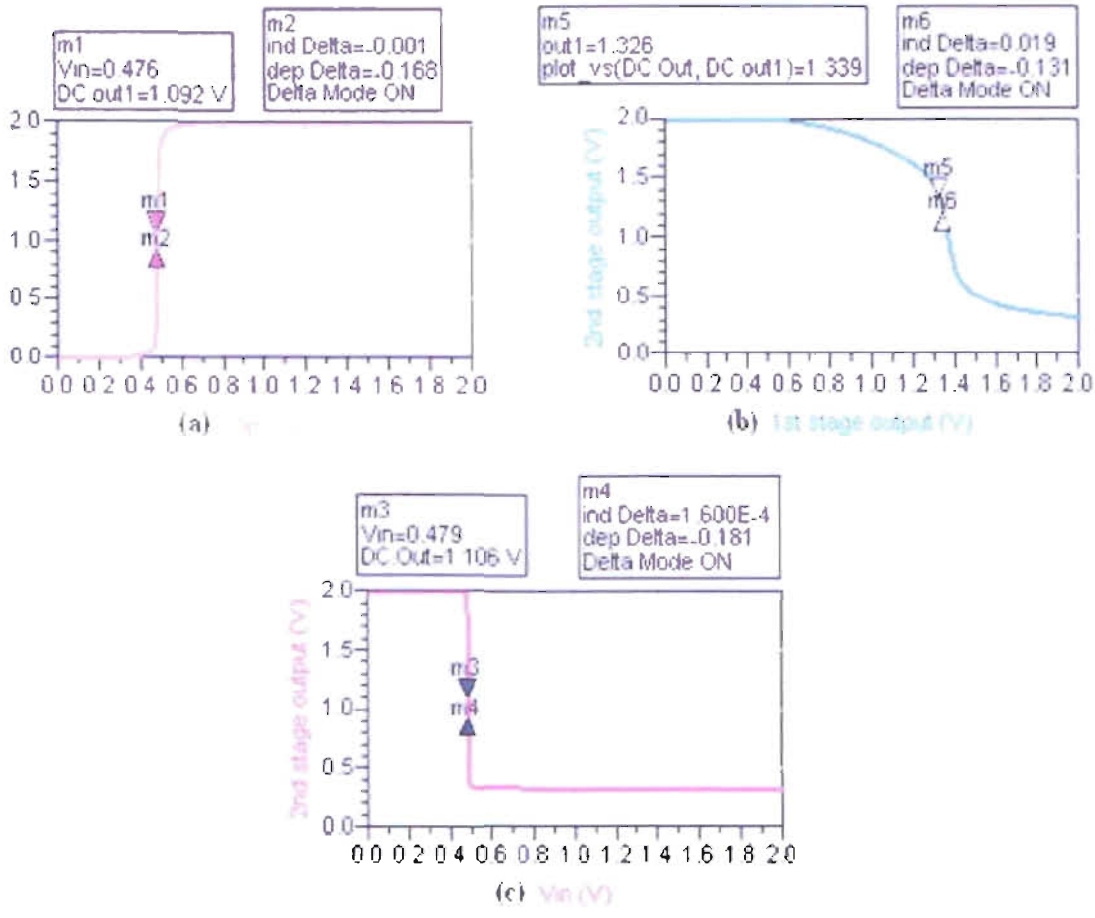

Figure 3-6: Variation of output voltages with respect to the inputs of different stages of the Op Amp when the supply voltage is increased from 2V to3V (a) 1st stage (b) 2nd stage (c) overall voltage variation

Table 3-4: Differential gain for increasing supply voltage by 1 V

	V/V Scale	dB Scale
1st stage gain	168	44.5
2nd stage gain	6.9	16.8
Overall gain	1131.3	61.1

The supply variation has significant impact on the gain of the amplifier. The table 3-4 summarizes the result, where it can be seen that when the supply voltage is increased by 1V the gain of the amplifier drops to 61dB. This variation is around 63% in V/V and when the supply decreased by 1V the gain increased to 7000V/V, as can be seen in table 3-5, which is quite a large amount.

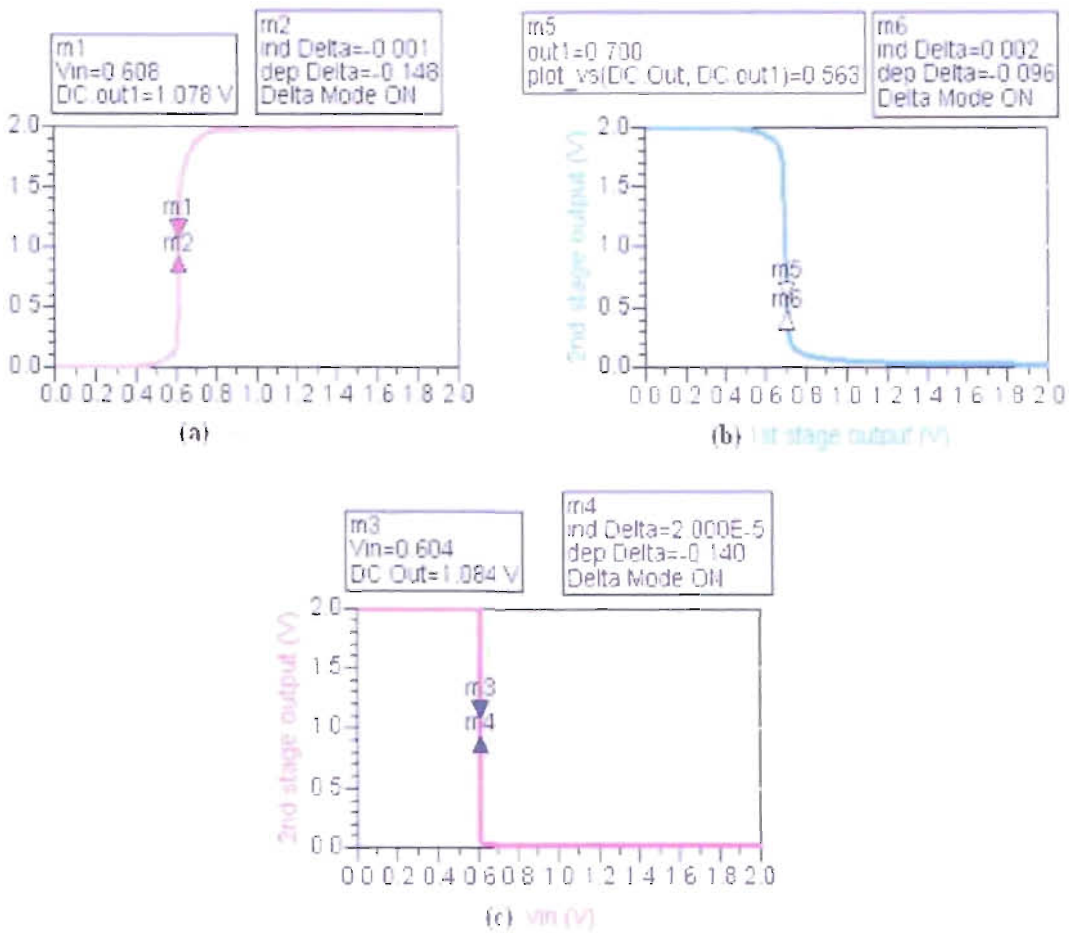

Figure 3-7: Variation of output voltages with respect to the inputs of different stages of the Op Amp when the supply voltage is decreased from 2V to 1V (a) 1st stage (b) 2nd stage (c) overall voltage variation

Table 3-5: Differential gain for decreasing supply voltage by 1 V

	V/V Scale	dB Scale
1st stage gain	148	43.4
2nd stage gain	48	33.6
Overall gain	7000	76.9

3.5 Summary

Our purpose of designing a high gain Op Amp was to show the negative impact on the external circuits such as differentiator, integrator and power booster etc. The simulation result showed that for a small variation in the reference voltage can cause a significant change (13%-15% for temperature variation & 60%-130% for the supply variation)in the gain of the amplifier. This large percentage change in the gain will obviously impose a devastating impact on the external circuits. For instance, if this reference circuit is used in system such as power booster then a small variation in the reference due to temperature or supply can cause the system less efficient. If the gain of the Op Amp is reduced, then the power booster may not be able to amplify the transmitted signal, in order travel a desired distance, rather it will attenuate the transmitted signal significantly. As a result the signal will be lost after travelling a small distance. On that case, the BGR circuit in the power booster has to be changed so that the amplifier can work properly otherwise more power boosting antennas will be required which will ultimately increase the cost. In case, the gain of the amplifier is increased due to decrease in supply and temperature then a highly amplified signal may add noise into the system.

In oscillator, the effect of varying gain is very critical. If the gain of the Op Amp changes for some reason then the oscillator circuit may not be able to generate a desired voltage for a particular frequency. There are the few adverse effects on external circuits that might occur if the reference circuit prone to vary with supply, temperature and process. So we need to propose a design of BGR circuit that is immune to temperature, supply and process variation. The next chapter will discuss how BGR circuit can be made temperature, process and supply independent by proposing circuits that work using negative feedback mechanism.

CHAPTER IV

4 Proposed Bandgap Reference Circuit

4.1 Introduction

The last two chapters of the report deal with the design of a Bandgap reference circuit and the effect of varying reference voltage or current on the other analog circuits. No doubt, a constant reference voltage or current plays a vital role in the design of any analog & digital circuits so a designer always urges for a reference circuit that can provide him/her with a desired non-varying reference output.

This chapter deals with how a reference output can be made fixed even when the temperature varies. It is desirable that a reference circuit should be capable of generating a reference output that is independent of supply, process and temperature although our rational study on Bandgap reference circuit in chapter-2 shows that the reference can be made process independent to some extent but it has slight dependency on temperature and supply. Even though the change in reference output is in milli-range (which is very small) with temperature and supply but its impact on any sensitive circuit such as high gain Op-Amp (as discussed in chapter-3) is significant.

In order to avoid such discrepancy two modifications on the Bandgap reference circuit have been proposed which will be discussed elaborately in this chapter. The proposed circuitries use the concept of negative feedback mechanism to sense the change in the reference output and work accordingly to provide a constant output by suppressing the change.

4.2 Negative feedback mechanism

Negative feedback mechanisms are self-regulating responses to the changes experienced by a system usually due to external influences. These mechanisms feed some of the output of these changes back into the system to trigger counter-responses which result in restoring the system to its previous undisturbed state, or mitigating the effects of the initial change. It is this characteristic of 'negating' the impact of changes which defines such operations as 'negative feedback mechanism'.

4.3 First proposal

4.3.1 Circuit description

In the circuit of fig: 4.1, the current I_5 is a PTAT current so it depends on the temperature. The simulation result in chapter II shows that this current (I_5) also depends on the supply voltage as well. So, when temperature rises above 27^0C or supply increases above 2V (due to addition of noise) the current I_5 increases. The current source M_7 forms a mirror with M_5 so the current I_7 increases with increase of temperature or supply. Therefore the drain voltage of M_8 increases and hence the gate voltage of M_6. As a result, the current I_6 also increases. The greater the current through M_7, the greater will be the drain voltage of M_8 so that the same current flows through M_7 & M_8. The higher the drain voltage of M_8, the higher will be the gate voltage of M_6. As a result,

M_6 will draw more current from the reference output. Now invoking Kirchhoff's current law at node V_{out} gives,

$$I_{R2} = I_5 - I_6 \tag{4.1}$$

From equation (4.1), it can be observed that if I_5 increases then I_6 would increases proportionately keeping the current I_{R2} and hence the voltage drop across R_2 and Q_3 to its initial desired state.

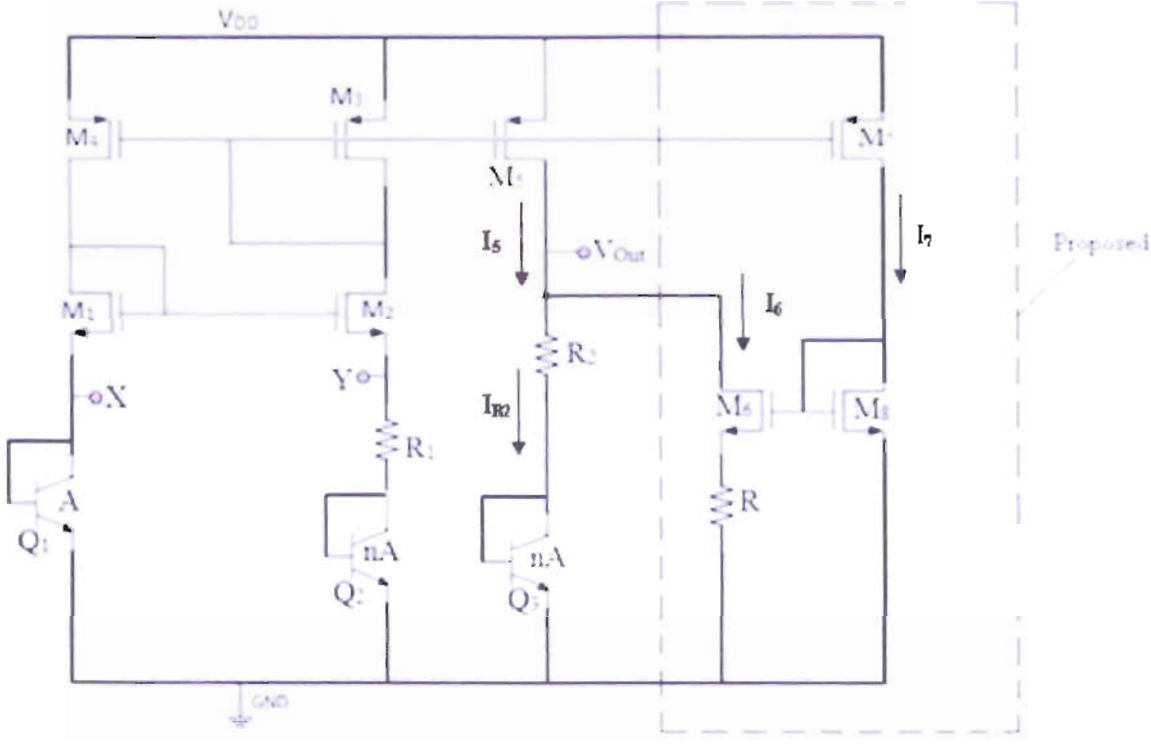

Figure 4-1: Negative Feedback mechanism to eject extra current from the reference circuit.

Theoretically, the current through M_8 & M_6 should be the same which is basically the current through M_5, but this is not what exactly we want. Our concern here is to pull out the extra current that flows when temperature is increased, from the reference output. The only way to make it possible is by making the mirroring effect of M_6& M_8 weaker. This is achieved by connecting a resistance R at the source of M_6.

4.3.2 Summary

In short, the proposed circuit above uses negative feedback mechanism to pull out extra current from the reference output and sustains the voltage level and current as it was earlier at the output. That is how, we can obtain a fixed reference output even when the temperature changes or there is any change due to process variation.

Our early proposal deals with the ejaculation of extra current which was introduced into the reference circuit due to rise in temperature. Now we shall extend our discussion by focusing on

different set-up of negative feedback mechanism in order to obtain a non-varying reference current/voltage.

4.4 Second proposal

4.4.1 Circuit Description

The set-up of figure 4.2 seems very simple & cheap but the way it works is as expensive. Even though its mechanism is complicated but the beauty of this proposal is that it simply follows Ohm's law to keep the reference output independent of temperature.

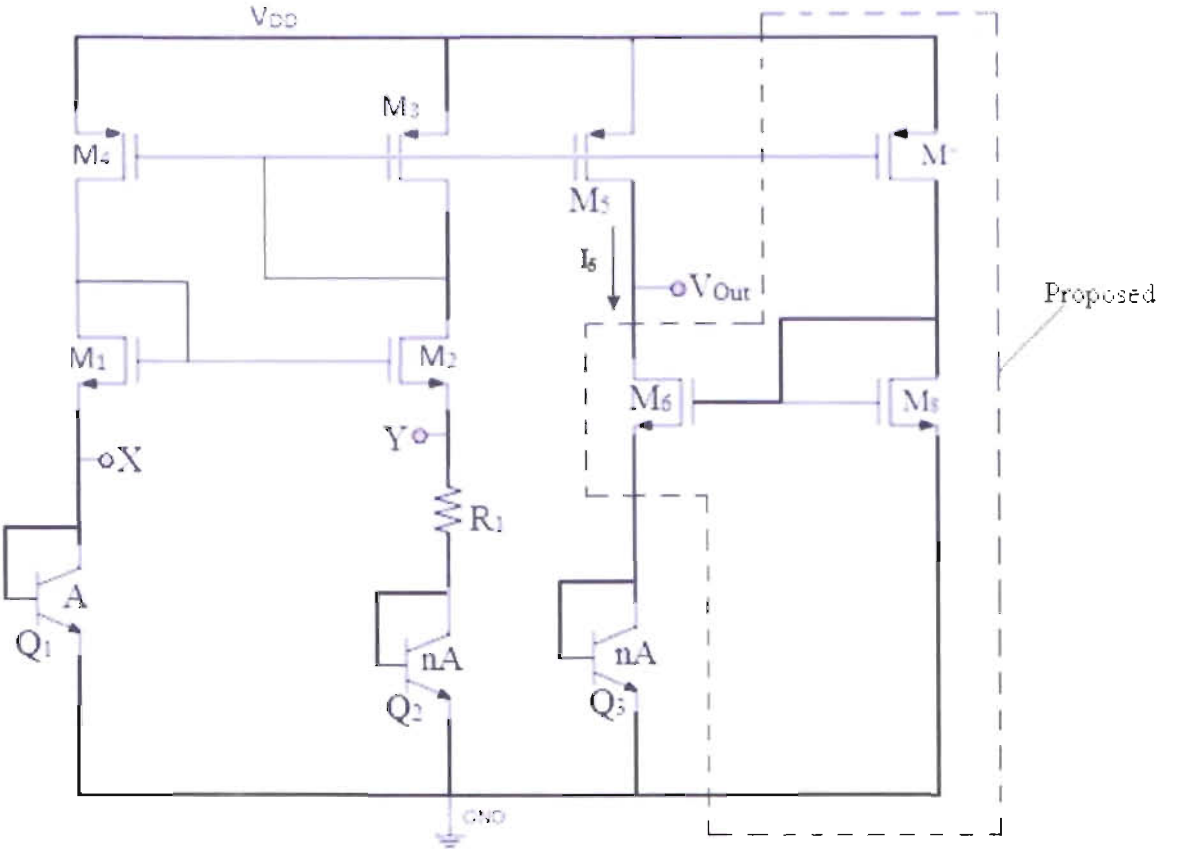

Figure 4-2: Negative Feedback mechanism to change the output resistance of the reference circuit.

For simplicity, let's consider M_6 as a resister. The idea here is that when the reference current I_5 increases, with the increase of temperature and supply, the resistance of M_6 would decreases in the same proportion keeping the voltage V_{out} to its initial desired state.

The mirroring configuration of M_5& M_7 allows the same current to flow through each branch. As the reference current increases, the current through M_7 also increases. For the series configuration of M_7 & M_8, the same amount of current should flow through them. When the current through M_7 increases the drain voltage of M_8 should increase as well which in turn increases the gate voltage of M_6. The increase in gate voltage of M_6 means the decrease in its resistance.

4.4.2 Summary

If we add up the concepts of the above proposal, then it simply states that when the PTAT current will change with temperature and supply, the MOS M_6 will sense the change and functions accordingly depending on the change. If the output current increases the resistance of the M_6 would decrease and vice versa keeping the reference voltage the same.

4.5 Conclusion

No doubt, the concepts of the stated proposals were very simple and innovative, compare to other proposals, which assimilate series cascoding [24] to obtain a stable reference output. In both cases, the objectives were to generate a temperature& supply independent reference output. The discussion for both the designs of the BGR circuit was made considering the case when the temperature rises above the ambient temperature or when the supply increases above 2V, but vice versa requires a slight modification on the above set-up not discussed in this initial stage of the design. It is expected that further analyses on the proposals will definitely meet the stated criterion. Unlike a basic BGR circuit, our design incorporates extra MOSFET devices for the sake of stable reference output and this will give rise to extra power consumption. The amount of power consumption is expected to be small enough to consider the proposed BGR circuit as a standard, stable reference generator.

CHAPTER V

5 Conclusion

5.1 Future development

The line regulation of the BGR circuit shows that the circuit still has supply dependency which can be minimized further if a better common-gate op Amp is proposed in future.

The proposals for a stable reference output were made, based upon the theoretical knowledge. Due to shortage of time, no simulations were performed for the justification of the proposals. Although the ideas of the proposals are simple but complicacy may arise while designing them. It is quite obvious that the circuits would show some anomalous behavior but it is believed at the same time, that if the circuits are designed properly with a clear understanding of their ambiguities then there is a light of hope that the proposals would meet the desired specifications.

A perpetual effort will be invested to operate the BGR circuit at a higher temperature range (above 300^0C) so that it can be implemented in systems such as satellite, space shuttle etc. This will significantly reduce the cost of the design as higher temperature devices are designed using diamond and GaAs which are expensive.

Once a suitable BGR circuit is achieved, the work will be extended further for the layout design and fabrication of the circuit.

5.2 Project summary

A typical BGR circuit was designed and simulated using Advanced Design System (ADS) tool. The purpose was to generate a reference voltage of 1.2V that is exempt to temperature, supply and process variations. The complicacy that aroused while designing was to keep the MOS devices in saturation so a proper selection of W/L ratios of the MOS devices was essential. To achieve this, trial and error method was applied to obtain an optimized W/L ratio in order to fulfill the necessary condition for the devices. Another reason for applying trial and error method was due to insufficient knowledge about the devices parameters. And because of this, the design output could not be verified by mathematical calculations. Series of simulations were carried out to study whether the design was immune to supply, process and temperature. The result showed that the design had little dependency. The simulated results were compared with the other proposed BGR circuits.

The design of the two stage operational amplifier was another great challenge. Due to shortage of time the usual design procedure was not followed rather the design was thought of as a whole and several analyses were carried out to optimize the condition, of a high gain Op Amp, as much as possible. The analyses include the adjustment of aspect ratios to keep the MOS devices in saturation; the biasing voltage of the Op Amp was properly selected in order to ensure relatively large current flow to maximize gain and also to improve dynamic output range, that is, the output voltage swing.

Finally, two mechanisms were proposed and studied to improve the BGR circuit. The mechanisms were discussed theoretically and no simulation was done for its justification due to shortage of time.

Appendix A

A.1 Advanced Design System (ADS) Tutorial

Advanced Design System (ADS) software is a powerful software used commercially to carry out various types of simulations such as Analog/RF, Signal processing, Cosimulation, Electromagnetic, Wireless test benches etc. The detail of these simulations can found in the help file of the software. We simulated different types of circuit models in ADS software such as BGR circuit & Op-Amp so handling ADS is one of the important tasks. This section of the report described about the ADS software installation process and simulation method. For our purpose we used 2008 version of the software.

A.1.1 Installation of ADS

The installation process can be subdivide into two parts such as–

1. Before installation procedure
2. Installation of license key

A.1.1.1 Before installation procedure

The ADS software is one of the largest software and it requires of about 4 GB memory space. Since a large memory space is required hence we can assume it operation is relatively slower. So certain things need to be taken into account before installation is being carried out. **Closed your Internet connection**, **Shutdown or turn-off your anti virus** are the most important tasks that must be performed before intallation. After taking care of the above taskes one have to follow the basic guide lines for the installation of ADS.

A.1.1.2 Installation of license key

After succesfully install the ADS software one have to install the license key and the installation procedures of the of license key are given below -

i. Go to the *'Agilent_ADS_2008/crack'* folder and copy ***'agsl33.dll'*** and ***'license.lic'***. And follow the next steps.
ii. Paste the both file ***'license.lic'***.and ***'agsl33.dll'*** following direction...

a) **D:\ADS2008\bin**

b) **D:\ADS2008**

Here a) < Setup drive>:\<Folder name>\bin

b) < Setup drive>:\<Folder name>

Note:In example drive location is **D:** and ADS setup folder name is **ADS2008**.

iii. Paste the Only ***'licence.lic'*** following direction.....

a)**D:\ADS2008\licenses\bin**

b)**D:\ADS2008\licenses**

A.1.2 Simulation process in ADS

In this section we tried to describe how to simulate a circuit in ADS. This process contains many steps such as **opennig a project file, how to install a design kit** and **creating circuit in ADS** etc. First we have to open the ADS software "Advanced Design System" which is shown in first figure (figure A.1).

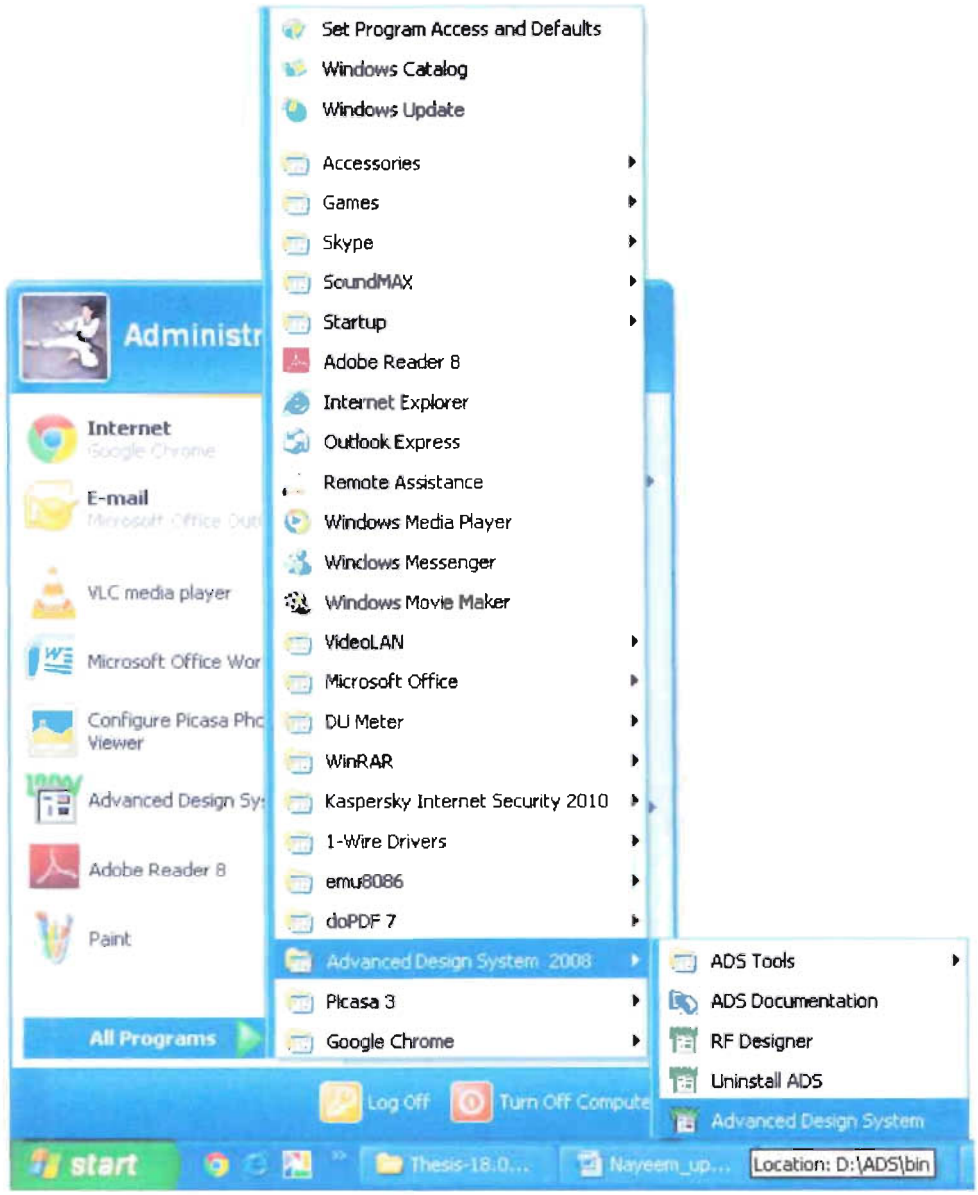

Figure A-1: Opening of the ADS

After opening of the ADS software the "Getting Started with ADS" window will appear. Now we have to select "**create a new project**" or "**open an existing project**" or "**open an example project**".

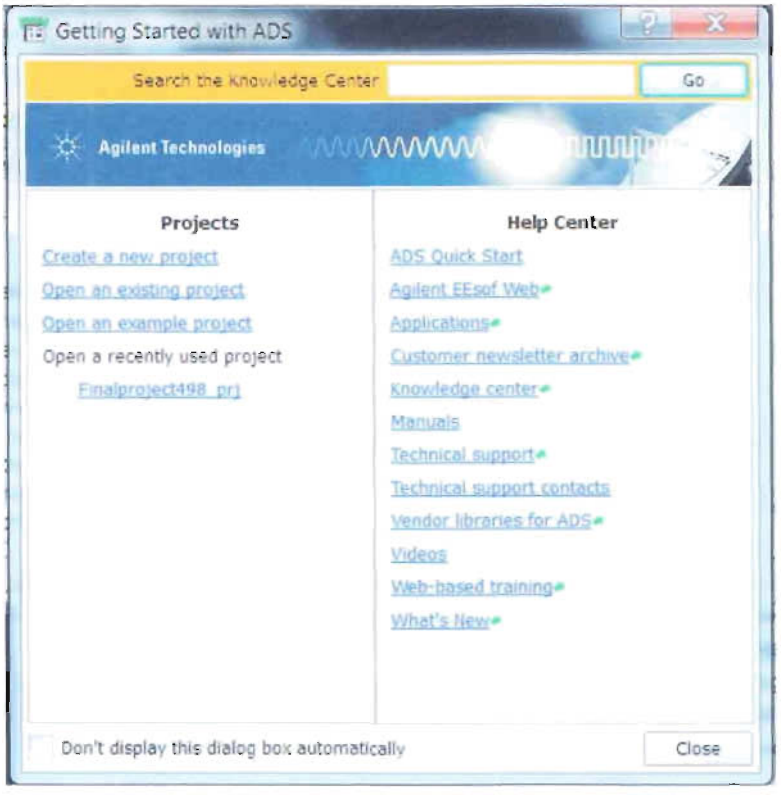

Figure A-2: How to start in ADS

A.1.2.1 Creating a Project in ADS

After opening, the main task is to create a project in ADS. For creating a project we have to click the "**create a new project**" option then a window named "New Project" will appear. In new project window we have to put the project name in the "**name**" option as shown in fig: A.3 and by changing the "Project Technology Files" we can select technology size of the devices (such as MOSFET, BJT etc) for simulation. Now that we have created a workable project hence we are ready to do our simulation.

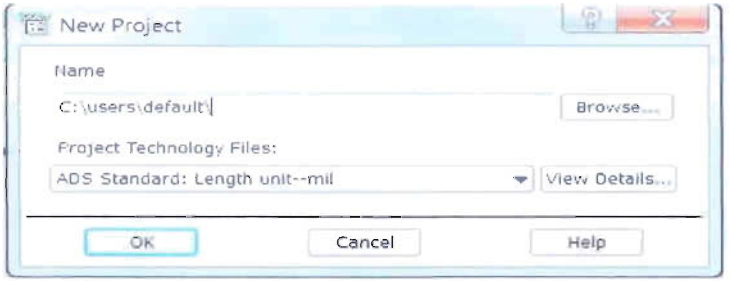

Figure A-3: Window for creating a new project in ADS

A schematic wizard will appear, as shown in fig: A.4, which needs to be closed but before closing the wizard we need to tick the "**do not show this dialog again**" button for the permanent removal of this schematic wizard. Now we are able to create our desired circuit in "[name_prj] untitled1 (schematic):1" as shown in fig: A.5.

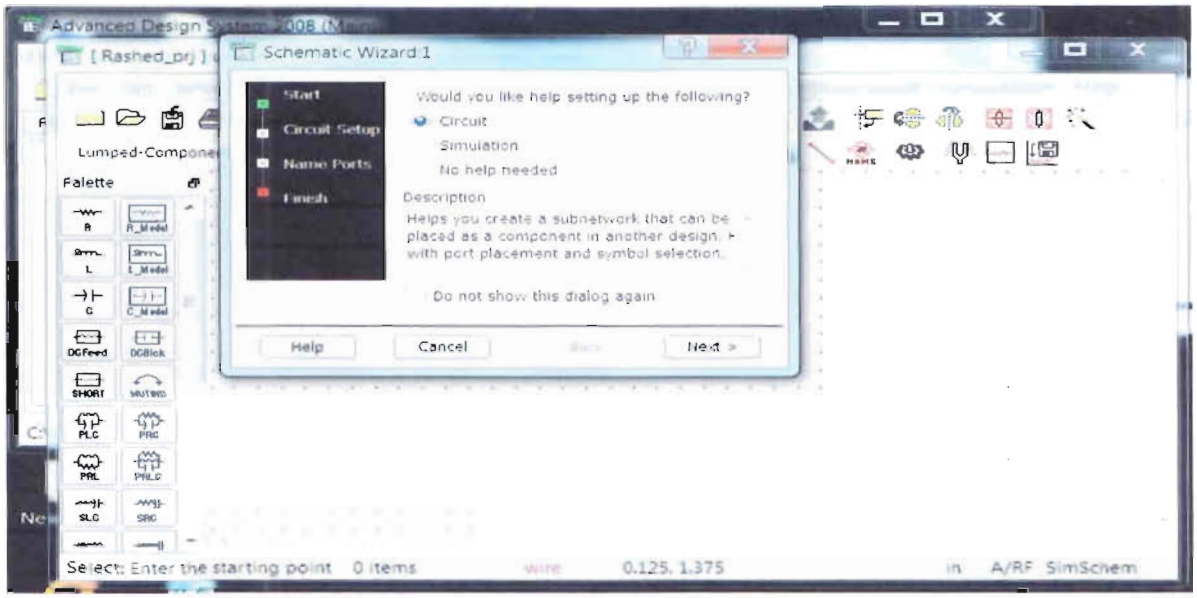

Figure A-4: Schematic Wizard after creating Project

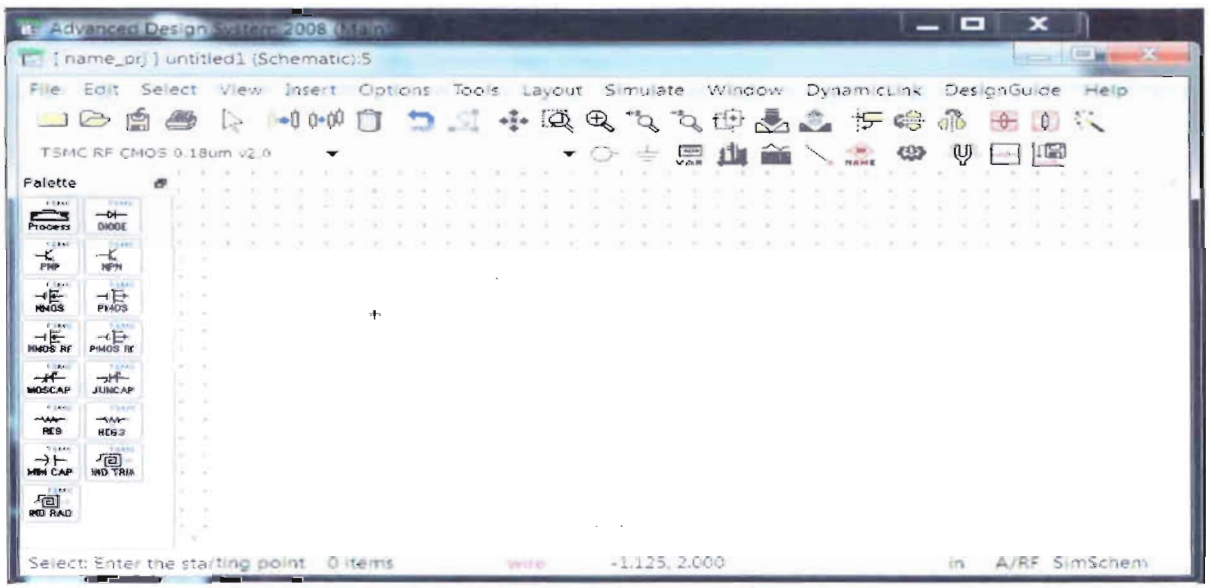

Figure A-5: Window for circuit design

A.1.2.2 Installation of the design kit

In ADS, a design kit is needed when we try to design a circuit for a specific technology such as tsmc_cm0.18 (Taiwan Semiconductor Manufacturing Company that provides designer with 180nm device for the design). So we need a prepared designed technology which is provided by a company or institute. In our thesis we use "tsmc_cm0.18" model which that provides a device of minimum width of 180 nm. To carry out our task with this "tsmc_cm0.18" model we need to install the design kit in ADS. In design kit installation process, first we have to go to "**Advanced design system 2008 (main)**" window and then select "**design kit**" option and click the "**install design kit**" button as shown in fig: A.6.

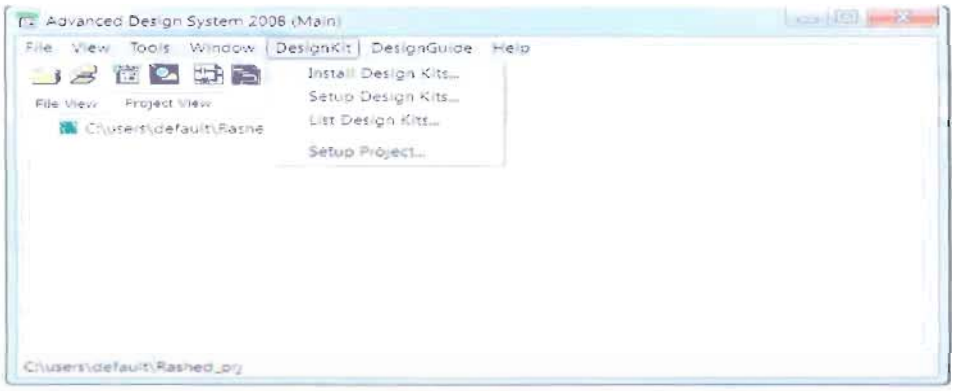

Figure A-6: Installation of the design kit

After clicking the "**install design kit**" button, the "**install ADS design kit**" window as shown in fig: A.7, will appear. In this window there are many options such as "**unzip design kit now**" and "**path**" etc. If we need to unzip design kit, then we have to use this option "**unzip design kit now**" or we can manually unzip the design kit by using zip file extract software. And then define the path of the unzip design kit, but we do not need to define the "name" or "boot file" or "version" because after selecting a design path all type of data will be taken automatically.

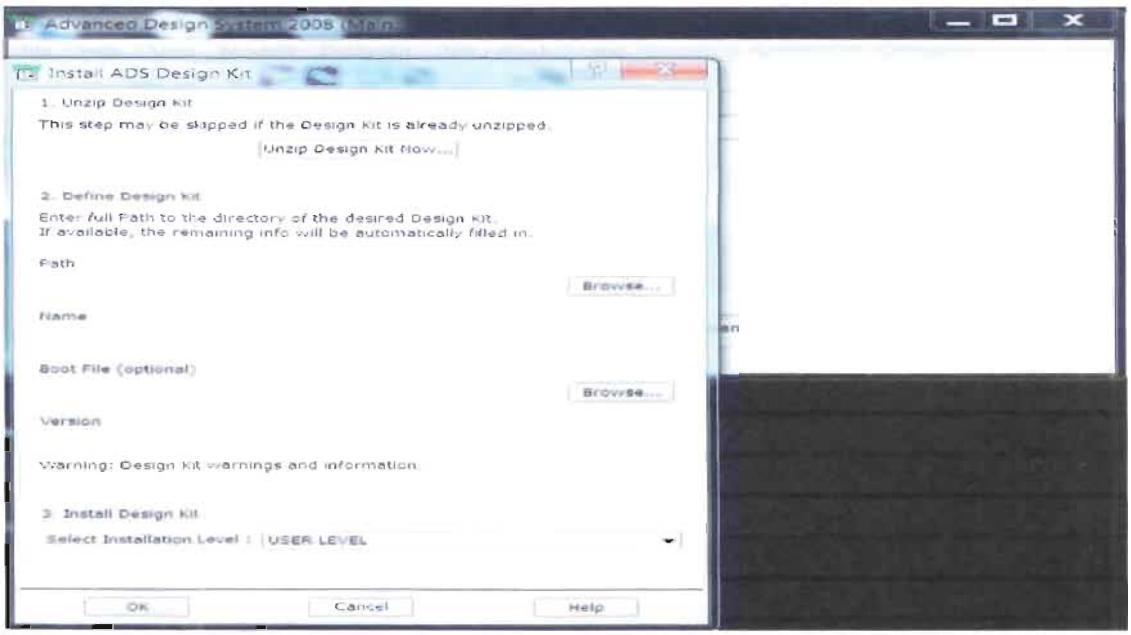

Figure A-7: Window for the installation of Design kit

In the unzip process of the design kit, we have to define the directory of the unzip design kit file and we have to define the file where we want to save design kit for future use as shown in fig: A.8.

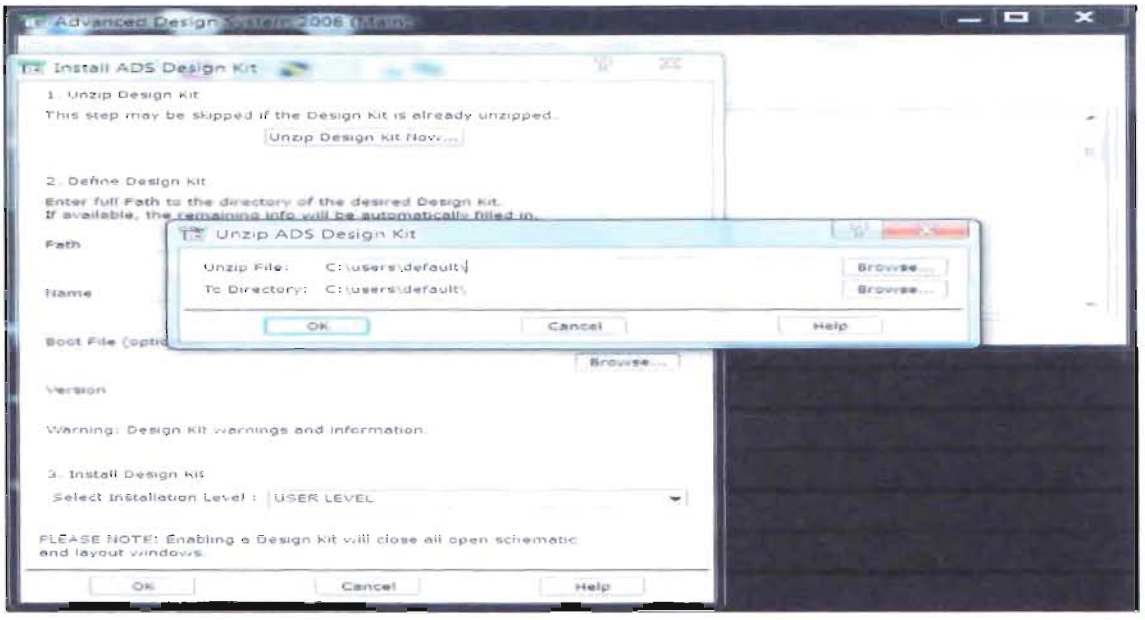

Figure A-8: Installation process for unzip design kit

Previously we said that we can manually install the design kit in ADS and the option of the manual installation is "**define design kit**" (fig: A.9). Here we just have to define the path of the saved and unzipped design kit because all other options will be taken automatically the software. If we want to install design kit for different user level, we will use the "**install design kit**" option to change the user level. In default process "**user level**" is defined by automatic process (fig: A.9).

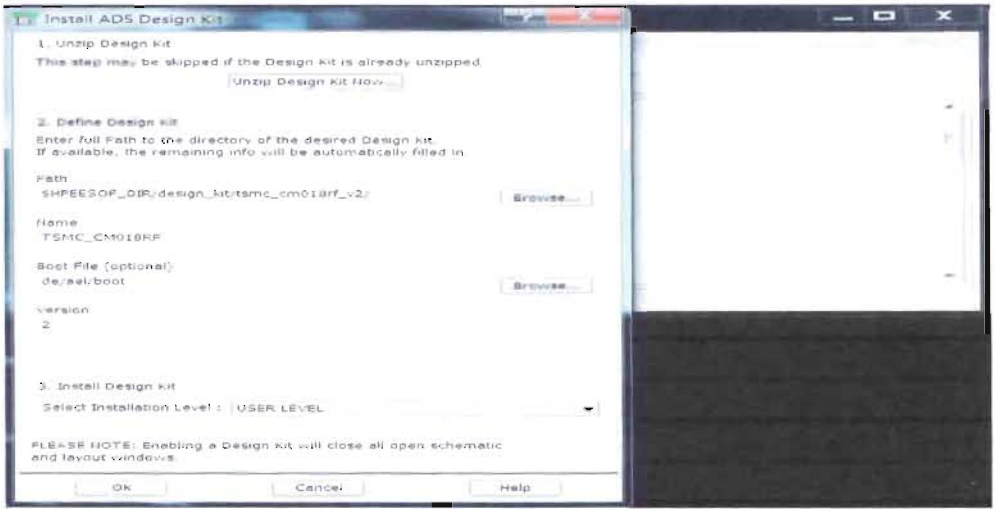

Figure A-9: Defining a design kit

A.1.2.3 Design in ADS

In ADS, "[name_prj] untitled1 (schematic):1" is used to design a circuit or we have to re-open new schematic from the main page. For opening a new schematic we have to

click "**window**" then "**new schematic**" or in the main window the new "**schematic window**" button can be used to open the new schematic (fig: A.10).

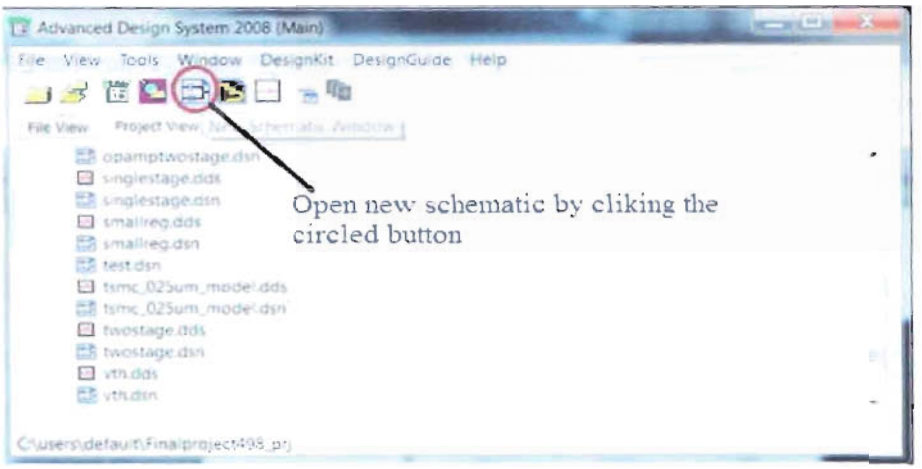

Figure A-10: A new schematic window for designing in ADS

Now we are ready to design a circuit. For designing purpose we have to select the palette option, to design a circuit in ADS, by choosing the necessary component such as MOSFET, BJT, and Resistor etc, required for the design (fig: A.11). For simulation, a source is needed which could be either a voltage or current source to; the simulation source and type can also be found in palette option. To vary the circuit component or source such as DC voltage source, a variable is needed to be declared (fig A.12) and on that case we need to select variable option. To connect two different components, we have to use insert wire option. Now that we have draw the desired in the schematic window hence we are able to simulate the circuit and for that we have click "**simulate**" option. By using "**new data display window**" we'll be able to see the plotted data or figure which must be saved before or after simulation.

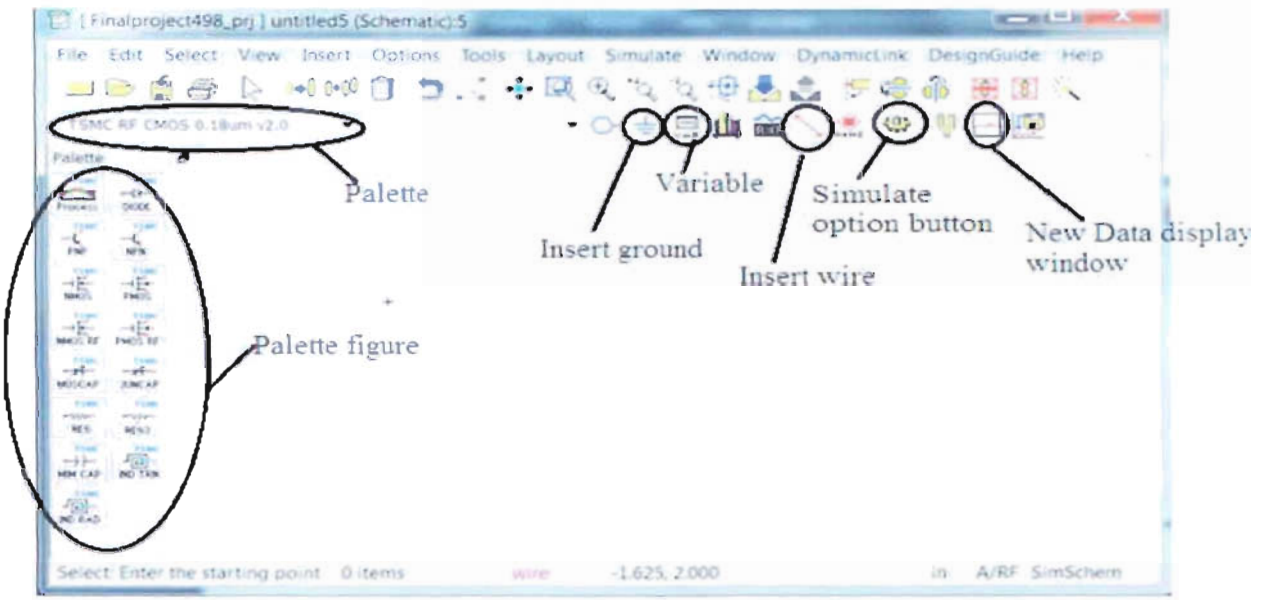

Figure A-11: New schematic to design a circuit

A complete circuit is created in schematic as shown in the fig: A.12. Here "TSMC RF CMOS 0.18um" is the net list included file, where total modeling process of the 180nm technology is included in this model file. Current probe is used to measure the current of this branch and 'V_DC' is the fixed DC source. Here for DC analysis we define a DC variable as 'VDD' by using variable DC1 source. In variable DC source we put the variable name and vary the value for the DC analysis. Since we declare 'VDD' as a variable, so we have to initialize the VDD by using 'VAR' palette. 'VAR' is needed for different purpose which will be discussed later. Practically any device is temperature dependent and if someone desires to see the effect of the varying temperature in the circuit then one have to simulate this circuit by varying the temperature. For using temperature as variable, DC2 variable is used, as no other palette can be defined in ADS for temperature variable. And we don't need to define an initial value for temperature as temperature is not the source in our circuit. If we want to know the voltage at different nodes, then we have to define node by clicking **"Define node".**

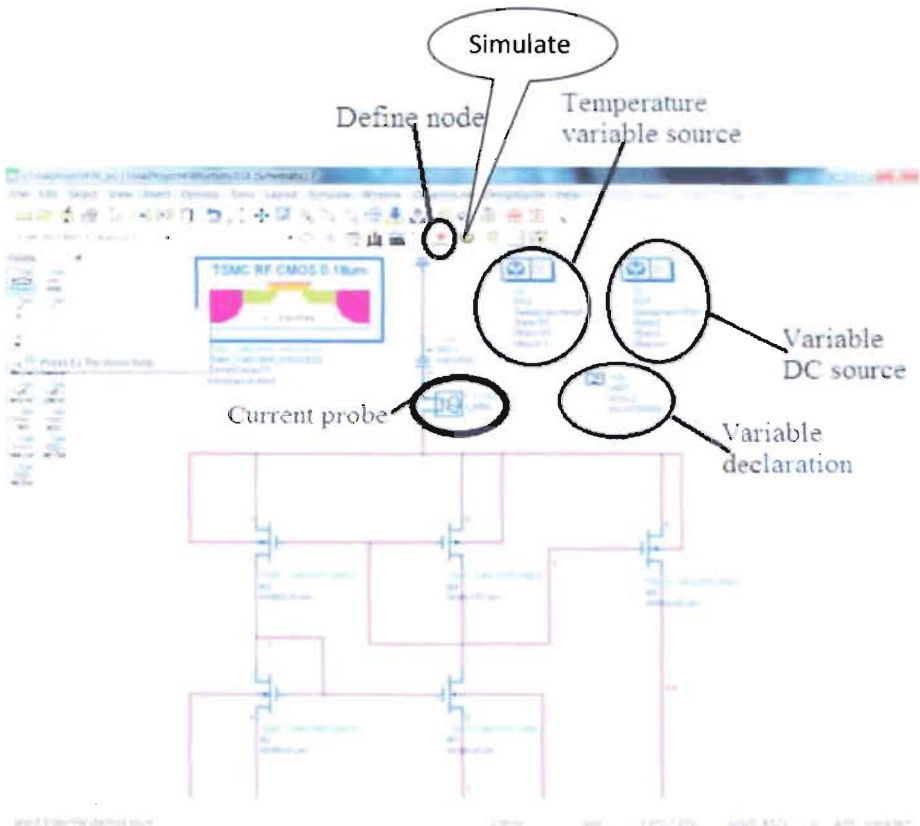

Figure A-12: A test circuit designed in ADS Schematic

A.1.2.4 Simulation in ADS

As we are done with the design now we have to click simulate button to carry out the simulation as show in the fig: A.12. After simulating the circuit, the "name[page 1]:0" window (figure A.13) will appear where we can plot the different types of figures. To plot the data at different nodes of the circuit we have to use palette as shown in left side of the window of the fig: A-13.

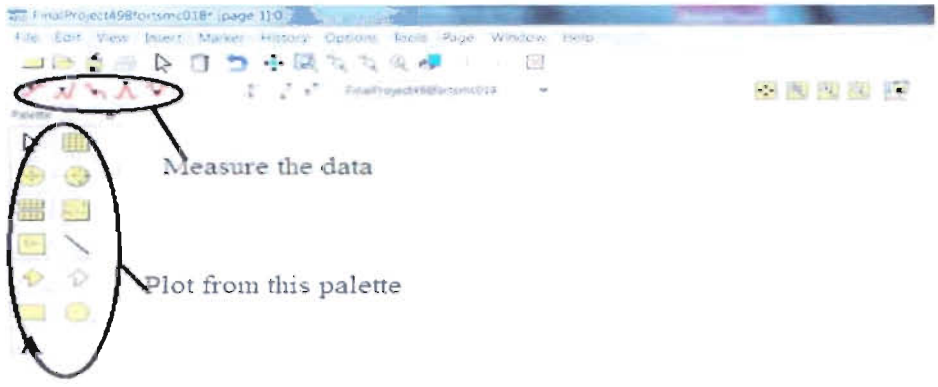

Figure A-13: A window for plotting the simulated result.

In schematic window we have '**simulate**' option, if we click this option many sub options will appear in the window such as Simulate, Annotate DC simulation and Detailed Device Operating

Point etc as shown in the fig: A-14. If the DC value of all nodes of the circuit is needed then we have to click the "**Annotate DC simulation**" option and to see the node voltages for the particular condition in the circuit, the circuit need to be initialized with a particular value. The annotate dc value at different nodes will appear in the circuit diagram after the circuit has been simulated. The software measures this dc value depending on the initial value given in the "**var**" (in this case 2 is used to initialize). We can also check the detailed operating point of the device by using "**Detailed Device Operating Point**" (fig: A-14).

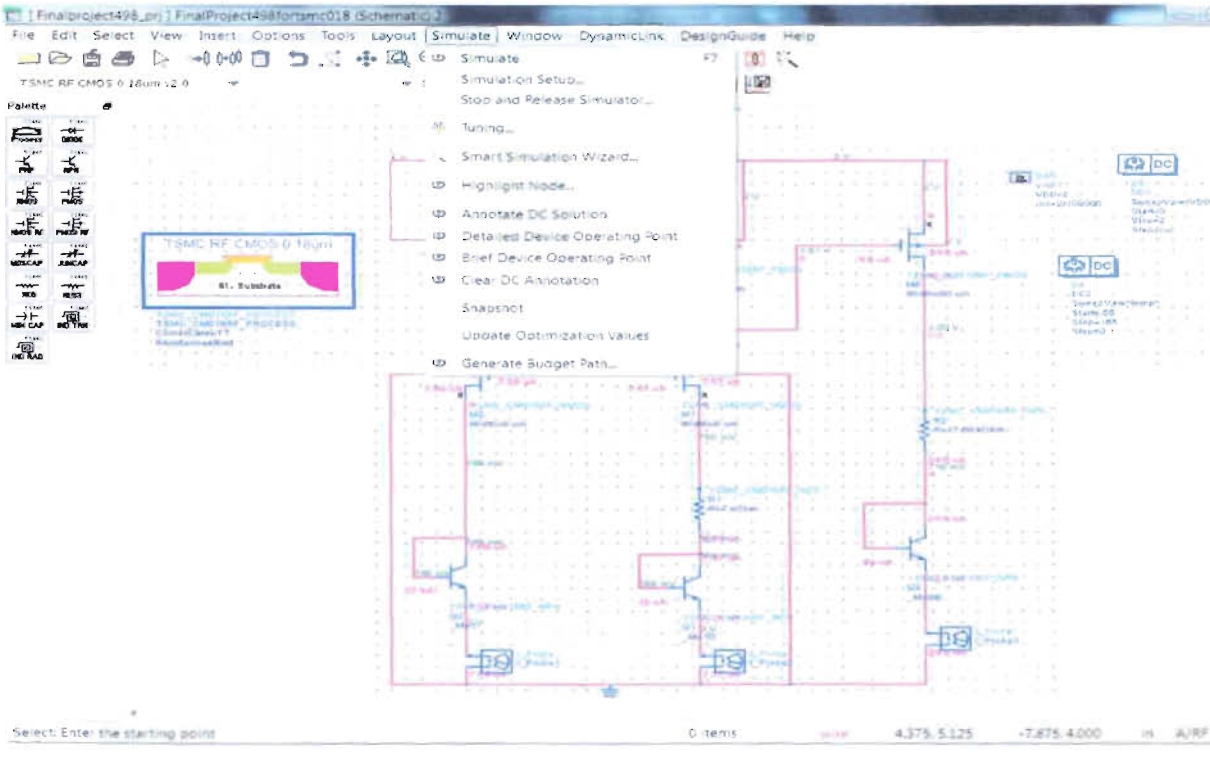

Figure A-14: Various simulation options for the design.

Now we have to plot the data in data window by using the gridded rectangular plot from the palette. In the plot we need to the put the marker to determine the different values of the simulated result (fig: A.15). In order to determine the difference between the two points in the plot we need to go to the properties (fig: A.16) of the marker and define the reference of the marker with respect to the other. For separate plot we have to define different reference to get the proper result.

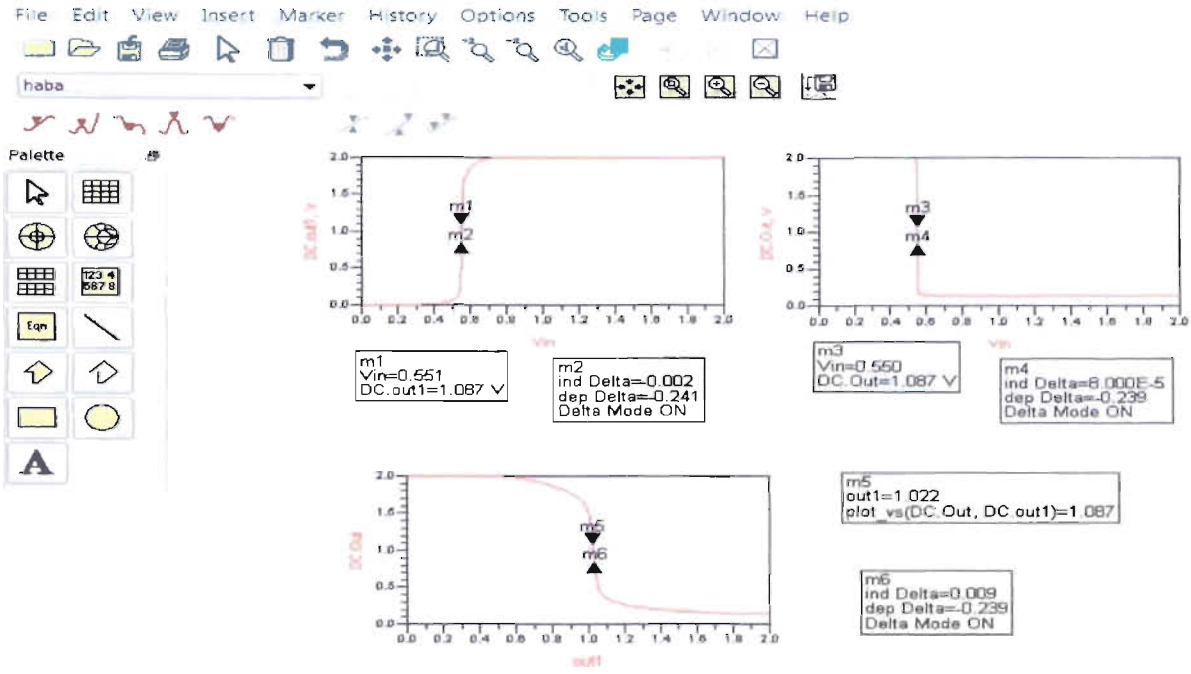

Figure A-15: Different types of graphs plotted in the plot window

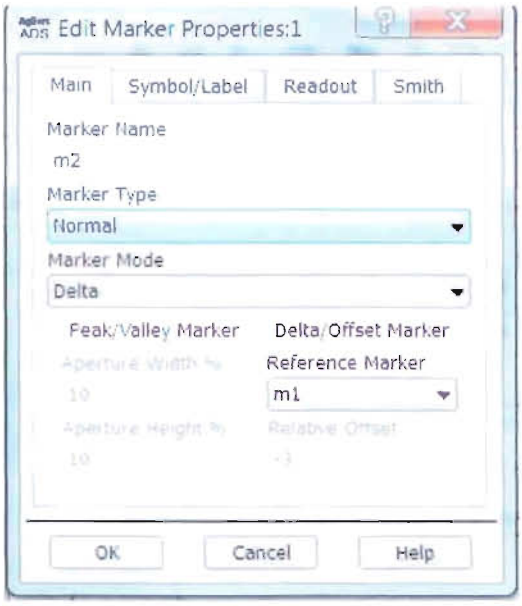

Figure A-16: Marker properties window

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