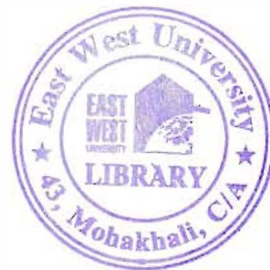
DEGRADATION OF EFFECTIVE DECOUPLING CAPACITANCE IN HIGH SPEED CMOS CIRCUITS



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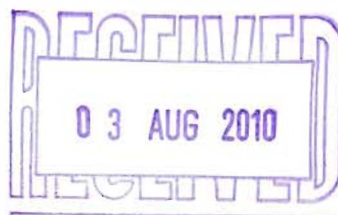

Abstract

ıe to increasing demand on power by silicon operating at higher frequencies, voltage droops in wer buses at switching transients can be a critical constraint. On-die decoupling is used to luce the droops and achieve higher performance. In this thesis we perform an analysis of high quency decoupling capacitor design using low loss tangent high-k material as dielectric. These pacitors can be used effectively at higher frequencies and can able to compensate the voltage oop to ensure the constant power delivery. We also consider the performance degradation of e decoupling capacitor at high frequency. It is noted that dielectric material effective pacitance reduces above several GHz due to the degradation of the dielectric constant. Below ese frequencies it is demonstrated that decoupling capacitors have better performance at high-quency if the high-k material has lower loss tangent. For this reason we choose lower loss ngent high-k material to design the decoupling capacitor and placed them closer to CMOS rcuits. Our analysis is done on the basis of simulation result done using the ADS software hich is briefly discussed inside this paper.

Acknowledgements

We are so much thankful to our supervisor Dr. Md. Ishfaqur Raza because without his special care and helpful hand we couldn't complete the project successfully. He tried so hard and gives us much more time to know the depth of knowledge which is related with our project. He motivated and guided us successfully to understand that what we are going to do and what are the factor we need to know to complete it. So again we want to give him thanks from our heart and pray to "ALLAH" to keep him safe & happy.

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1. INTRODUCTION

1.1. Motivation:

In semiconductor circuit one of the most unfortunate features is parasitic component which causes voltage droop. To solve this voltage droop problem we can use a decoupling capacitor, familiarly known as "decaps", in shunt with the driving load and which can provide the required voltage to the driving load. But decoupling capacitors properly work only within a certain frequency bandwidth. If the frequency content of the signal increases the effective capacitance of the decoupling capacitor decreases, particularly at very high frequency. This will eventually reduce the effectiveness of the decoupling capacitor and the capacitor behaves like a short circuit for which at high frequency the circuit voltage droop can not then be compensated. But if we change the dielectric material then we have an opportunity to increase the frequency response of the capacitor. So our proposal is to look at different materials including High-K.

Basically high-k material can increase the sustainability of capacitor in high frequency due to its higher dielectric constant and lower loss tangent. Loss tangent is a dielectric material parameter which quantifies its inherent dissipation of electromagnetic energy. Actually it refers to an angle in a complex plane between the resistive (lossy) component of an electromagnetic field and its reactive (lossless) component. If the loss tangent of a dielectric material decreases then its frequency increases by the below relationship,

$$f = \sigma/2\pi\epsilon' tan\delta$$

The dielectric constant [1] refers how effective a dielectric is allowing a capacitor to store more charge depends on the dielectric material from which it made off. Every material has a dielectric constant k and it is the ratio of the field without the dielectric (E_0) to the net field (E) with the dielectric, $k = E_0 / E$. Benefit of the larger the dielectric constant is that it can store more charges. So, if we build capacitor with large dielectric constant and less loss tangent then we can build such a capacitor which is smaller in size but can operate in a comparatively high frequency and the performance of the capacitor is far better than any other normal material made capacitor.

We have discussed above that for better performance of the capacitor we need high-K material but it has a big impact on the size of the capacitor. Basically, Silicon dioxide has been used as a gate oxide

material for decades. As transistors have decreased in size, the thickness of the silicon dioxide gate dielectric has gradually decreased to increase the gate capacitance and thereby drive current and device performance. As the thickness scales below 2 nm, leakage currents occur due to electron tunneling increase significantly, leading to unwieldy power consumption and reduced device reliability. Replacing the silicon dioxide gate dielectric with a high -K material allows increased gate capacitance without the concomitant leakage effects and with an acceptable small size.

For the above consideration our motivation is to build a capacitor with high-K material such as hafnium dioxide (HFO_2), Yttrium Oxide(Y_2O_3) and Lanthanum Oxide (La_2O_3) which can store a large amount of charge and can sustain in a comparatively high frequency with small size and also observe the capacitance of these three materials with respect to frequency.

1.2. Literary Survey:

1.2.1. Decoupling Capacitor:

Decoupling capacitor is one kind of capacitor which is used to provide charge support to switching circuits. Electrical circuit noise caused by a circuit element can affect other circuit elements by modifying the voltage rail levels. To deduce this problem a capacitor is shunted after that noise creating element which eventually reduce the effect they have on the rest of the circuit. Bypass capacitor is the alternative name of a decoupling capacitor; as it is used to bypass the power supply or other high impedance component of a circuit.

In "High Capacitance, Large Area, Thin Film, Nanocomposite Based Embedded Capacitor[1]" paper, they represented thin film technology based on barium titanate ($BaTiO_3$)-epoxy polymer nanocomposites to develop and manufacture high performance embedded capacitors and can be used for decoupling purpose. The referred technology was able to produce high capacitance density (10 to 100 nF/inch2), large area, and thin film capacitors with controlled thickness from about 2 micron to about 25 microns for a series of BaTiO3 epoxy nanocomposites.

In "Layout of Decoupling Capacitors in IP Blocks for 90-nm CMOS [2]" paper, they introduced a design metric to determine the optimal number of fingers to use in the standard cell layout to obtain a desired capacitance level over a target operating frequency and investigated the tradeoffs between

high-frequency performance of decaps and electrostatic discharge (ESD) protection and its impact on the layout of standard cell decaps.

In "Efficient Placement of Distributed On-Chip Decoupling Capacitors in Nanoscale ICs [3]" paper they proposed a system of distributed on-chip decoupling capacitors where on-chip decoupling capacitor is providing the required on-chip decoupling capacitance under existing technology constraints. In this system of distribution a capacitor is placed closest to the current load to provide the required charge and as the first capacitor is depleted, the next decoupling capacitor is activated to provide a large portion of the total current drawn by the load.

1.2.2. White Space or White Area Decoupling:

White space refers to the unused blank space in a semiconductor device. Now a day's semiconductor chips are very small in size so we need to manage our redundant space effectively. As we use a decoupling capacitor in the semiconductor device to compensate the voltage droop so, that decoupling capacitor can be placed in that white space or white area region.

In "Quantifying Decoupling Capacitor Location [4]" paper, they discuss about the position of the decoupling capacitor. Coupling between an IC and a decoupling capacitor is a function of the spacing between the IC and capacitor, and spacing between power and ground layers. They studied the impact of the mutual inductance on decoupling, i.e., local versus global decoupling by using a circuit extraction approach based on a mixed-potential integral equation where local decoupling (white area decoupling near the required load) has benefits over global decoupling for certain ranges of IC/capacitor spacing and power layer thickness.

1.2.3. Voltage Droops:

Voltage droop defines the unintentional drop in voltage level due to current drawn by switching circuits. It occurs due to the path inductance and resistance. Although small amounts of voltage drop are unavoidable, there are times when voltage droop is excessive and can cause unexpected and unwanted behavior in a circuit. To prevent voltage droop, decoupling capacitors should be used as compensator to compensate the current needed to drive the load.

In "Test Pattern Generation for Power Supply Droop Faults [5]" paper, they represented about a new modeling of droop faults (basically timing fault) to explain the timing behavior in a faulty circuit

induced by power supply voltage drop in nano-scale VLSI chips. In new modeling a simple ATPG (Automatic Test Pattern Generation) based procedure for stuck-at faults has been adapted to test droop faults where for validation of the methodology in combinational circuits, a set of appropriate clusters of gates is selected to cover potential droop-prone regions in a circuit.

In "Decoupling Capacitors for Multi-Voltage Power Distribution Systems [6]" paper they investigated the dependence of the impedance and magnitude of the voltage transfer function on the parameters of the power distribution system and explained an anti-resonance phenomenon. They showed that the magnitude of the voltage transfer function is strongly dependent on the parasitic inductance of the decoupling capacitors. So they design a technique to cancel and shift anti-resonant spikes out of range of the operating frequencies for which the decoupling capacitor can perform its required operation properly.

1.2.4. Dielectric Constant & Loss Tangent:

The loss tangent is a parameter of a dielectric material that refers the inherent dissipation of electromagnetic energy. Basically this term defines an angle in a complex plane between the resistive (lossy) component and reactive (lossless) component of an electromagnetic field.

The dielectric constant is the ratio of the permittivity of a substance (material) to the permittivity of free space. So, dielectric constant, $\varepsilon=\varepsilon_0/\varepsilon_r$ where ε_0 represents the field without the dielectric and ε_r represents the field with the dielectric.

In "Dielectric Constant and Loss Tangent Characterization of Thin High-K Dielectrics Using Corner-to-Corner Plane Probing [7]" paper, they presented a new methodology for the extraction of frequency-dependent dielectric constant and loss tangent parameters which is based on a 2-port measurement of a rectangular power ground plane pair by probing from corner to corner and curve fitting to simulation results.

1.2.5. High K Materials:

High-k materials are material which has a higher dielectric constant (ε_r or K). High-k materials are used in semiconductor manufacturing processes which replace the silicon dioxide gate dielectric.

The implementation of high-k gate dielectrics has developed several strategies to allow further miniaturization of microelectronic components, colloquially referred to as extending Moore's Law.

In "Recent Advances in High-*k* Nanocomposite Materials for Embedded Capacitor Applications [8]" paper, they discuss about the high dielectric constant (*k*) composite materials which have been developed and evaluated for embedded and decoupling capacitor application where they try to achieve high dielectric performance including high-*k* and low dielectric loss for polymer composites. In this paper the referred high-*k* materials which meet the requirements for this application should possess high dielectric constant, low dissipation factor, high thermal stability, simple process ability and good dielectric properties over broad frequency range.

1.3. Proposal of Decoupling Capacitor:

In this paper we propose a decoupling capacitor model to compensate the voltage droop of the affected power delivery system of the semiconductor device and investigate the performance degradation of the decoupling capacitor at high frequency for the different high-k materials.

For capacitor we use high-k materials due to scale down effects of SiO_2 gate oxide, while maintaining lower power consumption and increased performance of the decoupling capacitor at high frequencies. If we scale down the gate oxide then electron tunneling occurred in VLSI circuits but if we use the high-k materials which has the higher dielectric constant then can reduce electron tunneling by virtue of using a thicker dielectric. Although a material has higher dielectric constant but if the material has higher loss tangent then the capacitor made of that material becomes a lossy capacitor, thus performance degradation of high frequency. But fortunately almost all the high-k material has lower loss tangent compare to Silicon for which they can sustain acceptable performance at high frequency. For the above stated reason we chose three different high-k materials to design the stack capacitor to show the performance degradation at high frequency.

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2. POWER DELIVERY IN HIGH FREQUENCY CIRCUIT

According to Moore's Law, the number of transistor is increasing exponentially. The increasing number of transistors over the past several decades in microprocessor is shown in Fig. 1.

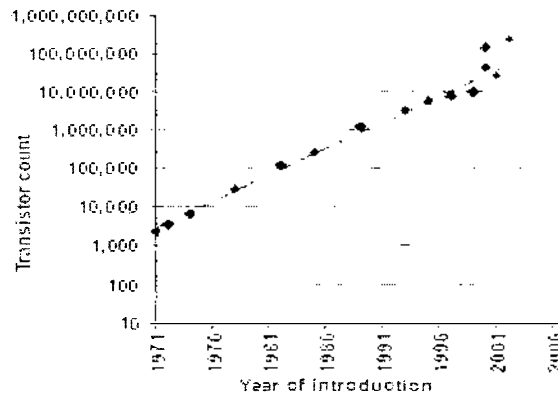

Figure 1: Transistor count doubles every 18-24 months.

It is also known that these transistors need to switch faster to improve its performance because the more the transistors switch fast then we can get better performance from the microprocessor chip. As transistor are getting smaller and faster, over the last two decades the current levels of the microprocessor has also been increasing dramatically. This high current was delivered from the power supply on the system motherboard to the chip through the package. To handle this high current, the package must provide a low resistance path in the order of <1mOhm. In Fig. 2 we noticed that at present the typical supply current is in 10-30 A range, also a range that is expected to increase for future microprocessor [9].

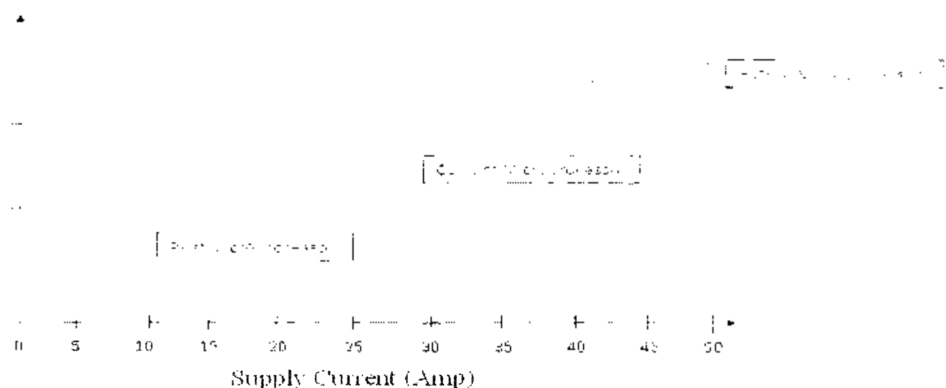

Figure 2 : Increase in supply current for Microprocessor in future.

: increase in current consumption by the microprocessor is also demanding that the reduction of voltage level of the microprocessor. International Technology Roadmap for Semiconductor RS) published 'Roadmap Information' about future technology requirements for semiconductor :ry year. If we look over **ITRS 2009 Edition** then we see the projected reduction in voltage level er the next couple of years, Table 1.

Table 1: Change of voltage level for future technology predict by ITRS

Year	2009	2010	2011	2012	2013	2014	2015
Volts (V)	1	0.97	0.93	0.9	0.87	0.84	0.81

ıe reduction of power supply voltage is also decreasing noise margin. The paper published by Y.- . Jiang, K.-T. Cheng, "Analysis of Performance Impact Caused by Power Supply Noise in Deep ıbmicron Devices." in 1999 shows that around 10-15% voltage drop may cause 20-30% increase in ıte propagation delay. So for most of the 90 nm static CM●S gates a change of 1% in power ıpply voltage may occur to nearly 4% change in delay. The delay of a logic gate increases when ıere is a supply voltage drop across the gate.[10]

this situation we can say that as CM●S technology scales day by day so the power supply has ecome a big issue because of increasing clock frequency and decreasing supply voltage. As a result :en several transistors switch simultaneously then a significant power supply drop will be happen. .s power supply drop is happening because there are parallel load across the power grid. This ·enomenon is known as voltage droop.

modern high speed system resistive IR and inductive L(di/dt) voltage drops are the main ırce of voltage droops. The IR droop has been increasing due to increased resistance in the power : because of reduced widths of the metal as technology becomes more advanced. Also in CM●S .:nology the demand of high current is increasing that's why the effect of L (di/dt) is increased .· by day. [11] So when devices are switching with respect to the clock edge, then it will draw :ent to charge or discharge CMOS gate capacitances. As a result at the edge of clock the voltage ɔs at the parasitic elements is observed which is reduces the power rail voltage, or V_{cc}/V_{dd}. This ..ıction in supply voltage due to switching is known as power supply noise. The increase in :er supply noise reduces the signal noise margin, increases signal delay, delay uncertainty and .k jitter.

So we need to implement and consider power distribution in a digital system which is given below.

- One of the most effective ways to reduce the power supply noise is to use decoupling capacitor on the card, board, module and chip. Here decoupling capacitors worked as a charge storage device so that it can oppose the voltage droops at the edge of clocks at different stages of the network. However, these capacitors are controlled by their location with respect to the CMOS devices and their inherent parasitic components (such as equivalent series resistance and inductance, i.e. ESR and ESL). The placing of the decoupling capacitor in a power delivery system is shown in Fig. 3 & 4.

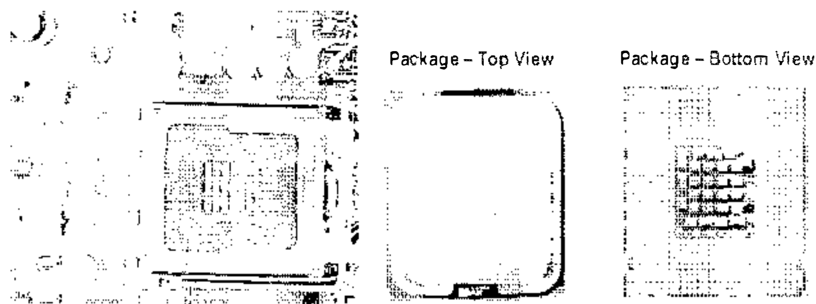

Figure 3: Power delivery solution for the Pentium 4 processor.

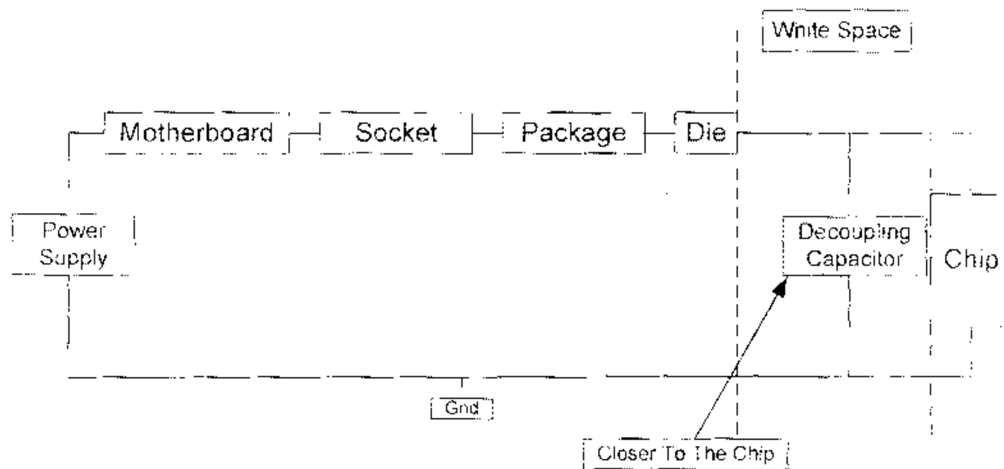

Figure 4: Equivalent model of power delivery system in microprocessor.

...re power is delivered to the chip after passing through the motherboard, socket and package. ...ing this power delivery, there will be loss (L, R loss). Decoupling capacitor are used as local ...rge reservoir. So decoupling capacitor is placed closer to the chip so that it can provide extra

current to charge the load capacitor in addition to the power supply. Also it will reduce power supply noise because the inductive effect in the loop current path is decreased. As the inductance scales slowly, the placement of decoupling capacitor is very important because it affect the performance of power supply network as well as the chip performance.

The performance of decoupling capacitor depends on the distance between the current load and the decoupling capacitance. Decoupling capacitor should be placed close to a current load during discharge and once the switching event is completed then decoupling capacitance should be charged before the next clock cycle starts.[12]

Decoupling capacitors are generally placed in white space available on the die. To get effective performance physically decoupling capacitor should be placed closer to the chip so that it can reduce the parasitic voltage droop at the switching transition.

- The second step is to remove excessive IR drops - which we do by reducing the wire size. However dynamic voltage fluctuations may still occur even if the wire sizing is performed.

- We also need to place low inductance capacitances under packages and on packages. For this reason now capacitances have been designed within the silicon die and placing them in critical space which is known as white space. Because the more the capacitor placed near to the chip the more inductance loss will be reduced.

However, as guided by Moore's law, the power demand of the CMOS devices are ever increasing with faster clocks, smaller devices, and integration of analog and digital circuits within the same die. So these issues are more critical to make the management of voltage droops that's why the conventional techniques of controlling voltage droops are failing beyond a certain bandwidth.[2]

3. NOVEL METHOD OF REDUCING POWER DROOP

3.1. Improved VLSI Circuit Performance Using Localized Power decoupling:

In "Improved VLSI Circuit Performance Using Localized Power decoupling [13]" paper. they proposed an advance technology for DRAM capacitor by using the decoupling strategy. In the paper they proposed a technique, in which the decoupling is provided at the CMOS level, right where the power is needed. This technology is needed for VLSI circuits due to increases the performance of the system, because power droop in silicon is a major problem in the semiconductor circuits. When semiconductor circuit operates in high frequency and as the power levels are reduced then the semiconductor devices are limiting the timing and voltage budget which is design in circuits to account for noise and also include voltage drooping due to inductive losses. Novel techniques are involved to compensate these losses at all levels including motherboard, package through out in silicon: but due to lack of available space and design constrain decoupling at die level is very limited. For all this, to solve the above mentioned problem this paper is come forward with an advance technology where they mention about a methodology to introduce decoupling right at the transistor. The crux of the concept is to use DRAM capacitors, as a local capacitance bank to deliver power to the devices right when the switching takes places.

In this paper they are concentrated only in dynamic power which is a function of clock frequency or more accurately is a function of the switching of the CMOS circuit transistor. Basically dynamic power relates to bow many times the circuit switches in a second and the switching of a circuit is a function of the RC time constant where the RC time constant depends on the source and drain capacitance at the driver end and the gate capacitance of the receiving end. But for the newer process s the source and drain of a transistor is in smaller dimension for which the capacitance reduces and eventually also the resistance reduces which means it also reduces the RC time constant. As the RC time constant reduces the switching speed of the circuit increases which is the ultimate goal. But the reduced RC time constant causes the switching current to race quicker and resulting in a large di/dt for which the faster switching speed translate into higher harmonics in the signals. In time domain

large di/dt cause the large voltage droop across any inductance as $V_L=L*di/dt$. For larger di/dt the inductive voltage drop increases which reduces the power supply to the IC. To reduce the voltage droop and increases the power supply they find an alternative source for the fast switching current where they used localized decoupling concept in the circuit. Through localized decoupling process they place a decoupling capacitor before the driving load where the decoupling capacitor operates either in charging mode or in discharging mode. To build the decoupling capacitor they incorporate the DRAM capacitor technology where the technology matures in the form of one transistor one capacitor configuration. The capacitors can be either in the stacked or trench configuration.

In this paper they bring a new ideology by bringing together two parallel semiconductor technologies. The capacitor technology follows the DRAM ideology and whiles the system level decoupling and die white space decoupling is not sufficient enough to support nano-dimensions transistor circuit with 10s picoseconds transition rates for which the trench and stacked capacitor model can be successfully designed right next to transistors without taking more space then the isolation transistor.

3.2. Low-Cost Deep Trench Decoupling for Low-Power CMOS:

In "A Novel, Low-Cost Deep Trench Decoupling Capacitor for High-Performance, Low-Power Bulk CMOS Application [14]" paper; they represent an overview & electrical results for a novel deep trench decoupling capacitor, which is borrowed from the regular embedded DRAM trench process, but with significant process simplification by using decoupling, to provide reduction of cost and process cycle time. By using this phenomenon; capacitor can provide significant chip-level area savings, using only 1/8 silicon real estate to fabricate the same capacitance as standard planar gate oxide capacitors and also the "decap" demonstrates a improvement in leakage compared to standard planar gate oxide capacitors. By using deep trench capacitor 10^5 improvements in leakage can be realized than in conventional planer decap designs.

Inductance is one of the unfortunate features in semiconductor circuit which produce noise on the power delivery and have a detrimental impact on circuit performance. Decoupling capacitor (decaps) reduce the induce noise and provide the low impedance path to ground. For higher clock speed device more effective decoupling is needed. Decaps are planer oxide device where the Nwell is one

ite and gate is another. In decaps gate dielectric limits the amount of the charge which can obtains om planer decaps and are often found to contribute to standby leakage. In high speed circuit signs decap can account more than 10% of the total chip area. To solve the above stated problem this paper they introduced a novel decap design which utilized IBM's unique eDRAM technology d called as "DZ decaps" where the DZ decaps have a extremely high capacitance/area, very low akage/fF, and series resistances competitive with planar gate oxide decaps. In this paper they ention the fabrication process of Dz trench capacitor and its fabrication advantages. Basically Dz ench capacitor are fabricated in a similar manner to bulk eDRAM Deep Trench (DT) capacitor here the DZ capacitors share exactly the same pad films, oxide head mask used for trench efinition, lithography process, buried plate process and node dielectric formation process. After the ode dielectric process DZ capacitor module is much simpler than DT capacitor because there is no eed of resist recess and collar oxide formation for DZ capacitor and the full vertical trench surface an be used as decaps. In DZ decaps the number of polyfills and poly recess are reduced and because f this DZ decaps saves approximately 35% in process cost.

n the comparison of Dz capacitor and typical planar gate-oxide capacitor, the DZ decaps is much etter than the typical planar gate-oxide capacitor because DZ decaps need 1/8 chip area to provide he same capacitance and the leakage is 5 order less than the typical planar gate-oxide capacitor neans DZ decaps can offer more than 8X more capacitance/unit area and 10^5 reduction in leakage.

3.3. A Decoupling Platform for Substrates, Sockets, and Interposers:

"A Novel Decoupling Capacitance Platform for Substrates, Sockets and Interposers [15]" paper. ey represent a technology deployed within substrates, interposers or sockets to enhance core power livery because power integrity has become a leading focus due to increasing demands of power ivery networks in current and next generation computer system. This technology developed a vel integration of decoupling capacitance between the core power nets and the ground .Then places the numerous decoupling capacitors sub-optimally placed on traditional printed circuit ard (PCBs). This decoupling capacitor can lower the power supply noise and increased core power bility, permitting greater semiconductor switching frequency while reducing overall system cost. actual system application, this technology proves it's superiority in both cost and performance to wide range of expensive and largely ineffective decoupling strategies.

In semiconductor circuits the current quest for data transmission at 10 Gbps and is hindered by instability in core voltage of supplying semiconductor beyond 10 Gbps and this problem will be more pronounced with shrinking lithography, increased switching speeds and greater power requirements. Core voltage "design for stability" has been a compartmentalized endeavor due to inadequate communication among the chip, package and board designers and also lack of system co-design combine to result in suboptimal performance, including bit-error rate, device malfunction, increased noise coupling and lower semiconductor yield. In semiconductor chips system designer restored to exotic "fixes" but unfortunately these "fixes" are inadequate because they are an after though rather than a fore though, to the system architecture design.

In today's system maintain stable core voltage and suppressing switching noise on power supply are two intimately related problems and can be solved by reducing the impedance seen by the power delivery system by providing effectively decoupling capacitance. The traditional approach to core decoupling has been to endow the PCB, substrate and die with more decoupling capacitance. If in a system hundreds or thousands of discrete decoupling capacitors are present then in practical level they are extremely wasteful these capacitors are not place near to the required part (which needs the voltage to operate properly). Due to the increase bus length and remote voltage regulator module location which introduces loss and inductance the system suffers unnecessarily. To compensate this problem they add High-capacitance interdigitated capacitors (IDCs) directly to the substrate or in PCB. This phenomenon increases the cost but for better performance the additional coat can be neglected. Incentives for a more novel, root-level solution drove the development of this new decoupling platform that integrates discrete or custom capacitance into the voltage core much closer to the die. The first feasible implementation of this solution (named as CapCor) is within a socket and provides substrate solder-attach on top and PCB solder-attach on the bottom. Viewed from a system-wide perspective, if a decoupling capacitor is added under the substrate then it is more effective than on the PCB which render hundreds of PCB decoupling capacitors redundant and reduce the total system cost. As hundreds of PCB decoupling capacitors eliminate means their supporting pads, vias and traces also eliminates which basically reduce the resistance and inductance and improve the electrical signal performance. In this new and novel configuration decoupling capacitance is integrated inside the interposer between power and ground pins where the design involves direct solder of discrete caps to the power and ground pins. In microprocessor high switching speed requires highly stable power. In this new process as the decoupling capacitor is

place near to the substrate, so it has lower parasitic component means lower power droop means highly stable power.

In this paper they presented a novel decoupling technology demonstrated to improve power delivery, suppress transient noise on the power system and stabilized the core voltage and also showed that CapCore is a superior alternative to hundreds of PCB decoupling capacitors, at the same time delivering lower power impedance which substantially reduce both the PCB complexity and total cost.

4. HIGH-K DIELECTRIC CONSTANT

High-*K* materials are dielectric material with high permittivity constant (ε_r or K). Recently high-*K* material have received wide acceptability for various applications including gate dielectrics, high charge-storage capacitor and electro active materials [16][17][18]. The implementation of high-k gate dielectrics has allowed further miniaturization of microelectronic components, often referred to as extending Moore's Law. High-*K* materials with high dielectric constant and low dielectric loss are imperative for real applications of embedded passives, specifically capacitor to provide the size reduction and performance enhancement of many microelectronic systems [19][20].

4.1. Why Need High-K?

To allow the advancement of semiconductor performance in integrated circuits. it appears likely that dielectrics other than SiO_2 will be required. The problem is that an optimal replacement gate dielectric for SiO_2 has to be found which can be used in applications requiring thickness of 10"A in a layer. At this thickness, quantum mechanical electron tunneling is prevalent, and leakage currents cannot be maintained below the proposed maximum limit of 1 A/cm^2 (for high performance processors) [21][22][23] .To maintain the correct transistor operation, a specific level of capacitance density is required in this small gate capacitor. This limitation appears to be of theoretical origin (i.e., unable to be relieved by continued process improvement), thus the solution demands the introduction of a new higher permittivity gate dielectric composition, or possibly a transistor offering an alternative architecture. For the improved transistor operations may only be achieved in the presence of metallic gate electrodes (highly doped poly-Si is currently in use) which will not become depleted under bias [24]. Moreover, new and improved methods and instrumentation must be developed for accurate device and process characterization. With these reduced dimensions, and the influence of the size of contaminant particles, leads to device failure. In these failures, the contaminant size fall below diameters that can be detected optically, a method currently used for contaminant particle detection [25].

In our project we develop a decoupling capacitor using High-*K* material. We show in this paper by using high permittivity and low loss tangent high-*K* material we get much better decoupling capacitance for better performance in power analysis grid. Ideally, the larger dielectric constant (*K*)

ill allow the thickness to be increased such that a tolerable level of tunneling leakage can be aintained. Though replacing SiO_2 with any dielectric having K>4 would be theoretically itisfactory, the possibility of higher leakage must be considered. So to avoid this problem we onsider high permittivity of high-*K* material.

4.2. High-K Dielectrics:

rom a dielectric property point of view, dielectric constant and dielectric loss are the two most nportant parameters that dictate the performance of a candidate material for embedded capacitors. hin dielectrics with a high dielectric constant are very attractive for improving the decoupling erformance. To accurately estimate the performance of thin high-*K* dielectrics, the frequency lependent dielectric constant and the loss tangent have to be extracted [7].

n the beginning, ferroelectric ceramic materials with permanent dipole moment which gives these naterials high-*K* in the thousands, including BaTiO3 (barium titanate), BaSrTiO3 (barium strontium itanate), PbZrTiO3 (lead zirconate titanate) etc., have been used as dielectric materials for lecoupling capacitors [30][31]. In our research we need low loss tangent and high permittivity of nigh-*K* material. So at level we select following material, Table 2 give an overview of the most ommonly applied high-k dielectrics

Table 2: Key parameters of high-k dielectrics evaluated

material	structure	permittivity	loss tangent	Reference
HfO_2	amorphous MIM	25	0.006	[26]
ZrO_2	amorphous MIM	22	0.005	[27]
La_2O_3	amorphous MIM	20	0.016	[28]
Y_2O_3	amorphous MIM	12	0.003	[29]

As hafnium oxide (HfO2) or zirconium oxide (ZrO2) presents several good characteristics: *K*-value om 15 to 35 at DC and high thermal stability in direct contact with silicon and good process mpatibility. HfO2 and ZrO2 are promising alternatives for both MIM and MOS structures [32]. nthanum oxides (La_2O_3) have high permittivity, good resistance to devitrification, and an ppreciably large band gap. The calculated permittivity of La_2O_3 (hexagonal) is approximately 38, ile the measured values range between 20 and 30.

5. SIMULATION & ANALYSIS

5.1. Main Circuit:

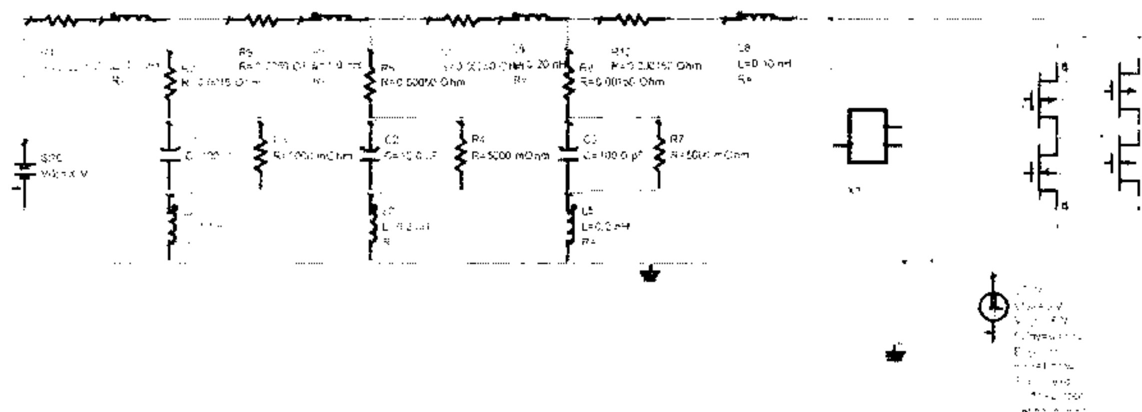

Figure 5: simple model of Power Delivery Analysis circuit.

1 Fig. 5. the equivalent model of a power delivery circuit has been designed. A typical power elivery circuit has a DC supply voltage which is supplied by a voltage regulator located on a. rinted circuit board plane. In this circuit the load is a multitude of inverters. The power path is ıodeled with inductances and resistors. We have also added decoupling capacitors. Decoupling apacitors will be used to reduce the effect of parasitic inductance in power delivery networks. Decoupling capacitors are widely used to manage power supply noise [33]. The capacitor solution vill be modeled at different stages of this circuits i.e at the motherbord,on the packgae and in the lie. Decoupling capacitors are an effective way to reduce the impedance of power delivery systems perating at high frequencies [34].Generally in low frequency inductance become short and by this me capacitance become charged. In the high frequency inductance operates and voltage droop cross L is increased. The total sum value of L increase which affects circuit performance. So we sert a decoupling capacitor immediately after the inductance to reduce the inductive effect on ower. The decoupling capacitor provides the storage charge to compensate for voltage drop due to ductance. Each capacitance is modeled with the parasitic resistance(ESR) and inductance(ESL) hich is series with the capacitance.

Ve use the following value for the equivalent parameter in the microprocessor chip power delivery stem which is given in Table 3.

Table 3: The value we used for the equivalent parameter in main circuit

Equivalent Parameter	Mother Board	Socket	Package	Die
Resistance (R)	0.0015ohm	0.0050ohm	0.00050ohm	0.000150ohm
Inductance (L)	1.0nH	1.0nH	0.20nH	0.10nH

/e also use decoupling capacitor in the power delivery system where the value we use for the quivalent capacitor model is given in Table 4.

Table 4: The value we used for the equivalent capacitor parameter

Equivalent Capacitor Parameter	Mother Board	Socket	Package	Die
Equivalent Series Resistance (ESR)	0.0015Ohm	0.0005Ohm	0.0015Ohm	ESR1**
Capacitor (C)	100uF	10uF	100pF	0.1792pF
Parallel Resistance (R_p)	5000mOhm	5000mOhm	5000mOhm	R_p1**
Equivalent Series Inductance (ESL)	0.1nH	0.2nH	0.2nH	ESL1**

**ESR1,ESL1,R_p1 small and incignificant effect.

5.2. ESL & ESR:

There are various design issues which affect the power distribution impedance. It has already been demonstrated that the power distribution impedance for a modern computer must be kept low and flat over a large frequency range [35]for improved product performance. Power distribution system noise affects computer product timing performance. In high frequency reducing power distribution noise is with decoupling capacitors.

Capacitor ESR determines the number of capacitors required to achieve certain target impedance at a particular frequency and is therefore an important design parameter. ESR of a capacitor of paramount importance is within power supply design for both switching and linear power supplies. The equivalent series resistance, ESR shown in Fig. 6 plays a major part in the performance of the circuit as a whole.

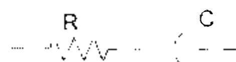

Figure 6 : The Equivalent Series Resistance, ESR associated with a capacitor

apacitors with high values of ESR will naturally need to dissipate power as heat. It is found that hen the temperature of a capacitor rises, then generally the ESR increases, although in a non-linear shion. Increasing frequency also has a similar effect. As the dielectric thickness increases so does e ESR. As the plate area increases, the ESR will go down if the plate thickness remains the same.

SL (Equivalent Series Inductance) shown in Fig. 7 is pretty much caused by the inductance of the ectrodes and leads. The ESL of a capacitor sets the limiting factor of how well (or fast) a capacitor an de-couple noise off a power bus. The ESL of a capacitor also sets the resonate-point of a apacitor. Because the inductance appears in series with the capacitor, they form a tank circuit. The SL is defined by the size of current loop of power circuit. The bigger the current loop the greater ne ESL inductance. By placing the capacitance closer to the CMOS, we can see a significant eduction in inductance.

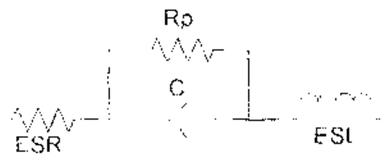

Figure 7 : Capacitor equivalent circuit

5.3. Why & where to place Decoupling Capacitor:

apacitance between power and ground distribution networks, referred to as decoupling capacitors r decaps, acts as local charge storage and is helpful in mitigating the voltage drop at supply points. o manage power supply noise decoupling capacitors are widely used. An effective way to reduce e impedance of power delivery systems operating at high frequencies are decoupling capacitors.

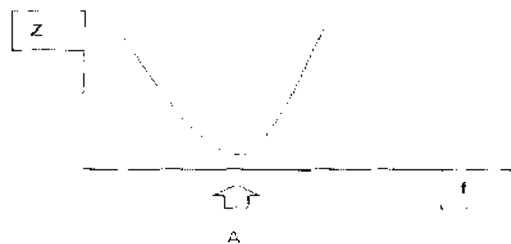

Figure 8: Plot frequency vs. impedance

$$Z = R + j\omega L + \frac{1}{j\omega C} \quad \text{(i)}$$

From Fig. 8 we see that before the point 'A' has low frequencies, where value of inductance is low compare to capacitor. Eventually at a low frequency the value of impedance is high. Generally with the frequency increases capacitance value will decreases at a point 'A' will come where the value of inductance and capacitance cancel out each other, only resistance value remains. After point 'A' as the frequency increases the capacitance decreases but inductance increases which increase the impedance. So total impedance is increase by L and R when power delivery systems run in high frequency and system performance is decreased. To reduce voltage drop of system we want place decoupling capacitance near to the chip because if place it far from the chip the inductance between circuits and decap will increase. For away from the chip, IR loss and $L\frac{di}{dt}$ loss are increased.

5.4. Inductive drop - $L\frac{di}{dt}$ loss:

In a high frequency RC time constant is decrease and switching current is quicker that cause large $L\frac{di}{dt}$ is increased. Therefore, the circuit will have large $L\frac{di}{dt}$ voltage drop across any inductance $V = L\frac{di}{dt}$.

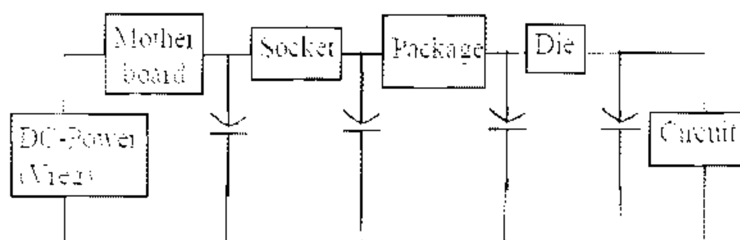

Figure 9 : Power Delivery Analysis circuit

In the power delivery circuit in Fig. 9 we also have resistive drop which is independent of the rate of change (i.e. switching). The total voltage drop in terms of inductance and resistance effect of motherboard, package, socket and silicon [36].

$$V_{dr} = \left(Lm\frac{di}{dt} - Rm\right) - \left(Lp\frac{di}{dt} - Rp\right) - \left(Ls\frac{di}{dt} - Rs\right)$$

Expressing total voltage drop as the sum of inductance and resistance component,

$$V_{dr} = \sum\left(Ln\frac{di}{dt} - IRn\right)$$

So the voltage available in the circuit is

$$V_{eff} = V_{dd} - V_{dr}$$

Modern high performance microprocessors due to their growth in power consumption and switching speeds the $\frac{di}{dt}$ effects are becoming a growing concern. Fast switching current may cause large $\frac{di}{dt}$ and increasing inductive drop which reduces the power rail voltage to drop. The effective power supply (V_{eff}) is shared across the large of component in the silicon through a network of power and ground rails. Here the circuit performance and activities of transistors are affected when voltage droop accelerates. So (V_{dr}) must be minimized to improve circuit performance. We added decoupling capacitors to counteract the $\frac{di}{dt}$ variations in the voltage. It is necessary to model accurately the inductance and capacitance of the package and chip and analyze the grid with such models, as otherwise the amount of decoupling to be added might be underestimated or overestimated. Also it is necessary to maintain the efficiency of the analysis even when including these detailed models.

5.5. Reduce Path Inductance L:

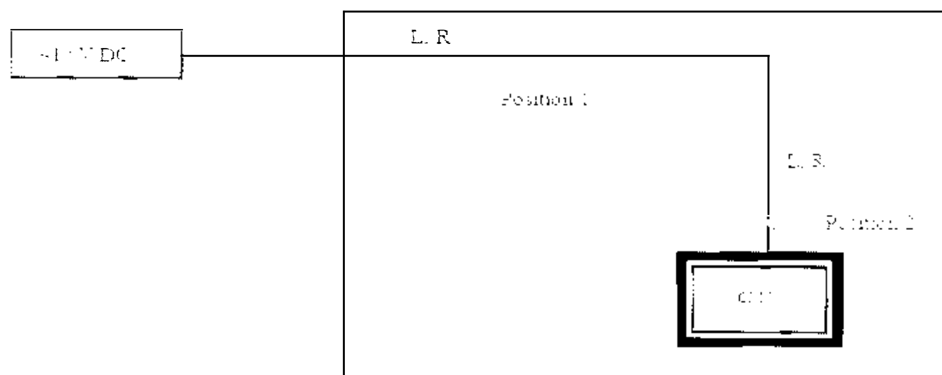

Figure 10 : Placement of decoupling capacitance.

In Fig. 10 is shown a simple model of Chip with a 1.5 DC voltage supply form DC-to-DC regulator. The power transmission buss line shown in Fig.6 has inductance and resistance. If this system runs at high frequency then inductive impedance will increase. Although the resistance is quite small, the inductance voltage drop will be significant. To compensate the impact of inductance in every step of the circuit, we need to add decoupling capacitance appropriately. Let assume we want to place decoupling caps in two white area of the chip. If we place decaps in 'position 1' the value of loop inductance is much higher than the 'position 2'.So to avoid loop inductance we need to place decaps near the chips and minimize IR loss and $L\frac{di}{dt}$ loss.

5.6. White Area:

In a semiconductor device the unused blank space (those areas not occupied by the circuit elements) refers as a white space or white area. In the modern day the size of chip going to very small so, we need to use redundant space effectively. We design decoupling capacitors in the semiconductor device white area to reduce the voltage droop. Traditionally Decoupling capacitors have been allocated into the white space available on the die based on an unsystematic or adhoc approach [37],[38], as shown in Fig. 11. As a result, the power supply voltage drops below the minimum tolerable level for remote blocks, thus affecting circuit performance. The size of an on-chip decoupling capacitor, however, is directly proportional to the area occupied by the capacitor and can require a significant portion of the on-chip area. As described in [39], maximum parasitic impedance between the decoupling capacitor and the current load (or power source) exists at which the decoupling capacitor is effective. Alternatively, to be effective, an on-chip decoupling capacitor should be placed to ensure that both the power supply and the current load are located inside the appropriate effective radius [39].

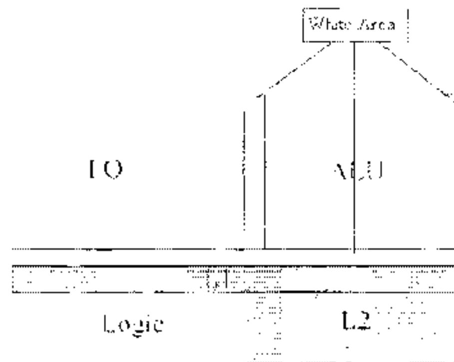

Figure 11 : Placement of on-chip decoupling capacitors using a conventional approach in white area.

5.7. Description on ADS:

In this project our major tools was ADS. We used two part from this tools these are momentum part and schematic part. In the schematic tools we were develop a power delivery analysis circuit and we use momentum tools to design a capacitance.

Momentum is an electromagnetic simulator which is used to evaluate and design modern communications systems products. Momentum can computes S-parameters for general planar

circuits, including micro strip, slot line, strip line, coplanar waveguide, and other topologies. Momentum tools use to simulate multilayer RF/microwave printed circuit boards, hybrids, multichip modules, and integrated circuits. The main things to use momentum tools is it can predict the performance of high-frequency circuit boards, antennas, and ICs. The major benefit of this is that it can simulate when a circuit model range is exceeded or the model does not exist, it can identify parasitic coupling between components, it can analysis and verification to design automation of circuit performance and it can visualize current flow and 3-dimensionaldisplays of far-field radiation. The major features of this tool have to fit frequency sampling for fast, accurate, simulation results. To achieve performance specifications of a design the optimization tools can change geometric dimensions. It also has comprehensive data display tools for viewing results and equation and expression capability for performing calculations on simulated data.

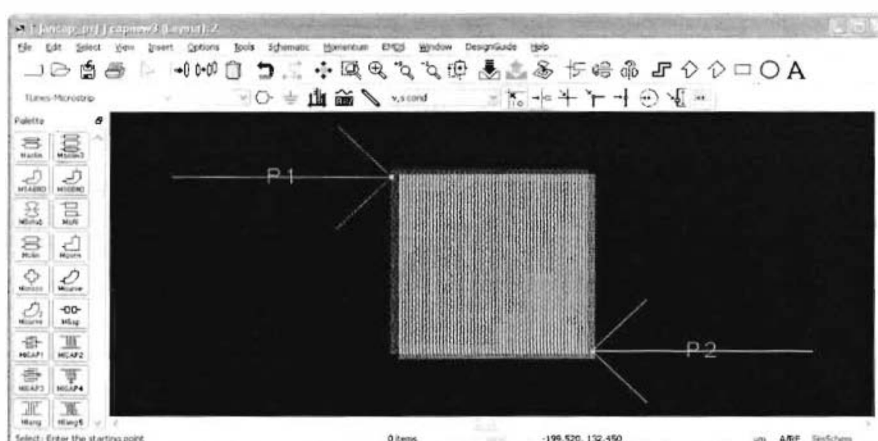

Figure 12: Momentum window of ADS

Fig.12 shows the momentum window of ADS while designing the capacitor. In the momentum we design capacitor for different type of High-K material. After design this capacitance we use **Component** option of momentum then we selected create/update and update design capacitance in the component library. After update component we use this capacitance in schematic window to simulate power delivery circuit. In Fig.13 represent the schematic window of ADS.

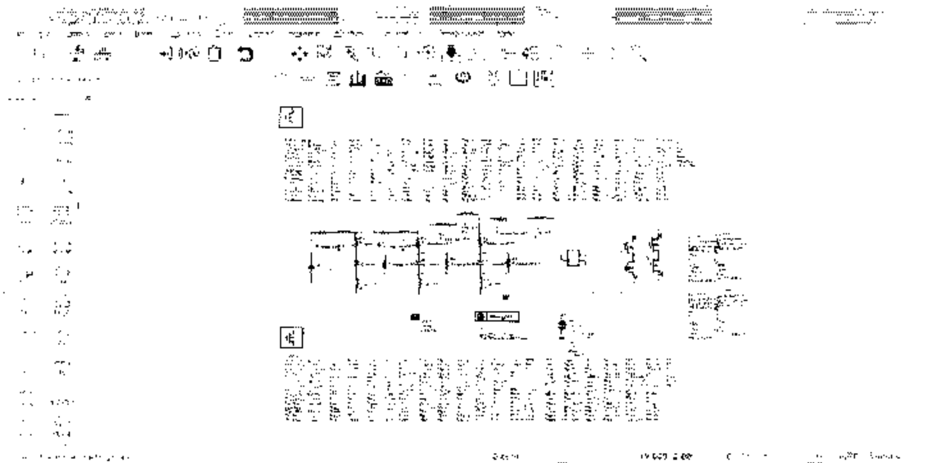

Figure 13 : Schematic window of ADS

We used BSIM4 transistor models both for NMOS and PMOS transistors. Designing capacitor was attached to the source node of two inverters connected back to back, each driving another inverter, to simulate a capacitive load. The model consisted of a motherboard, package, and a socket. Adequate decoupling was placed on the system, at the motherboard and package.

5.8. Result & Calculation:

A simulation analysis has been done to demonstrate the advantage of local decoupling technology. It also assumes that the capacitor will be shared by about 4 back to back CMOS invertors. We design capacitance using the momentum tool from ADS. To design the capacitance the high-k material that we have used are shown in Table 5.

Table 5: High-k materials with dielectric constant and loss tangent.

Material Name	Dielectric constant	Loss tange
Hafnium Oxide (HfO_2)	25	0.006
Lanthanum Oxide (La_2O_3)	20	0.016
Yttrium Oxide(Y_2O_3)	12	0.003

We use 0.179pf capacitance for different analysis. Most important thing is thickness of the capacitance. If the thickness of the decoupling capacitance is very small then it does not affect on the circuit to minimize the droop. Consider these entire things we are assuming that thickness of

HfO_2 0.1μm and calculate other high-k material thickness to make the same capacitance for these materials. Using this thickness in capacitor model then we get minimum droop for HfO_2.

5.8.1. Calculation To Make The Capacitance Same:

For HfO_2, loss tangent=0.006 and permittivity=25.

Area of capacitnace, A= 90μm×90μm = 8100 μm²

$\epsilon_o = 8.85 \times 10^{-18}$ F/ μm

Capacitance of HfO_2, $C = \epsilon_r \epsilon_o \frac{A}{d} = \frac{25 \times 8.85 \times 10^{-18} \times 8100}{0.1} = 0.1792\text{pF}$

Now to make same capacitance we need to find other high-k material thickness. For La_2O_3, loss tangent is 0.016 and ϵ_r =20. So I asume that HfO_2 (ϵ_r=25,thickness=0.1 μm) is okay for minimum droop. To keep the same value of capcitance , thickness of La_2O_3 is $= \frac{0.1 \times 20}{25}$=0.08 μm and

Capacitance is $C = \frac{20 \times 8.85 \times 10^{-18} \times 8100}{0.08}$=0.1792pF

Similarly, For Y_2O_3 ,losstangent=0.003 and ϵ_r =12. So thickness of $Y_2O_3 = \frac{0.1 \times 12}{25}$ =0.048 μm and

Cpacitance is $C = \frac{12 \times 8.85 \times 10^{-18} \times 8100}{0.048}$ = 0.1792pF

In existing material SiO_2 is used to make the capacitance but there are some limitation in this material layer. The main cause is Si material have some limit of its thickness. We cannot make it too much thin. To make same capacitance of SiO_2 the calculated thickness is 0.00156 μm, which is too small for ϵ_r = 3.9. To avoid complex simulation we assumed the thickness of the SiO_2 is 0.01 μm.

5.9. Simulation Result:

In the power delivery circuit shown in Fig. 5, we observe voltage droop before adding capacitance which is shown in Fig.14.

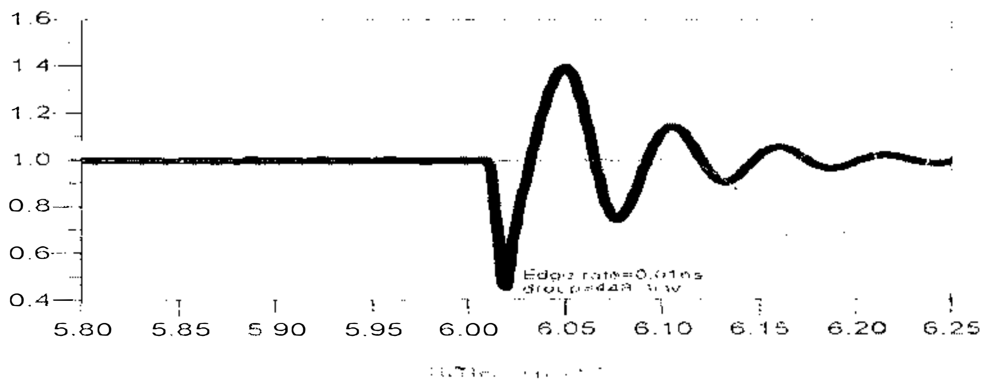

Figure 14 : Without decoupling capacitance voltage droop

om this Fig. we see that for lower edge(0.1ns) rate the voltage droop is 823.4mV and for the gher edge rate(0.01ns) the voltage droop is 448.3mV. So we can say that the voltage droop will crease with the increase of edge rate.

ow we want to show the improvement of the voltage droop after placing our designed capacitor oser to the CMOS circuit. The plot we got in after simulating in ADS is given Fig. 15.

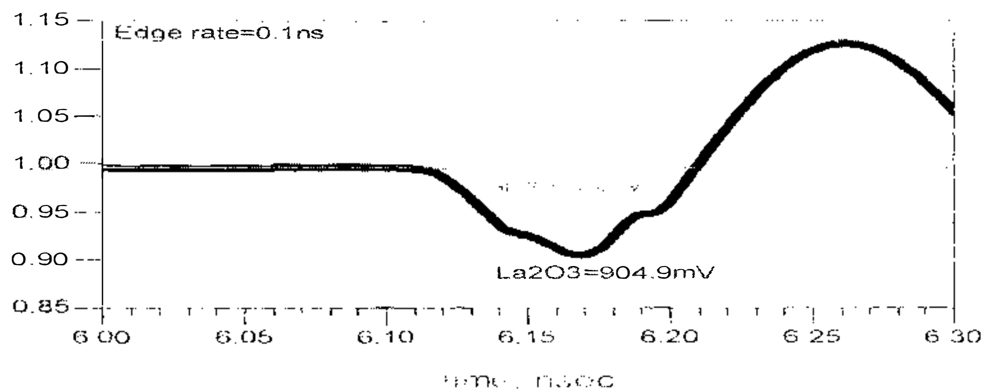

Figure 15: Showing voltage droop for HfO_2 and La_2O_3 at 0.1ns edge rate

ere in Fig.15 shows the voltage droop for HfO_2 and La_2O_3 when rise time =fall time that means lge rate is 0.1ns. From this figure we can say that the voltage droop is significantly changed after acing decoupling capacitor. HfO_2 has loss tangent value= 0.006 and La_2O_3 has loss tangent 0.016 between them HfO_2 has the lower loss tangent than the La_2O_3. The figure shows that the voltage oop for HfO_2 (990.4mV which is closer to 1 in fig.15) is much lower than La_2O_3 (904.9mV). So e can say that high-k material with low loss tangent can improved the voltage droop more gnificantly than higher loss tangent. In conclusion we want to say that loss tangent is a big factor to eate impact on reducing the voltage droop.

Now if we want to determine the voltage droop considering high-k material with respect to the SiO_2 for the 0.1ns edge rate which simulation result is shown in Fig. 16.

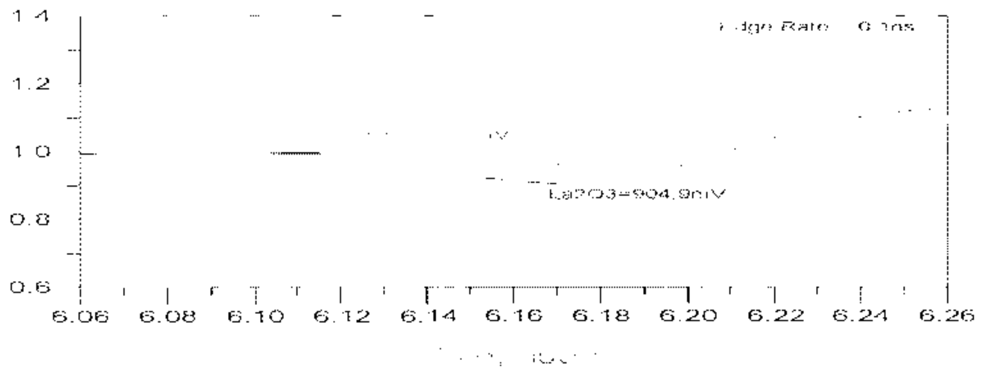

Figure 16: Simulation result which shows voltage droop for SiO_2, HfO_2 and La_2O_3 at 0.1ns edge rate

Here for SiO_2 the simulation result shows the voltage droop= 823.2mV which is much bigger than high-k material. Also without decoupling capacitor we got voltage droop = 823.4mV where after placing SiO_2 material decoupling capacitor voltage droop is 823.2mV so with or without capacitor in a system is the same matter for SiO_2.

Again we did the same simulation but now we changed the edge rate which is 0.01ns that means we increased the frequency. In this situation the changed in voltage we got is shown in Fig. 17.

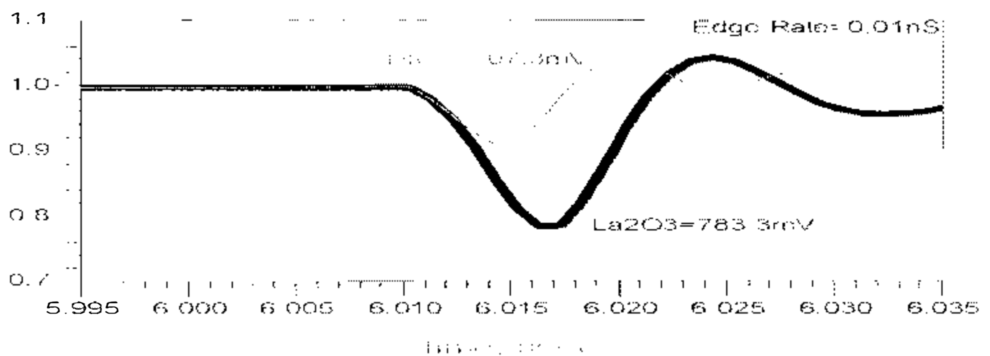

Figure 17: Showing voltage droop for HfO_2 and La_2O_3 at 0.01ns edge rate

From Fig. 17 we can that voltage droop is increased, nevertheless, the low tangent material HfO_2 (voltage droop of 907.3mV) gives better performance than the higher loss tangent material La_2O_3 (783.3mV). In this case with edge of 0.01ns, as shown in Fig. 17, we find that without decoupling capacitor the voltage droop was 448.3mV where after placing our designed capacitor the voltage droop is significantly reduced. Now if we want to see for 0.01ns edge rate what happens with the voltage droop by using capacitors made of SiO_2. The simulation result is shown in Fig. 18.

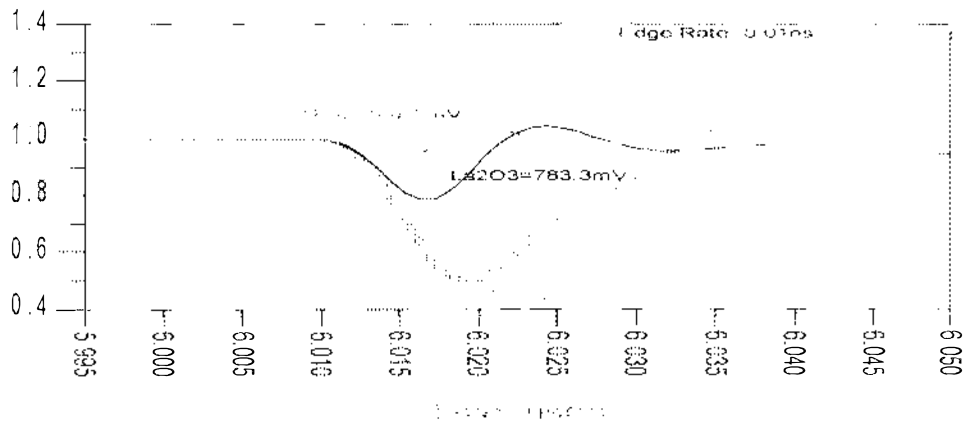

Figure 18: Simulation result which shows voltage droop for SiO_2, HfO_2 and La_2O_3 at 0.01ns edge rate

In this condition again we can say that by using SiO_2 material with or without placing decoupling capacitor is the same thing. Because without capacitor voltage droop was 448.3mV after placing SiO_2 decoupling capacitor it shows voltage droop is 489.9 mV which is not much improved.

During our project period we worked with another high-k material which is Yttrium Oxide (Y_2O_3). It has loss tangent =0.003 which is lower than HfO_2. But the dielectric constant for this material is 12 where HfO_2 has 25. We take the equivalent oxide thickness for HfO_2 is 0.1um to make the same capacitance for both HfO_2 and Y_2O_3, the thickness for Y_2O_3 becomes 0.048um. As a result although it has a lower loss tangent than HfO_2 but the voltage droop for Y_2O_3 is not improved better than the HfO_2. The simulation result is shown in Fig. 19.

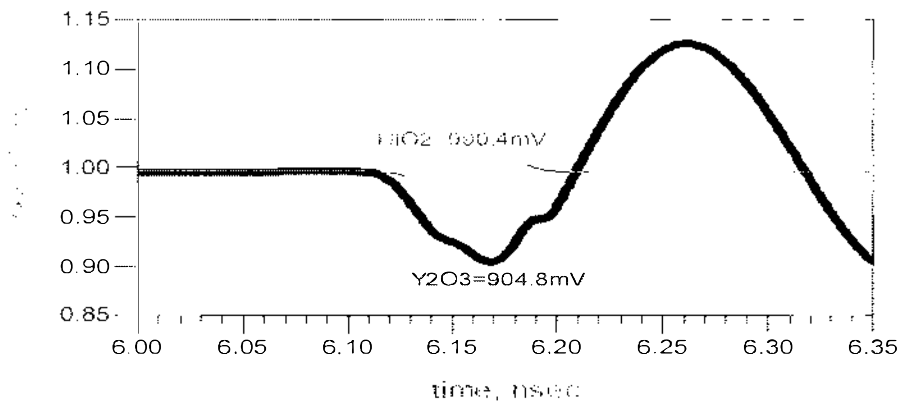

Figure 19: Showing voltage droop for HfO_2 and Y_2O_3

So we can say that the oxide thickness is also a matter that affects the voltage droop, even though the material has the lower low tangent.

6. PROPOSED CAPACITOR COMPONENTS

From the previous chapter we already know about the voltage droop and its effect on microprocessor power delivery system. So the main objective of ours is to reduce the voltage droops and decoupling capacitor is one of the solutions to oppose the voltage droops. In our thesis we design few capacitor models using high-k material with low loss tangent and compare those with SiO_2.

6.1. Why We Use High-K Material In Designing Capacitor:

Over 40 years ago, since the introduction of the metal-oxide-semiconductor (MOS) system the SiO2 gate oxide has been serving as the key enabling material in scaling silicon CMOS technology. As we already know that to reduce cost, maintaining low power consumption and increasing performance devices are scaling day by day so we need to scale down the SiO2 gate oxide. However continued SiO2 gate oxide scaling is becoming difficult since (a) the gate oxide leakage is increasing with decreasing SiO2 thickness and (b) SiO2 is running out of atoms for further scaling.[40]

When devices scale and need high capacitance then the area occupied by the capacitor must scale in order to obtain a small cell size. To achieve high capacitance, the equivalent oxide thickness must be 1nm or lower. So below 90nm technology node replacing SiO2, high-k dielectric will allow the achieving of t_{ox} (equivalent oxide thickness) of <1nm. [41]

The "International Technology Roadmap for Semiconductors" published in 2008, predicts gate oxide thicknesses for the future devices which is given in Table 6.

Table 6: The data for equivalent oxide thickness for future technology given by ITRS

Year	2015	2016	2017	2018	2019	2020	2021	2022
Equivalent oxide thickness t_{ox}(nm)	1.1	1.1	1	1	0.9	0.9	0.8	0.8

So the "International Technology Roadmap for Semiconductors" predicts gate oxide thicknesses cannot be achieved by using SiO_2 that's why high-k gate dielectrics and gate electrodes will be required for the future application.

Decoupling capacitors need to be placed close to the chip to reduce the voltage droop. However, in our project we want to show that at high frequency loss tangent is another factor that reduces the

effectiveness of the capacitance, despite being close to the circuit. As a result the effectiveness of the decoupling capacitor for reducing voltage droop is reduced due to loss tangent of capacitor dielectric. Thus the designed circuits fail to provide its desired performance at high frequency. So first we need to know about loss tangent and how it affects on the effectiveness of capacitance.

6.2. What Is Loss Tangent?

In conductive materials, currents are formed by the motion of free electrons or holes under the influence of an electric field. The relation is J=σE, where σ is the material conductivity. For finite conductivity, resistive heating of the material causes wave power losses. We need to understand the complex permittivity as it relates to the conductivity. Thus the permittivity becomes complex, and from Maxwell's equation we know,

$$\nabla \times H = J - \frac{\partial D}{\partial t} = \sigma E - j\omega\varepsilon E \quad \ldots\ldots (1)$$

$$\nabla \times H = \sigma E - j\omega(\varepsilon' - j\varepsilon'')E \quad \ldots\ldots (2)$$

where $\varepsilon = \varepsilon' - j\varepsilon''$; ε' – real or lossless part of ε and ε'' = imaginary or lossy part of ε.

$$\nabla \times H = [(\sigma - \omega\varepsilon'') - j\omega\varepsilon']E$$

$$\nabla \times H = (\sigma' - j\omega\varepsilon')E \quad \ldots\ldots (3)$$

where $\sigma' = \sigma - \omega\varepsilon''$ = equivalent conductance.

It is clear that ε'' the imaginary part of ε is involved in a frequency-dependent term $\omega\varepsilon''$ with the dimension of conductance. For dc, $\omega = 0$ and therefore $\omega\varepsilon'' - 0$ so power loss is small in a good dielectric conductance for which σ is small. However at high frequency ω is very large so losses can become larger as $\omega\varepsilon''$ becomes significant. The sum of σ and $\omega\varepsilon''$ constitutes what may be the called the equivalent conductivity σ'. [42]

Now the two terms of the right hand side of equation (3) are conduction current density, $J\sigma s = \sigma'$E and displacement current density $Jds = j\omega\varepsilon'$E. If we take the ratio of conduction current density displacement current density magnitude then we got.

$$\frac{J\sigma s}{Jds} = \frac{\varepsilon''}{\varepsilon'} = \frac{\sigma'}{j\omega\varepsilon'} \quad \ldots\ldots (4)$$

These two vectors point in the same direction in space, but they are 90° out of phase in time. The displacement current density leads conduction current density by 90°, just as the current through a

pacitor leads the current through a resistor in parallel with it by 90° in an ordinary electric circuit. nis phase relationship is shown below in Fig.20,

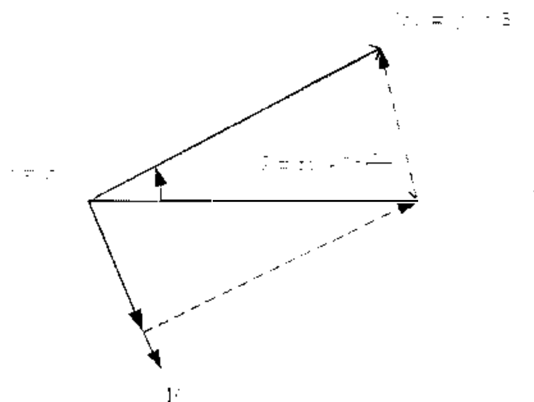

Figure 20: Showing the power factor angle where Js is leads E to determine loss tangent.

ne angle is identified as the angle by which the displacement density leads the total current ensity and tan = . The ratio is called a loss tangent because it is a measure of power ss in the medium. [44]

6.3. Equivalent Model of a Capacitor:

'e know for a capacitor a dielectric is placed between two conductors. The lumped element model a capacitor is defined by a lossless ideal capacitor in series with a resistor which is known as the uivalent series resistance (ESR). The equivalent series resistance of a capacitor is shown in Fig. . The ESR actually represents the losses in the capacitor. In a low-loss capacitor the ESR is very nall, and in a lossy capacitor the ESR can be large. Basically ESR which is shown in Fig. 21 presents the loss due to both the dielectric's conduction electrons and the bound dipole relaxation nenomena.

) in a dielectric either the dielectric's conduction electrons or the bound dipole relaxation nenomena dominates loss. For the case of the conduction electrons being the dominant loss, where C is the lossless capacitance.

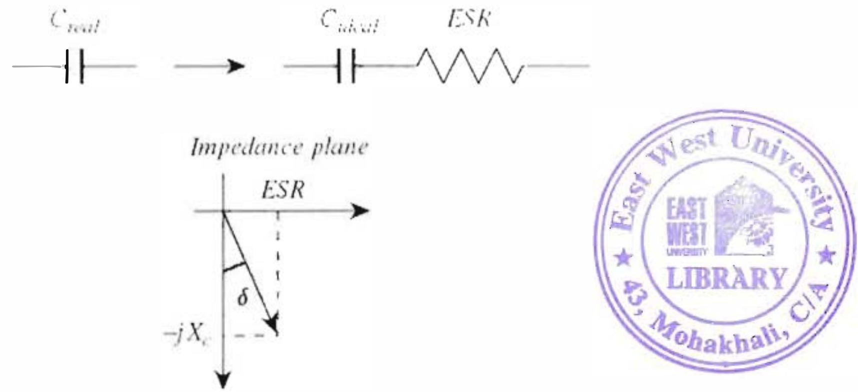

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Figure 21: Equivalent model of a capacitor and its loss tangents relation.

If we represents the electrical circuit parameters as vectors in a complex plane, then capacitor's loss tangent is equal to the tangent of the angle between the capacitor's ESR vector and the negative reactive capacitive vector, as shown in the above diagram. The loss tangent is then,

$$\tan\delta = \frac{ESR}{|Xc|} \quad \text{where } Xc = \frac{1}{\omega c}$$

$$= \omega c.\, ESR = \frac{\sigma}{\delta' \omega}$$

As the same AC current flows through both *ESR* and X_c, the loss tangent is also the ratio of the resistive power loss in the ESR to the reactive power oscillating in the capacitor. For this reason, a capacitor's loss tangent is sometimes stated as its dissipation factor or the reciprocal of its quality factor *Q*,

$$\tan\delta = DF = \frac{1}{Q}$$

So we can say from the above equation that as the loss tangent, δ decrease then the dielectric loss of the material will also be reduced.

6.4. The Effect of Loss Tangent on the Effectiveness of the Capacitance:

Now we want to consider how loss tangent eventually decreases the effectiveness of the capacitor. The capacitor consists of two conductors separated by dielectric medium which is shown in the Fig. 22 is shown below,

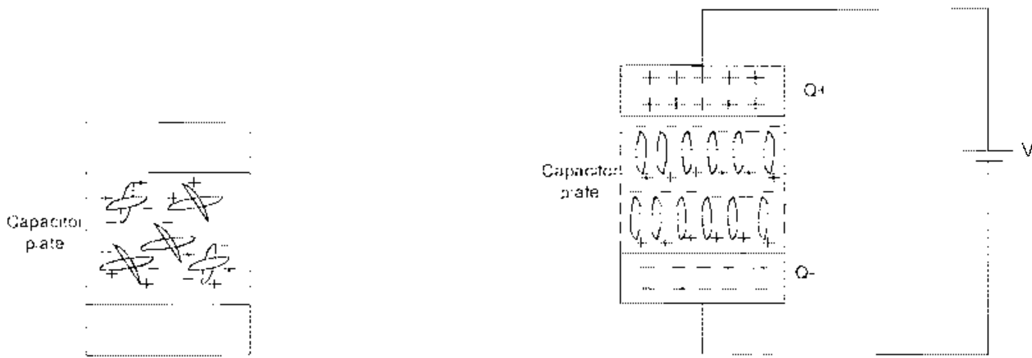

Figure 22: Initially without applied voltage V & after applied voltage V

When a dc voltage source is connected between the two conductors then charge will transfer where the positive charge will store in the upper conductor and the negative charge will store in the lower conductor. In the dielectric medium normally dipoles are randomly oriented. An applied electric field will exert a torque on the individual dipoles and tend to align these dipoles in the same direction. [45]

When the dipoles of the dielectric material rotate due to charges on the plates. some energy is lost as heat. This phenomenon is the one of the factors which results in reduced storage charge of the capacitor. Also at high switching frequencies due to the very small rise times, the dipoles are not able to rotate fast enough, thereby unable to either store charges on the plate or supply the charge quick enough. Thus, the performance of the capacitor is degraded [43]. This loss in the capacitor performance can be characterized as a degradation of the capacitor itself at high frequencies.

If Q is the total charge storage in the capacitor before taking the loss into consideration,

$$Q=CV \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

When ∇Q representing the loss, such that $Q' = Q - \nabla Q$, then

$$Q' = CV \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (5),$$

where V is desired voltage level and C is the capacitance.

om equation (5) we see that when Q decreases, the effective capacitance will also decrease, if we ꞏ to keep the voltage level stable. Thus if we increase the switching frequency then the loss tangent a function of frequency will increase eventually decreasing the effectiveness of the capacitor. The ange in loss tangent of water with frequency is shown in Fig. 23 [45].

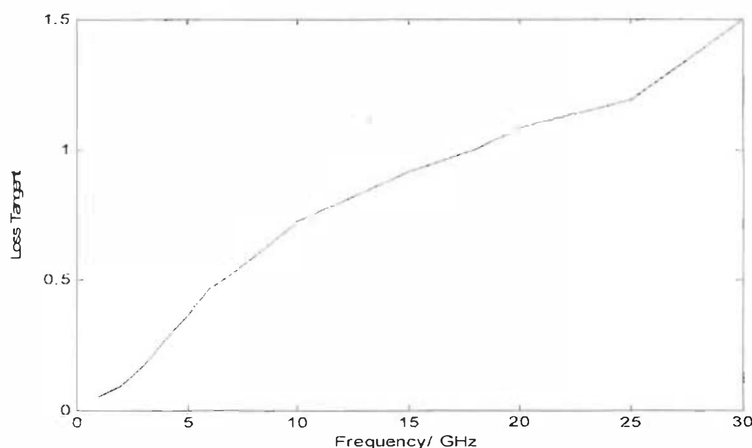

Figure 23: Change in loss tangent of water with frequency.

Fig. 23 we see that with increase in frequency, tan δ (loss tangent) also increases, almost linearly. nis data represents tan δ for water. If we draw parallels with capacitor dielectric, we see that with creasing frequency capacitor becomes relatively lossy as switching frequency increases. The ermal losses at high frequencies are reduces due to the inability of the dipoles to switch quick nough, but nevertheless it also means that the capacitor cannot provide the necessary electrical ipport to limit voltage droop [45]. Thus, the system performance will be degraded.

6.5. Our Proposed Capacitor Material:

om the above discussion we understand that at high frequency the capacitor didn't work properly at's why we used two different low loss tangent high-k materials for designing capacitors model id also we maintain same capacitance value for the two material by adjusting their equivalent oxide ickness t_{ox}. We used these capacitors in power delivery system in ADS software and observed the iange in voltage droop. We mainly work on Hafnium Oxide (HfO_2) and Lanthanum Oxide (La_2O_3) aterial and compare between them on the effect of voltage droop. Here we kept the capacitance me for the two materials by changing the oxide thickness. To make the same capacitance value we

O_2 as reference which has thickness of 0.1um and then calculate the other material thickness. ulation is given in results and simulation part. Then we design the two capacitor model and them in ADS software which is briefly shown in simulation part. Now we will show that ovement of voltage droop by using these capacitor model. The simulation figure is shown in

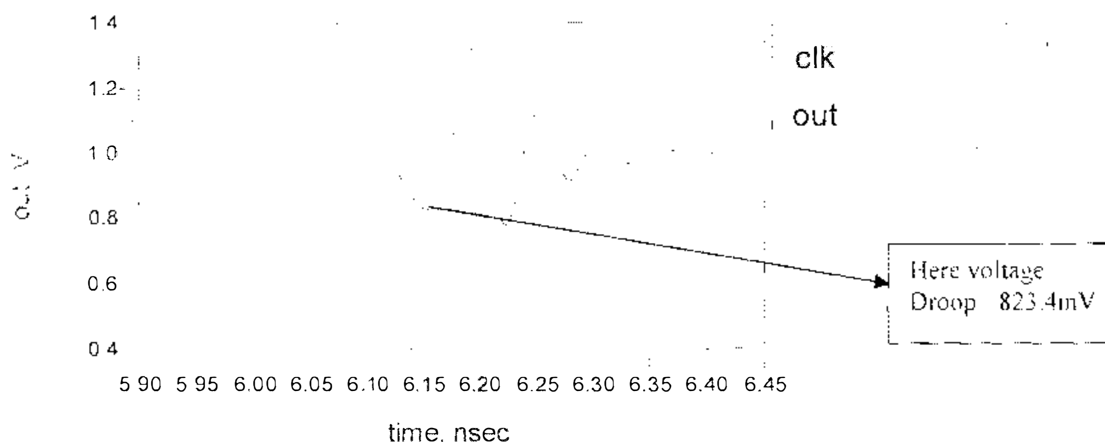

Figure 24: Simulation result without using decoupling capacitor

nize the voltage droop we placed the decoupling capacitors with different high-k materials. nge in voltage droop is shown in Fig. 25. It shows the voltage droops for HfO_2 and La_2O_3.

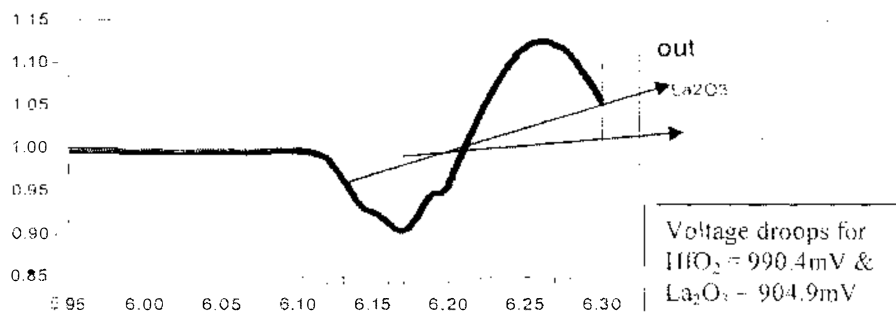

Figure 25: Simulation result when placing decoupling capacitor by using HfO_2 and La_2O_3 material

lue we got for the voltage droop from the simulation is compared with a case where neither oupling is used. All this is shown in Table 7.

Table 7: Voltage droops we got for different materials

Condition	Voltage Droop(mV)
Without Capacitor	823.4
With Capacitor(HfO_2)	990.4
With Capacitor(La_2O_3)	904.9

ı the data we can say that for edge rate of 0.1ns without using decoupling capacitor the voltage ɔ is 823.4 mV which is improved by placing our designed capacitor. Here we can also say that een two materials HfO_2 & La_2O_3, the voltage droop is minimized by using HfO_2 which has r loss tangent than La_2O_3.

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7. CONCLUSION

.s paper we recommended a high-k dielectric decoupling capacitor stack model which can e voltage droops at high frequency with acceptable performance degradation. In semiconductor es voltage droop significantly affects the performance of critical circuits. The occurrence of ge droop is primarily due to parasitic components in the power delivery network which cannot iminated. Decoupling capacitors are used as charge storage devices which reduce voltage os by providing immediate charge needs during switching events. However, at high frequencies ipling capacitors don't work properly as for the extreme conduction of electricity in dielectric ·ial. If we use such a dielectric material which has higher dielectric constant and lower loss nt, as a decoupling capacitor's dielectric, then it is possible that the decoupling capacitor can ite at high frequency as it has lower loss tangent means lower inherent dissipation of ·omagnetic energy and for the higher dielectric constant it can store more charge & the size of ipacitor reduces due to the scale down of the gate oxide.

esign the stack model of decaps we use ADS (Advance Design System) software. Using entum we designed two planar capacitors where two different high-k materials, hafnium oxide $_2$) and lanthanum oxide (La_2O_3) were used. We then placed the two stack capacitor models ately into our power delivery circuit. For different capacitance values, we changed the ness of the capacitors. From our ADS simulation we found out that after placing our design os in high frequency the voltage droop is improved which means the circuit performance will be r. We then used the lower loss tangent high-k material capacitor with which we got better rmance. The higher loss tangent La_2O_3 showed greater voltage droop as compared with lower angent HfO_2 at high frequency operations.

8. FUTURE WORK

is paper we demonstrate that the hafnium oxide (HfO_2) is a good dielectric material as it can ate at high frequency while minimizing the voltage droop. But in near feature it is very likely ble that better material can be found to take the place of the hafnium oxide. In the selection ess of dielectric material we identified zirconium oxide (ZrO_2) which has lower loss tangent the hafnium oxide (HfO_2). With circuits operating at higher frequencies, materials which can ate in a very high frequency with minimum degradation in dielectric constant and low loss ent have to be identified.

9. REFERENCES

.. N. Das, M. D. Poliks, J. M. Lauffer and V. R. Markovich, "High Capacitance, Large Area, 'hin Film, Nanocomposite Based Embedded Capacitors", Endicott Interconnect Technologies, ıc., 1701 North Street, Endicott, New York, 13760.

:. Meng, K. Arabi, and R. Saleh, "Novel decoupling capacitor designs for sub-90nm CMOS :chnology," *International Symposium on Quality Electronic Design (ISQED)*, pp. 266 - 272, 1ar. 2006.

‹I. Popovich , E. G. Friedman , R. M. Secareanu , O. L. Hartin, "Efficient placement of istributed on-chip decoupling capacitors in nanoscale ICs", in *Proc. IEEE/ACM international 'onf. Computer-aided Design*, San Jose, California, Nov.'2007, pp. 811-816.

. Jun, J. L. Knighten, A. Orlandi, N. W. Smith, and J. L. Drewniak, "Quantifying decoupling ıpacitor location," *IEEE International Symposium on Electromagnetic Compatibility*, vol. 2, pp. 61-766, Aug. 2000.

. Mitra , S. Bhattacharjee , S. Sur-Kolay , B. B. Bhattacharya , S. T. Zachariah , S. Kundu, "Test attern Generation for Power Supply Droop Faults", in *Proc. 19th International Conf. on VLSI 'esign*, Jan. 2006, pp. 343-348.

1. Popovich, E. G. Friedman, "Decoupling capacitors for multi-voltage power distribution 'stems", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol.14, no.3, pp. 17-228, Mar. 2006.

. E. Engin1, A. Tambawala1, M. Swaminathan, S. Bhattacharya1, P. Pramanik, K. Yamazaki,)ielectric Constant and Loss Tangent Characterization of Thin High-K Dielectrics Using orner-to-Corner Plane Probing", *IEEE Electrical Performance of Electronic Packaging*, pp.29- 2, Oct. 2006.

Lu, C. P. Wong, "Recent Advances in High-*k* Nanocomposite Materials for Embedded ıpacitor Applications", *IEEE Transactions on Dielectrics and Electrical Insulation*, vol. 15, no. pp. 1322-1328, Oct. 2008.

Mahajan, K. Brown, V. Atluri, "The Evolution of Microprocessor Packaging", *Intel Journal of chnology*, Apr. 2000.

Li, L. Fang, M.S. Hsiao, "Efficient power droop aware delay fault testing", in Proc. of Test ınf. of ITC 2007, IEEE International, Jan. 2008.

M. Salahuddin, S. Raju and M. I. Raza," Localized Trench Decoupling to Reduce On-Chip ltage Droop", paper submission to IEEE Trans.CAD.

Aug'un, M. J. Hill, K. Eilert, K. Radhkrishnan, A. Levin, "Power Delivery for High- formance Microprocessors", *Intel Journal of Technology*, vol. 9, no. 4, Nov. 2005.

S. Sraboni, O. Mohaimen, R. H. Mustazir. and S. M. Salahuddin, and M. I. Raza, "Improved SI Circuit Performance using Localized Power Decoupling", *in proc. 5th ICECE Conf. on ctrical & Computer Engineering*, Dhaka, Bangladesh, Dec. 20-22, 2008.

Pei, R. Booth, H. Ho, N. Kusaba, X. Li, M. Brodsky, P. Parries, H. Shang, R. Divakaruni, S. er, "A Novel, Low-Cost Deep Trench Decoupling Capacitor for High-Performance, Low-Power ılk CMOS Applications", in *Proc. 9th International Conf. Solid-State and Integrated-Circuit chnology,* Beijing, China, 2008.

G. Nickel, J. F. Rosenberger, S. W. Crane, Jr. Z. Horvath, J. Jeon, P. T. Codd, A. C. ıngellaris, "A Novel Decoupling Capacitance Platform for Substrates, Sockets, and .erposers", *presented at the 6th Electronic packaging Technology,* Singapore, Dec. 8-10, 2004

Facchetti, M. H. Yoon and T. J. Marks, "Gate dielectrics for organic field-effect transistors: w opportunities for organic electronics", *Advance Materials (Adv.Mater.),* vol. 17, no. 14, pp. 05-1725, 2005.

Bai, Z. Y. Cheng, V. Bharti, H. S. Xu and Q. M. Zhang, "Highdielectric- constant ceramic-wder polymer composites", *Applied Physics Letters (AIP),* vol. 76, pp. 3804-3806, Apr. 2000.

M. Zhang, H. F. Li, M. Poh, F. Xia, Z. Y. Cheng and H. S. Xu, "An all-organic composite tuator material with a high dielectric constant", *Nature,* vol. 419. pp. 284-287, Sep. 2002.

K. Ulrich, L. W. Schaper, *Integrated Passive Component Technology,* in *Handcover* Wiley-EE Press, 2003.

Prymark, S. Bhattacharya, K. Paik and R. R. Tummala, *Fundamentals of Microsystems ckaging,* New York: McGraw-Hill, 2001.

A. Muller, T. Sorsch, S. Moccio, F.H. Baumann, K. Evans-Lutterodt, and G. Timp, "*The ectronic structure at the atomic scale of ultrathin gate oxides,*" Nature, vol. 399, pp. 758–762, 99.

S. Momose, M. Ono, T. Yoshitomi, T. Oghmo, S. Nakamma, M. Saito, and H. Iwai, unneling gate oxide approach to ultra-high current drive in small geometry MOSFETs," *ectron Devices Meeting, 1994. IEDM '94. Technical Digest., International.,* pp. 593–596, 1994

Taur, D.A. Buchanan, W. Chen, D. J. Frank, K.E. Ismail, S.-H. Lo, G.A. Sai-Halong, R.C. swanathan, H.-J. C. Wann, S.J. Wind, and H.-S. Wong, "CMOS scaling into the nanometer gime." *Proceedings of the IEEE,* vol. 85, pp. 486 504, 1994.

. Hauser and W.T. Lynch, available at Semiconductor Research Corporation website, vw.src.org (1998)

. Association, the National Technology Roadmap for Semiconductors (Sematech, Austin, 99.

Gerstenberg, *Handbook of Thin Film Technology,* McGraw-Hill, New York, 1970

Nakane, A. Noya, S. Kuriki, and G. Matsumoto, "Dielectric properties of europium oxide ms." *Thin Solid Films,* vol. 59, Issue 3, pp. 291–293, 1979.

Mahalingham, M. Radhakrishnan, and C. Balasubramanian, "Dielectric behaviour of thanum oxide thin film capacitors," *Thin Solid Films,* vol. 78, pp. 229–233, 1981.

Wiktorczyka and C. Wesołowska, "Dielectric behaviour of Yb2O3 thin film capacitors," *Thin id Films,* vol. 120, Issue 3, pp.171-178, 1984

.. W. Schaper, *Integrated Passive Component Technology*, Wiley-IEEE Press, 2003.

I. Tohge, S. Takahashi and T. Minami, "Preparation of PbZrO3-PbTiO3 ferroelectric thin films y the sol-gel process", *J. Am. Ceram. Soc.*, vol.7, pp. 67-71, 1991.

.T. Vo, T. Lacrevaz, B. Flechet "In-situ Microwave Characterization of Medium-k HfO2 and ligh-k STO Dielectrics for MIM Capacitors Integrated in Back-End of Line of IC", *presented at PMC Conf. Microwave,* Asia-Pacific, pp. 1-4, 11-14, Dec. 2007.

1. Popovich, A. V. Mezhiba, and E. G. Friedman, *Power Distribution Networks With On-Chip Decoupling Capacitors*, Springer Publishers, 2008.

1. Popovich and E. G. Friedman, "Decoupling capacitors for multivoltage power distribution ystems," *IEEE Trans. Very Large Scale Integr.(VLSI) Syst.*, vol. 14, no. 3, pp. 217–228, Mar. 006

. Smith, "Decoupling Capacitor Calculations for CMOS Circuits," in *Proc.3rd IEEE Topical Meeting of Electrical Performance of Electronic Packaging*, pp. 101-105, Nov. 1994.

I. Su, S. S. Sapatnekar, and S. R. Nassif, "Optimal Decoupling Capacitor Sizing and Placement or Standard-Cell Layout Designs,"*IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, No. 4, pp. 428--436, Apr. 2003.

. Zhao, K. Roy, and C.-K. Koh, "Decoupling Capacitance Allocation and Its Application to ower-Supply Noise-Aware Floorplanning," *IEEE Transactions on Computer-Aided Design of ntegrated Circuits and Systems*, vol. 21, No. 1, pp. 81–92, Jan. 2002.

1. Popovich, E. G. Friedman, M. Sotman, A. Kolodny, and R. M. Secareanu, "Maximum ffective distance of on-chip decoupling capacitorsin power distribution grids," in *Proc. ACM Great Lakes Symp. VLSI*, May. 2006, pp. 173–179

. Chau, J. Brask, S. Datta, B. Doyle, J. Kavalieros, A. Majumdar, G. Dewey, M. Doczy, B. Jin, 1. Metz and Radosavljevic, " Application of High-k Gate Dielectrics and Metal Gate Electrodes enable Silicon and Non-Silicon Logic Nanotechnology", in *Proc. 14th biennial conf. on nsulating films on semiconductors*, vol. 80, pp. 1-6, Jun. 2005.

ich Liu and Tai-Bor Wu, "Application of High Dielectrics in CMOS Technology and Emerging lew Technology", *International symposium on advanced short-time thermal processing for Si-ased CMOS devices*, Paris , France, vol. 14, pp. 207-216, Apr. 2003.

D. Kraus, D. A. Fleisch, *Electromagnetics with Application,* 5th ed. New York: McGraw-Hill.

. K. Cheng, *Field and Wave Electromagnetics*, 2nd ed. New York: McGraw-Hill.

/. H. Hayt, Jr. J. A. Buck. *Engineering Electromagnetics*, 7th ed. New York: McGraw-Hill.

. E. Dubroff, S.V. Marshall, G. G. Skitek, *Electromagnetic Concepts and Applications*, 4th ed. ew York: McGraw-Hill.

.P Lewis, G. P, Shaw, A. Al-Shamma, A. I, Wylie. S. R, Riby. P, Alkhaddar. R and Phipps. D, *Tunable High Frequency Microwave Assisted Chemistry* ", 2nd GERI Annual Research ymposium GARS-2006, Liverpool, UK, Jun. 15, 2006.

Appendix

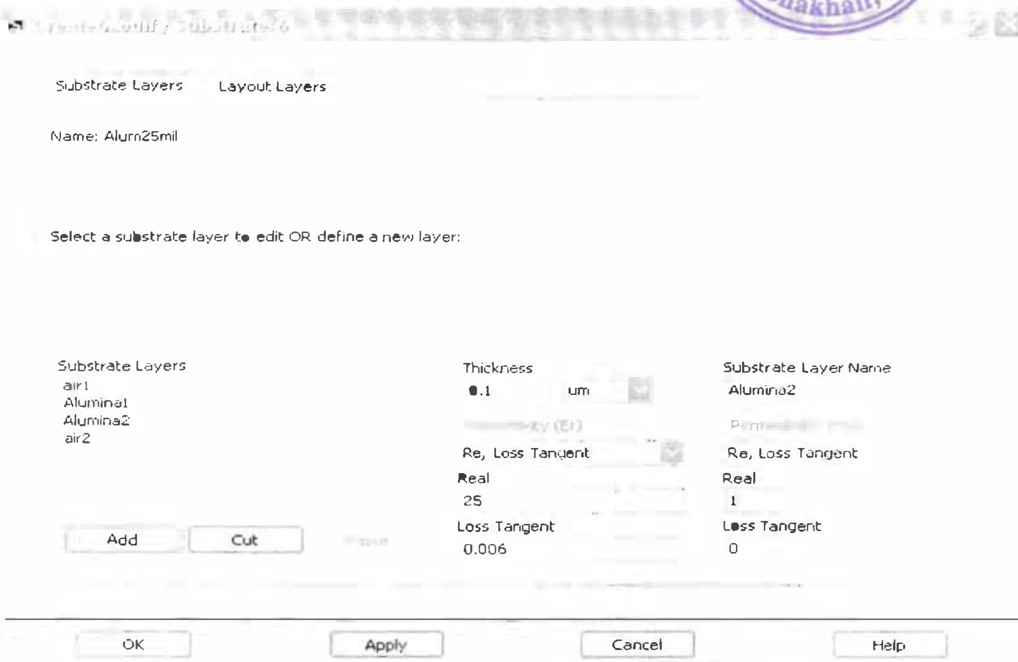

Figure 26: The ADS substrate layers window showing the declaration parameter while designing capacitor

Figure 27: The ADS Layout layers window showing the declaration parameter while designing capacitor