PERFORMANCE ANALYSIS OF SI NANOWIRE TRANSISTORS USING TOP OF THE BARRIER QUANTUM MODEL

By

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Abstract

After more than 30 years of validation of Moore's law, the CMOS technology has already entered the nanoscale (sub-100nm) regime and faced strong limitations. The nanowire transistor is one of the candidates which have the potential to overcome the problems caused by short channel effects in SOI (Silicon on insulator) MOSFETs. The nanowire transistors have gained significant attention from both device and circuit developers. Accurate modeling and calculations based on quantum mechanics are necessary to theoretically assess their performance limits. In this thesis we have studied the performance of silicon nanowire transistors using top of the barrier quantum model. We then studied the effects of wire width on device performance metrics such as on/off current ratio, switching delay, unity current gain frequency etc.

Acknowledgements

We would like to express our heartiest gratitude to our thesis supervisor, Dr. Khairul Alam, Assistant professor, Department of Electrical and Electronics Engineering for his invaluable advices and consecutive supports for this research. He has selected the research topic and provided us precious ideas. His strict attitude in research and teaching, his generosity and considerateness to students makes the whole work possible. We would also like to thanks Dr. Anisul Haque and Dr. Ishfaqur Raza for their support. Special thanks go to our parents who provide supports to make this work. We would also like to thank M.a.Jobayer Bin Bakkre, lab officer of VLSI laboratory for his help.

However, thoroughly expressing our thankfulness to our supervisor is certainly beyond our ability in English writing, and it would either be nearly impossible even if we could do it in our native language.

We apologize for unintentional errors in printing, if any.

Authorization page

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1. Introduction

1.1. BASIC MOSFET OPERATION

A basic n-channel MOSFET (Figure 1.1.A) consists of two heavily-doped n-type regions, the drain and source, which contain the most important terminals of the device. Previously the gate was made by metal, but is now made of heavily doped polysilicon, while the bulk of the device is p-type and is typically rather lightly doped [1]. We will assume that the substrate (bulk) terminal is at the equal potential as the source. However, it is extremely important to keep in mind that the substrate constitutes a fourth terminal, whose influence cannot always be ignored [1]. As an increasing positive voltage is applied to the gate, holes are progressively repelled away from the surface of the substrate [1]. At some particular value of gate voltage (the threshold voltage V_T), the surface becomes completely depleted of charge. Further increases in gate voltage induce an inversion layer. When a drain-source bias V_{DS} is applied then a conductive path ("channel") constitutes between source and drain.

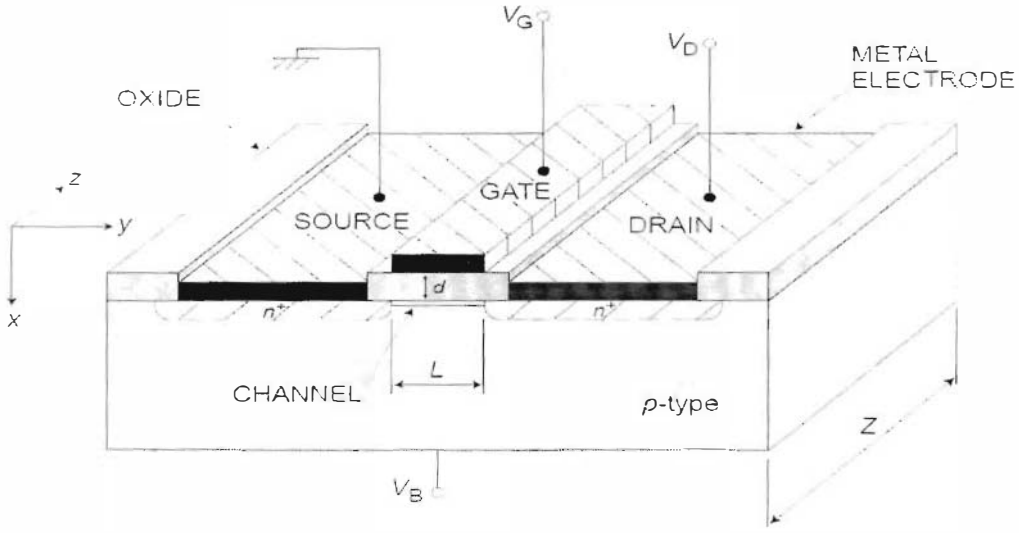

Figure 1.1.1 : Three dimensional view of an n-channel MOSFET with conducting channel and depletion region [2]

A change in the gate-source voltage V_{GS} alters the electron sheet density in the channel, modulating the channel conductance and the device current [3]. For $V_{GS} > V_T$ in an *n*-channel device, the application of a positive V_{DS} gives a steady voltage increase from source to drain along the channel that causes a corresponding reduction in the local gate-channel

bias V_{GX} (here X signifies a position x within the channel)[3]. This reduction is greatest near drain where V_{GX} equals the gate-drain bias V_{GD} [3]. Somewhat simplistically, we may say that when $V_{GD} = V_T$, the channel reaches threshold at the drain and the density of inversion charge vanishes at this point. This is called pinch-off condition, which leads to a saturation of the drain current I_{DS}. The corresponding drain-source voltage, $V_{DS} = V_{SAT}$, is called the saturation voltage. Since $V_{GD} = V_{GS} - V_{DS}$, we find that $V_{SAT} = V_{GS} - V_T$. When $V_{DS} > V_{SAT}$, the pinched-off region near drain expands only slightly in the direction of the source, leaving the remaining inversion channel intact. The point of transition between the two regions, $x = x_p$, is characterized by $V_{XS}(x_p) \approx V_{SAT}$, where $V_{XS}(x_p)$ is the channel voltage relative to source at the transition point. Hence, the drain current in saturation remains approximately constant, given by the voltage drop V_{SAT} across the part of the channel that remains in inversion. The voltage $V_{DS} - V_{SAT}$ across the pinched-off region creates a strong electric field, which efficiently transports the electrons from the strongly inverted region to the drain [3].

Typical current–voltage characteristics of a long-channel MOSFET, where pinch-off is the predominant saturation mechanism, are shown in Figure 1.1.B However, with shorter MOSFET gate lengths, typically in the sub micrometer range, velocity saturation will occur in the channel near drain at lower V_{DS} than that causing pinch-off. This leads to more evenly spaced saturation characteristics than those shown in this figure. more in

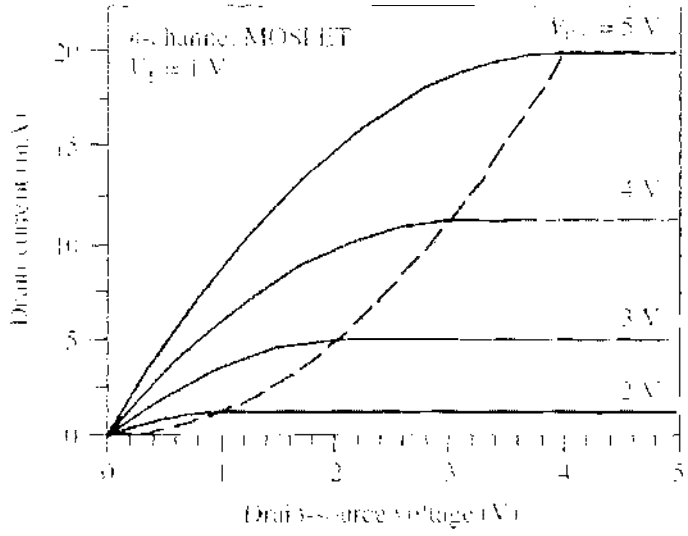

Figure 1.1.2: Current–voltage characteristics of an *n*-channel MOSFET with current saturation caused by pinch-off (long-channel case). The intersections with the dotted line indicate the onset of saturation for each characteristic. The threshold voltage is assumed to be $V_T = 1V$ [4]

agreement with those observed for modern devices. Also, phenomena such as a finite channel conductance in saturation, a drain bias–induced shift in the threshold voltage, and an increased sub threshold current are important consequences of shorter gate lengths.

1.2. MOSFET scaling

From the past few decades, we saw that the MOSFET has continuously been scaled down in size; typical MOSFET channel lengths were once several micrometers, but in current time integrated circuits are incorporating MOSFET with channel lengths in nanometer scale. Intel began production of a process featuring a 32 nm feature size (with the channel being even shorter) in late 2009[5]. The semiconductor industry maintains a "roadmap", the ITRS (International Technology Roadmap for Semiconductors), which sets the scaling speed for MOSFET development. Historically, the difficulties with decreasing the size of the MOSFET have been associated with the semiconductor device fabrication process, the need to use very low voltages, and with poorer electrical performance such as higher leakage currents, and lower output resistance necessitating circuit redesign and innovation [5].

1.3. Reasons for MOSFET scaling

Smaller MOSFETs are advantageous for some reasons because if MOSFET are scaled down its possible to pack more and more devices in a given chip area. This results in a chip with the same functionality in a smaller area, or chips with more functionality in the same area. Since fabrication expenses for a semiconductor wafer are quite fixed, the cost per integrated circuits is mainly related to the number of chips that can be produced per wafer [5]. Smaller ICs permit more chips per wafer, reducing the price per chip. In fact, over the past 30 years the number of transistors per chip has been doubled every 2–3 years once a new technology node is introduced [5]. For example the number of MOSFETs in a microprocessor fabricated in a 45 nm technology is twice as large as in a 65 nm chip [5]. This doubling of the transistor count was first explained by Gordon Moore in 1965 and which is called Moore's law.

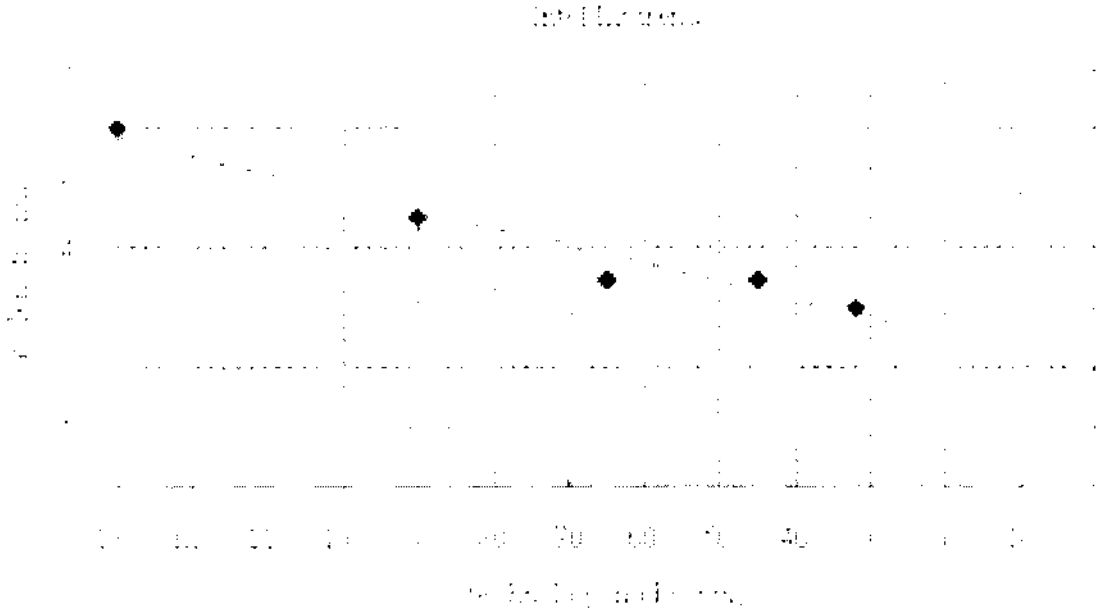

Figure1.3.1 : Trend of Intel CPU transistor gate length

It is also projected that smaller transistors switch faster. Scaling of the MOSFET requires all device dimensions to reduce proportionally. Transistor length, width, and the oxide thickness are the main device dimensions, suppose scale with a factor of 0.7 per node. This way, the transistor channel resistance does not change with scaling, while gate capacitance is reduced by a factor of 0.7. Hence, the RC delay of the transistor scales with a factor of 0.7 [5].That's why the switching delay is also reduced so, it is expected that smaller transistors switch faster.

While this has been traditionally the case for the older technologies, for the state-of-the-art MOSFETs reduction of the transistor dimensions does not necessarily translate to higher chip speed because the delay due to interconnections is more important.

1.4.Difficulties arising due to MOSFET size reduction

Producing MOSFETs with channel lengths much smaller than a micrometer is a challenge, and the difficulties of semiconductor device fabrication are always a limiting factor in advancing integrated circuit technology. In recent years, the small size of the MOSFET has created operational problems.

1.4.1. Higher sub threshold conduction

As MOSFET geometries shrink, the voltage that can be applied to the gate must be reduced to maintain reliability. To maintain performance, the threshold voltage of the MOSFET has to be reduced as well. As threshold voltage is reduced, the transistor cannot be switched from complete turn-off to complete turn-on with the limited voltage swing available; the circuit design is a compromise between strong current in the "on" case and low current in the "off" case, and the application determines whether to favor one over the other [5]. Sub threshold leakage (including sub threshold conduction, gate-oxide leakage and reverse-biased junction leakage), which was ignored in the past, now can consume upwards of half of the total power consumption of modern high-performance VLSI chips [5].

1.4.2. Increased gate-oxide leakage

The gate oxide, which serves as insulator between the gate and channel, should be made as thin as possible to increase the channel conductivity and performance when the transistor is on and to reduce sub threshold leakage when the transistor is off. However, with current gate oxides with a thickness of around 1.2 nm (which in silicon is ~5 atoms thick) the quantum mechanical phenomenon of electron tunneling occurs between the gate and channel, leading to increased power consumption [5].

Insulators (referred to as high-k dielectrics) that have a larger dielectric constant than silicon dioxide, such as group IVb metal silicates e.g. hafnium and zirconium silicates and oxides are being used to reduce the gate leakage from the 45 nanometer technology node onwards[5]. Increasing the dielectric constant of the gate dielectric allows a thicker layer while maintaining a high capacitance (capacitance is proportional to dielectric constant and inversely proportional to dielectric thickness). All else equal, a higher

dielectric thickness reduces the quantum tunneling current through the dielectric between the gate and the channel. On the other hand, the barrier height of the new gate insulator is an important consideration; the difference in conduction band energy between the semiconductor and the dielectric (and the corresponding difference in valence band energy) also affects leakage current level. For the traditional gate oxide, silicon dioxide, the former barrier is approximately 8 eV [5]. For many alternative dielectrics the value is significantly lower, tending to increase the tunneling current, somewhat negating the advantage of higher dielectric constant.

1.4.3. Increased junction leakage

To make devices smaller, junction design has become more complex, leading to higher doping levels, shallower junctions, "halo" doping and so forth, all to decrease drain-induced barrier lowering [5]. To keep these complex junctions in place, the annealing steps formerly used to remove damage and electrically active defects must be curtailed increasing junction leakage [5]. Heavier doping is also associated with thinner depletion layers and more recombination centers that result in increased leakage current, even without lattice damage.

1.4.4. Lower output resistance

For analog operation, good gain requires high MOSFET output impedance, which is to say, the MOSFET current should vary only slightly with the applied drain-to-source voltage [5]. As devices are made smaller, the influence of the drain competes more successfully with that of the gate due to the growing proximity of these two electrodes, increasing the sensitivity of the MOSFET current to the drain voltage. To counteract the resulting decrease in output resistance, circuits are made more complex, either by requiring more devices, for example the cascode and cascade amplifiers, or by feedback circuitry using operational amplifiers, for example a circuit like that in the bellow figure [5].

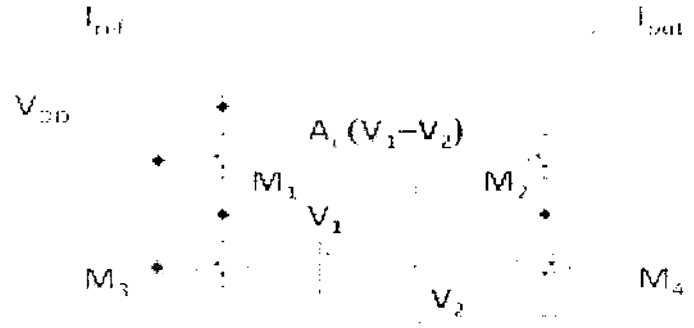

Figure 1.4.4.1: MOSFET version of gain-boosted current mirror; M1 and M2 are in active mode, while M3 and M4 are in Ohmic mode, and act like resistors. The operational amplifier provides feedback that maintains a high output resistance

1.4.5. Lower transconductance

The transconductance of the MOSFET decides its gain and is proportional to hole or electron mobility. At least for low drain voltages. As MOSFET size is reduced, the fields in the channel increase and the dopant impurity levels increase. Both changes reduce the carrier mobility, and hence the transconductance. As channel lengths are reduced without proportional reduction in drain voltage, raising the electric field in the channel, the result is velocity saturation of the carriers, limiting the current and the transconductance [5].

1.4.6. Interconnect capacitance

Traditionally, switching time was roughly proportional to the gate capacitance of gates. However, with transistors becoming smaller and more transistors being placed on the chip, interconnect capacitance (the capacitance of the wires connecting different parts of the chip) is becoming a large percentage of capacitance [5]. Signals have to travel through the interconnect, which leads to increased delay and lower performance.

1.4.7. Heat production

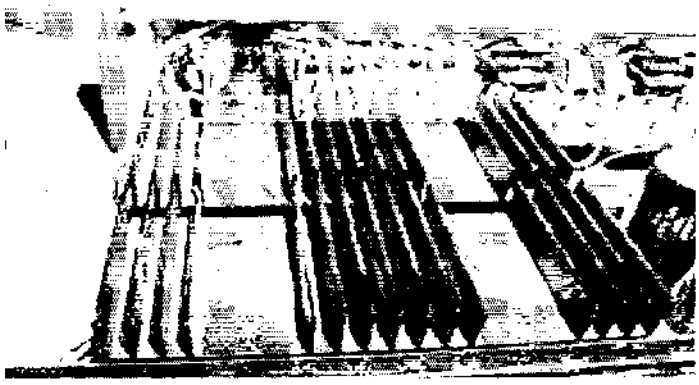

Figure 1.4.7.1: : Large heat sinks to cool power transistors in a TRM-800 audio amplifier

The ever-increasing density of MOSFETs on an integrated circuit is creating problems of substantial localized heat generation that can impair circuit operation. Circuits operate slower at high temperatures, and have reduced reliability and shorter lifetimes. Heat sinks and other cooling methods are now required for many integrated circuits including microprocessors. Power MOSFETs are at risk of thermal runaway. As their on-state resistance rises with temperature, if the load is approximately a constant-current load then the power loss rises correspondingly, generating further heat [5]. When the heat sink is not able to keep the temperature low enough, the junction temperature may rise quickly and uncontrollably, resulting in destruction of the device [5].

1.4.8. Process variations

With MOSFETS becoming smaller, the number of atoms in the silicon that produce many of the transistor's properties is becoming fewer, with the result that control of dopant numbers and placement is more unpredictable [5]. During chip manufacturing, random process variations affect all transistor dimensions: length, width, junction depths, oxide thickness etc., and become a greater percentage of overall transistor size as the transistor shrinks. The transistor characteristics become less certain, more statistical. The random

nature of manufacture means we do not know which particular example MOSFETs actually will end up in a particular instance of the circuit [5]. This uncertainty forces a less optimal design because the design must work for a great variety of possible component MOSFETs.

1.5. Modeling challenges

Integrated Circuits in current time are simulated by computer to achieve the goal of obtaining working circuits from the very first manufactured lot. As devices are scaled down, the complexity of the processing is increased and makes it more difficult to predict exactly what the final devices look like, and also the modeling of physical processes becomes more difficult as well. In addition, microscopic variations in structure due simply to the probabilistic nature of atomic processes require statistical predictions [5]. These factors combine to make sufficient simulation and difficulty arises in manufacture.

1.6. Nanowire Transistor

Source-to-drain tunneling, carrier mobility, process variations, and static leakage are some of the fundamental problems of MOSFET-inspired devices for sub-10nm channel length [6]. Power scaling is a simultaneous concern. However, it appears that emerging device architectures can extend the CMOS lifetime and provide solutions to continue scaling into the nanometer range or at least until the 10 nm walls is reached [6]. But what comes after this limit? The nanowire transistor is one candidate which has gained significant attention from both device and circuit developers because of its potential for building highly thick and high performance electronic products. Nanowire transistors can be made by using different materials such as glass or plastics which are low cost substrates [6]. Si and Ge nanowire transistors are predominantly more importance because of their compatibility with CMOS technology.

1.6.1. Background of Silicon Nanowire Transistors

The tremendous progress in IC technology in the past few decades causing a revolution which has become the driving power of the Information Technology revolt, which has stunningly changed the whole world. The secret of the sensation in IC technology is

actually simple: scaling down the dimension of each transistor, the basic element of integrated circuits, and increasing the total number of transistors in one IC chip. According to Moore's law – the number of transistors on one IC chip has quadrupled every three years and the feature size of each transistor has shrunk to half of its original value at the same time. Currently the gate length is about 35 nm, and will continue to be reduced in future generations. In fact, it is quite likely that the gate length will approach 10 nm before the end of this decade [7]. With such a small channel length, it is then assumed that ballistic transport should be the dominant method of transport [7]. However, recent experiments have recommended that the ballistic length in silicon might be less than the assumed 10 nm [7].

For maintaining the successive improvements in Integrator circuit device technology, non-stop achievement in device scaling is required. As the MOSFET gate length enters the nanometer range, however, short channel effects (SCEs), such as threshold voltage (V_T) roll off and drain-induced-barrier-lowering (DIBL), become more and more important, which limits the scaling ability of *planar* bulk or silicon-on-insulator (SOI) MOSFETs [7]. At the same time, the relatively low carrier mobility in silicon (compared with other semiconductors) may also degrade the MOSFET device performance. For these reasons, various novel device structures and materials – silicon nanowire transistors, carbon nanotube FETs, new channel materials (e.g., strained silicon, pure germanium), and molecular transistors and others. – are being extensively explored [7]. Among all these promising post-CMOS structures, the silicon nanowire transistor (SNWT) has its unique advantage – the SNWT is based on silicon, a material that the semiconductor industry has been working on for over thirty years; it would be really attractive to stay on silicon and also achieve good device metrics that nano electronics provides. As a result, the silicon nanowire transistor (SNWT) has obtained broad concentration from both the semiconductor industry and academia. SNWTs can be categorized into two groups according to the fabrication technology which are discussed below.

1) The first-type Silicon nano wire transistors can be viewed as 'narrow-channel' silicon-on-insulator MOSFETs realized by using a 'top-down' approach. Different from planar SOI FETs, the channel (Si body) widths of SNWTs are lithography-defined and comparable to

the Si body thicknesses, so the gate stacks are allowed to wrap around the wire channels to realize multi-gate or gate-all-around FETs, which offer better gate control than planar MOSFETs [7]. In current experimental SNWT structures, the wire dimensions (i.e., Si body thickness and width) range from 10nm to 100nm. At the scaling limit, where the device gate length is probably shorter than 10nm, this dimension has to be scaled down to the sub-10nm regime to maintain good electrostatic integrity [7]. To do this, very-high resolution lithography (e.g., <5nm) is required to define the nanowire widths. Therefore, the ultimate scaling of the top-down SNWTs could be limited by the highest resolution of lithography that can be achieved in practice [7]. It should also be noted that the minimum lithography-defined length in the circuits based on the top-down SNWTs should be the SNWT channel (Si body) width instead of the transistor gate length.

2) To avoid very-high-resolution lithography in the SNWT fabrication, a number of experimental groups are trying to synthesize semiconductor (e.g., Si, Ge, GaN) nanowires by using 'bottom-up' approaches, such as the Vapour-Liquid-Solid (VLS) growth technique [7]. With this technology, single-crystal Si nanowires with a diameter as small as 2-3nm have been achieved [7]. Based on these bottom-up nanowires, various types of devices and circuit components have been experimentally demonstrated, e.g., field-effect transistors (FETs), nanowire hetero junctions, logic gates, memory, decoders, bipolar transistors , thin-film transistors , light emitting diodes (LEDs) , lasers, photo detectors, and nano sensors. For the FET application, in particular, the bottom-up technique offers a possible, low-cost solution to achieve nanowires with ultra-small diameters and relatively smooth interfaces, which are essentially important for scaling the transistor gate length below 10nm[7].

2. Theory

2.1.BALLISTIC CURRENT

The transport in most of the nanostructures such as carbon nanotubes, silicon nanowires is ballistic. The ballistic current has both the tunneling and the thermionic components. Here an analytical model is derived for the I-V characteristics of nano devices under single sub band approximation. The current is thermionic only in the derivation. The Landaur equation for ballistic current is

$$I = \frac{2e}{h}\int_{E_c - e\phi_s}^{\infty} dE T(E)[f(E-\mu_s) - f(E-\mu_D)]$$

Here e is the electronic charge, h is Planck's constant, $T(E)$ is the transmission coefficient, f is the Fermi distribution function, μ_S and μ_D are the source and drain Fermi levels, respectively, and the factor of 2 accounts for spin degeneracy. The integration is performed from the bottom of conduction band to infinity for electron current. The conduction band bottom without gate bias is E_C and ϕ_S is the surface potential. For thermionic emission current $T(E) = 1$, and the current becomes

$$I = \frac{2e}{h}\int_{E_c - e\phi_s}^{\infty} dE\left[\frac{1}{1+e^{(E-\mu_S)/KT}} - \frac{1}{1+e^{(E-\mu_D)/KT}}\right]$$

Now integration of $\int \frac{dE}{1+e^{(E-\mu_S)/KT}}$ becomes $-KT\ln\left(1+e^{\frac{E-\mu_S}{KT}}\right)$. Therefore, the current expression becomes

$$I = \frac{-2eKT}{h}\left\{\left[ln\left(1+e^{(\mu_S - E)/KT}\right)\right]_{E_c - e\phi_s}^{\infty} - \left[ln\left(1+e^{(\mu_D - E)/KT}\right)\right]_{E_c - e\phi_s}^{\infty}\right\}$$

Now putting values in the above expression, we get the current as the following

$$I = \frac{2eKT}{h}\left[ln\left(1+e^{(\mu_S + e\phi_s - E_c)/KT}\right)\right] - \left[ln\left(1+e^{(\mu_D + e\phi_s - E_c)/KT}\right)\right]$$

The first term in the expression of current is the forward term that dominates in the saturation and the second term is the backward term that dominates in the linear region.

2.2.SURFACE POTENTIAL

In the derivation of current, we have a quantity ϕ_S called surface potential. So we will try to find an expression for the surface potential here. The current expression is derived assuming a single point as the channel, where the potential barrier along the source to drain is highest, and the transmission coefficient is unity above it and zero below it. This point of the channel is electrostatically connected to the gate, to the source, and to the drain that can be schematically represented as shown below.

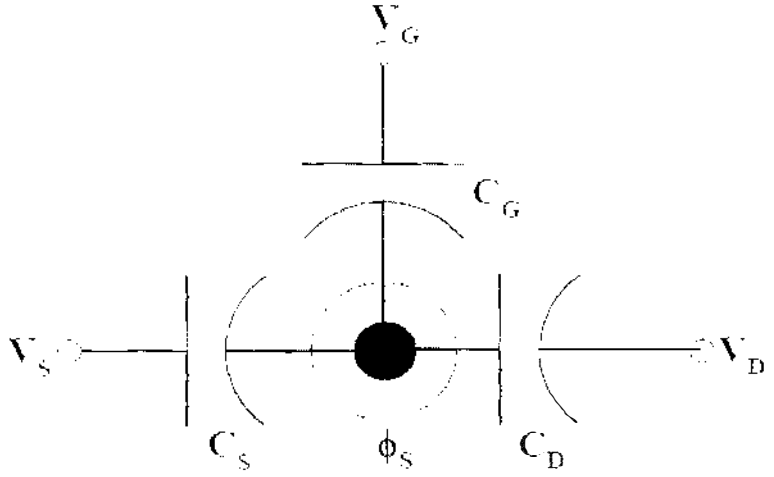

Figure 2.2.1 : Electrostatic representation of channel

Now the excess charge above equilibrium at that channel point would be the balanced by the charge associated with the three capacitors as follows

$$e(N-N_0) = c_G(V_G - \phi_S) + c_S(-\phi_S) + c_D(V_D - \phi_S)$$

$$e(N-N_0) = C_G V_G + c_S V_S + c_D V_D - \phi_S(c_G + c_S + c_D)$$

Now rearranging the terms and defining gate control parameter as $\alpha_g = C_G/C_T$, source control parameter as α_s C_S/C_T, and drain control parameter as $\alpha_d = C_D/C_T$ we get equation of surface potential $\phi_S = \alpha_g V_G + \alpha_s V_S + \alpha_d V_D - \frac{e(N-N_0)}{C_T}$.

Here $C_T = C_G + C_S + C_D$ is the total capacitance. The term $e(N-N_0)/C_T$ is related to the quantum capacitance. To calculate the surface potential ϕ_S , we need to know N the total number of electron (not electron density) at the channel ($N_0 = N$ at equilibrium i.e. ϕ_S 0). The total number of electron can be obtained by integrating the DOS function times the

quasi Fermi function in energy. However, we do not know the quasi Fermi function in the channel; rather we know the two Fermi levels, μ_s and μ_D. How the channel states are populated by the carriers according to these two Fermi levels are shown in the following figure

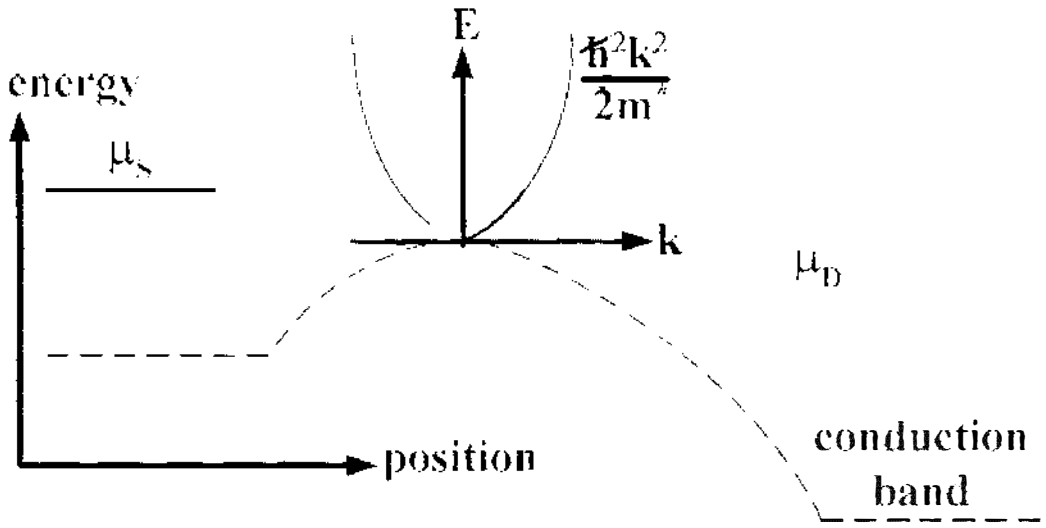

Figure 2.2.2 : : Band profile and carrier population

The electrons that are injected from the left (source) contact have positive velocity. Therefore, the right half (positive k) of E-k relation will be filled up by the carriers injected from the source. Similarly the left moving electrons will fill up the negative k states according to the drain Fermi level. Therefore half of the channel DOS will be associated with the source and the other half with the drain (E-k is symmetric). However, at equilibrium, the two Fermi levels are equal (E_f) and N_0 can be obtained from the following equation.

$$N_0 = L \int_{E_C}^{\infty} \left(\frac{1}{\pi\hbar} \sqrt{\frac{2m^*}{E - E_c}} \right) f(E - E_f) dE$$

Note that the expression contains the channel length L because we are calculating the total number of electrons not the density. Now the positive moving electrons N^+ and the negative moving electrons N^- can separately be calculated according to the following equations and $N = N^+ + N^-$.

$$N^{+} = L\int_{U_{scf}}^{\infty}\left(\frac{1}{2\pi\hbar}\sqrt{\frac{2m^{*}}{E-U_{scf}}}\right)f(E-\mu_{s})dE$$

$$N^{-} = L\int_{U_{scf}}^{\infty}\left(\frac{1}{2\pi\hbar}\sqrt{\frac{2m^{*}}{E-U_{scf}}}\right)f(E-\mu_{d})dE$$

Here we use $Uscf = E_C\text{-}e\phi_s$. Once the parameters (α's) are set up, we have to obtain the surface potential by self-consistently solving N and ϕ_s. However, for zero temperature, (T = 0^0K), the Fermi distribution has the value of unity up to Fermi level and zero beyond it. Therefore, the upper limit of the carrier expression will be the corresponding Fermi level and their analytical expressions can be obtained as shown in the following equation

$$N_0 = \frac{2L}{\pi\hbar}\sqrt{2m^{*}(E_f-E_c)}\ominus(E_f-E_c)$$

$$N^{+} = \frac{L}{\pi\hbar}\sqrt{2m^{*}(\mu_s-U_{scf})}\ominus(\mu_s-U_{scf})$$

$$N^{-} = \frac{L}{\pi\hbar}\sqrt{2m^{*}(\mu_D-U_{scf})}\ominus(\mu_D-U_{scf})$$

Here $\ominus(x)$ is the unit step function that has a value of 1 for x $\geq$0 and 0 otherwise, E_f is the equilibrium Fermi energy, and E_C is the bottom of conduction band at equilibrium. When $U_{scf} > E_f$ (orμ_s) almost zero current flows. The current starts to flow when V_G increases so that $V_G = V_T = -E_f/e$. That is, the threshold voltage is the gate voltage at which the bottom of conduction band (U_{scf}) levels (becomes equal) with the source Fermi level. In case of the intrinsic silicon nanowire transistors that we have used above (operate in the quantum capacitance limit) the threshold voltage is simply equal to the half of the band gap $V_T = Eg/2e$.

3. Result

3.1. Transfer characteristics

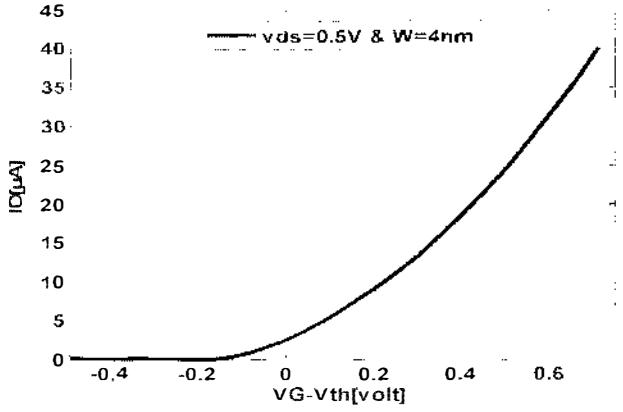

Figure 3.1.1: I_D versus overdrive (V_G-V_{th}) voltage, where w=4 nm & drain to source bias vds =0.5V

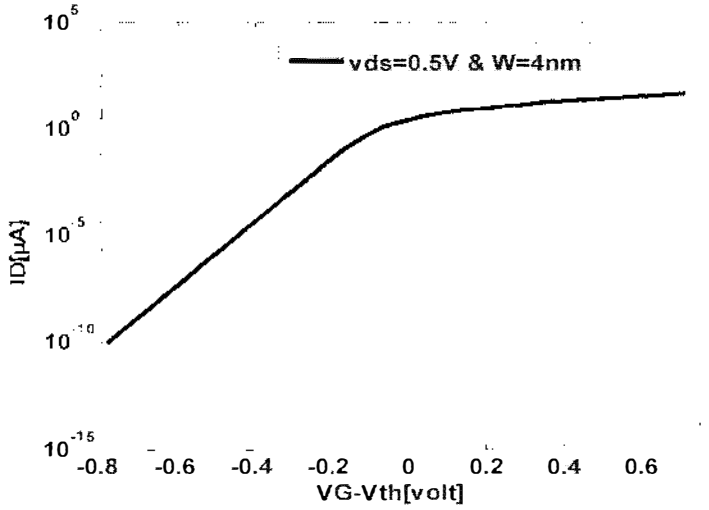

Figure 3.1.2: log I_D versus overdrive voltage (V_G-V_{th}), where w=4 nm & drain to source bias voltage vds =0.5 V

Figure 3.1.1 and figure 3.1.2 shown above is the transfer characteristics of silicon nanowire MOSFET. From linear plot we see that if the gate voltage is less than the threshold voltage, the MOSFET operates in cut off mode and the drain current is almost zero and MOSFET is OFF. If the gate voltage is greater than the threshold voltage the current increases exponentially.

3.2. Output characteristics

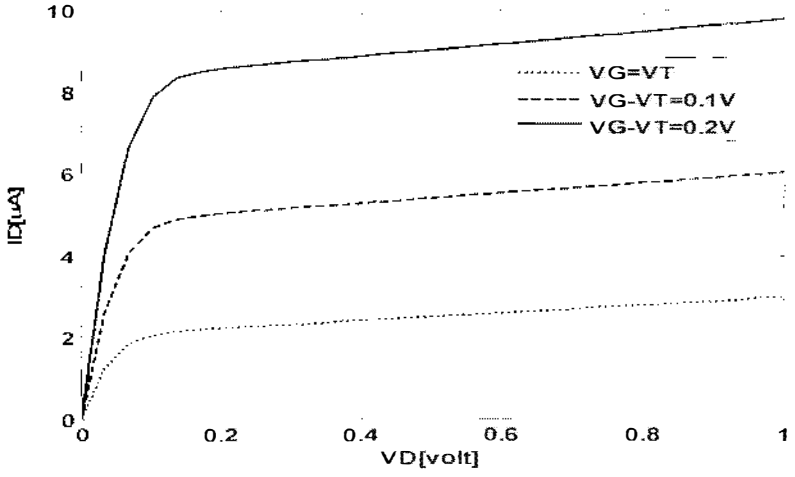

Figure 3.2: I_D versus V_D, where w=4 nm & $V_G = V_T$, V_T+0.1, V_T+0.2

Figure 3.2 shows the output characteristic of silicon nanowire MOSFET. From this figure we see that if we increase the gate bias the drain current is increased. For low drain bias current increases linearly. In this figure we draw three ID versus VD curves for overdrive voltage 0, 0.1and 0.2 V

3.3. Capacitance, cutoff frequency, transconductance, switching delay, charge at barrier top and energy of barrier top.

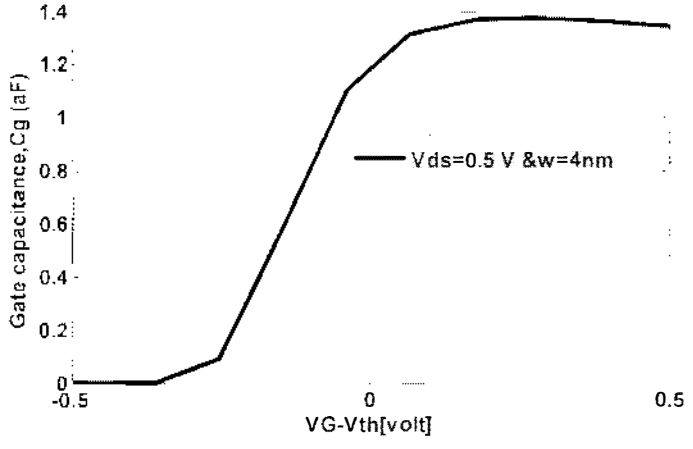

Figure 3.3.1: Cg versus overdrive voltage (V_G-V_{th}), where drain to source bias is 0.5V

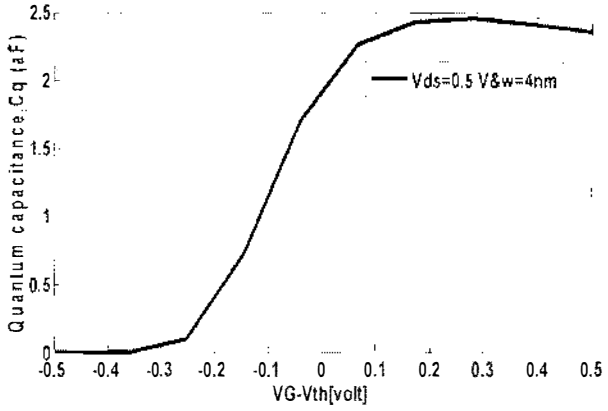

Figure 3.3.2: Cq versus overdrive voltage (V_G-V_{th}), where drain to source bias is 0.5V

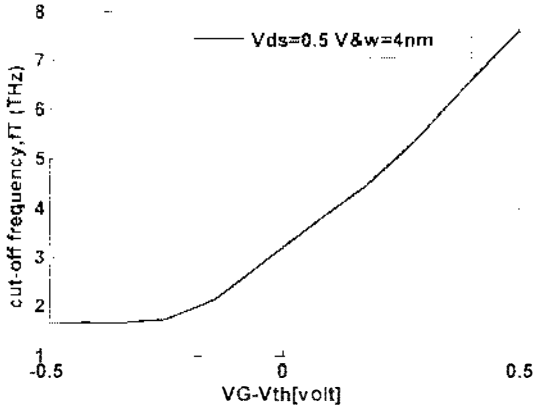

Figure 3.3.3: f_T versus overdrive voltage (V_G-V_{th}), where drain to source bias is 0.5V

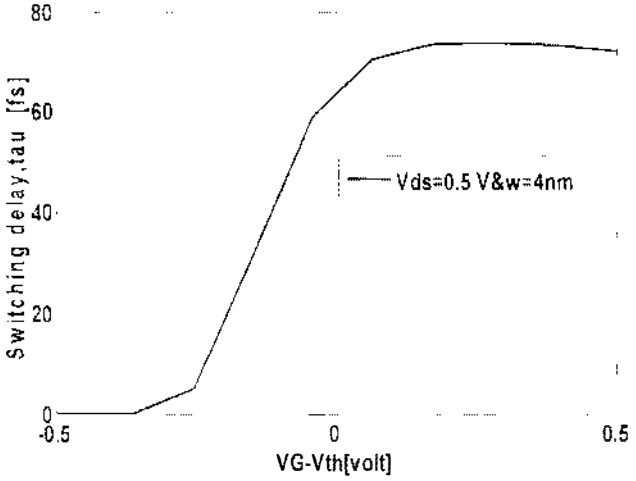

Figure 3.3.4: τ versus overdrive voltage (V_G-V_{th}), where drain to source bias is 0.5V

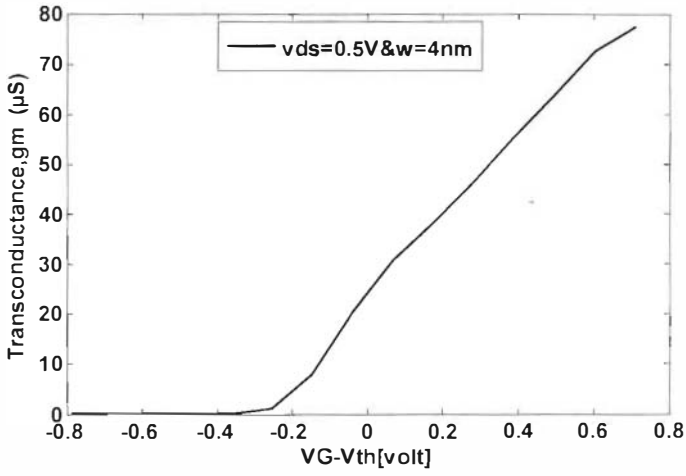

Figure 3.3.5: g_m versus overdrive voltage (V_G-V_{th}), where drain to source bias is 0.5V

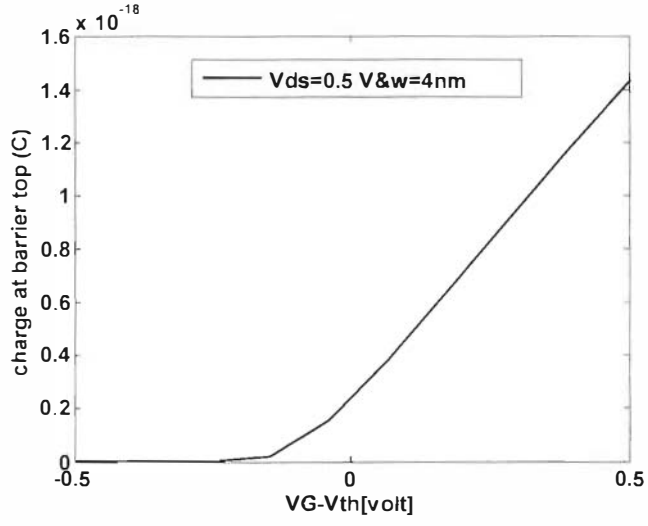

Figure 3.3.6: Q_{top} versus overdrive voltage (V_G-V_{th}), where drain to source bias is 0.5V

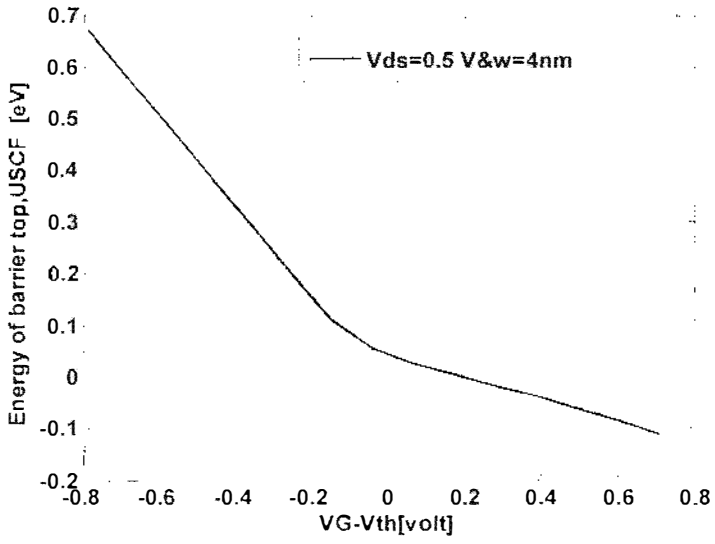

Figure 3.3.7: Energy of barrier top(USCF) versus overdrive voltage (V_G -V_{th}), where drain to source bias voltage is 0.5V and width is 4 nm

From figure 3.3.1 to figure 3.3.7 are shown the gate capacitance, quantum capacitance, cut off frequency, switching delay, transconductance, U_{scf} and Q_{top} versus overdrive voltage. The gate capacitance is calculated from $C_G = (C_{ox}*C_Q)/(C_{ox}+C_Q)$ where Cox is oxide capacitance and C_Q is quantum capacitance. The oxide capacitance for cylindrical structure is obtained from $C_{ox}= (2\pi\varepsilon L)/ \log (1+2*t_{ox}/w)$ and the quantum capacitance is calculated from $d(Qtop)/dVG$ at fixed V_{DS}. The gate capacitance C_G peaks at a gate bias of V_{th}+0.2 V where V_{th} is the threshold voltage for width 4 nm and then it decrease. When overdrive voltage is less than -0.2V, there is no charge in gate so the gate capacitance is zero. Over drive voltage from -0.2V to 0V the gate capacitance increase linearly. From Vth to V_{th}+0.2 it increases exponentially. Cut of frequency is calculated from $f_T = g_m/2\pi C_g$, the transconductance is obtained from $g_m= dI_D/dVg$ the switching delay is calculated from $\tau = (Cg * VDD)/Ion$ where Ion is the on current. The on current is the drain current at $V_{GS}=V_{TH}$+0.2 V and V_{DS} = 0.5 V. Quantum capacitance (C_q), cut off frequency (f_T), switching delay (τ) and transconductance peak at V_{th}+0.2V like gate capacitance (Cg).From figure3.3.6 we see that there is no charge at top of the barrier at the region where overdrive voltage less than -0.2V.After the threshold voltage it increases linearly. From figure3.3.7 we observed that if we increase the gate bias then the energy of the barrier top decreases linearly and after the threshold voltage it goes to negative value. In our study we see that for 4 nm width threshold voltage is 0.7845V.

3.4. Effects of wire width on device performance

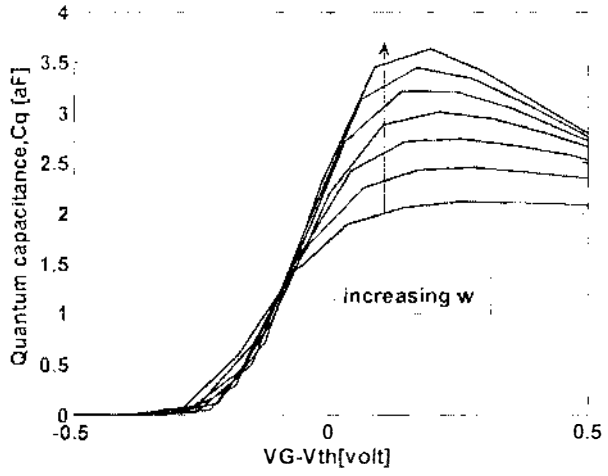

Figure 3.4.1: Cq versus overdrive voltage (V_G-V_{th}), where w varies from 3 to 9, drain to source bias voltage 0.5V

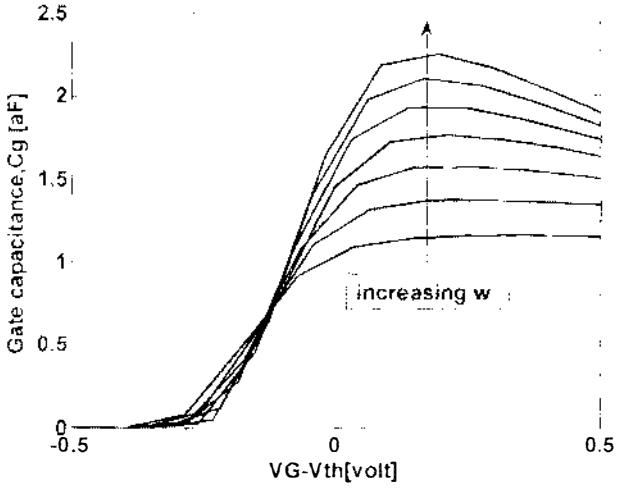

Figure 3.4.2: Cg versus overdrive voltage (V_G-V_{th}), where w varies from 3 to 9, drain to source bias voltage 0.5V

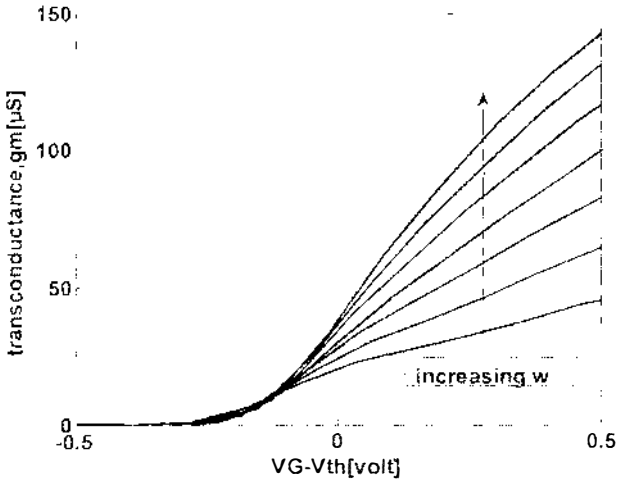

Figure 3.4.3: g_m versus overdrive voltage (V_G-V_{th}), where w varies from 3 to 9, drain to source bias voltage 0.5V

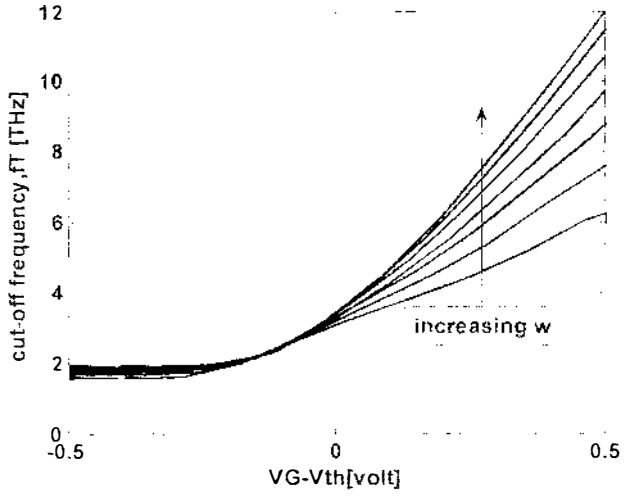

Figure 3.4.4: f_T versus overdrive voltage (V_G-V_{th}), where w varies from 3 to 9, drain to source bias voltage 0.5V

From figure 3.4.1 to 3.4.4 are shown the characteristics of gate capacitance, Quantum capacitance, threshold voltage, cutoff frequency and transconductance versus overdrive voltage for different wire width. From the figure we see that if we increase width then gate capacitance, Quantum capacitance, cutoff frequency and transconductance increase. According to the equation of band gap Eg = A_eg + B_eg/width_nw, where width_nw is the width of the silicon nano-wire MOSFET we see that if the width is increased then band gap is reduced so current is increased. The gate capacitance, quantum capacitance, cutoff frequency and transconductance also increase with wire width.

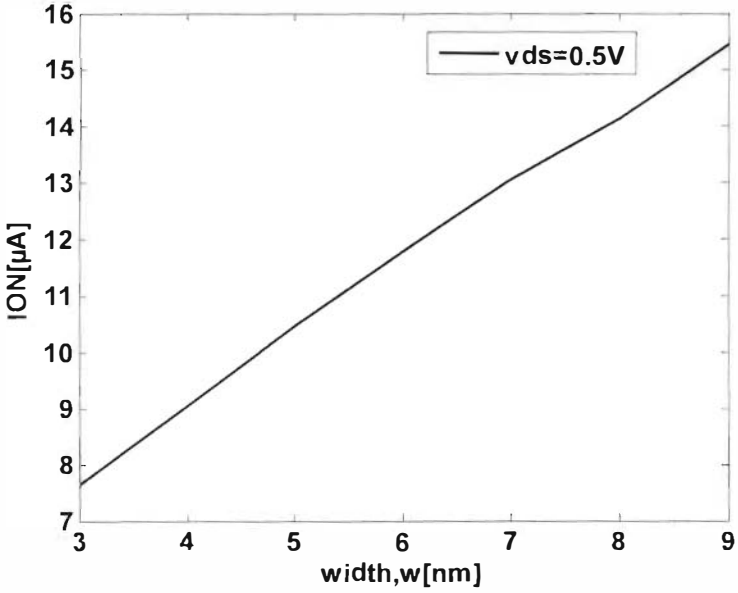

Figure 3.4.5: I_{on} versus width, drain to source bias 0.5V

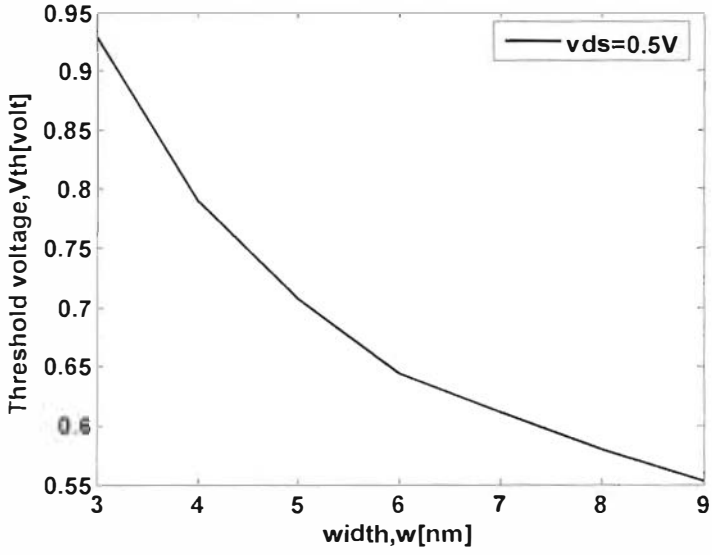

Figure 3.4.6: V_{th} versus width, drain to source bias 0.5V

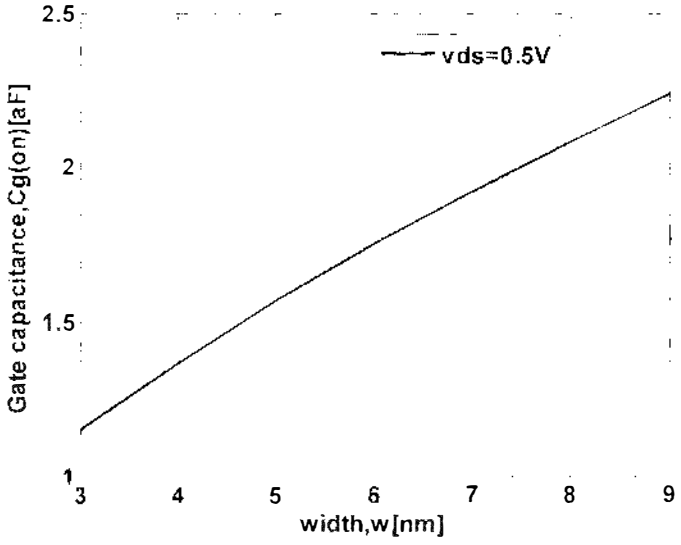

Figure 3.4.7: C_g versus width, drain to source bias 0.5V

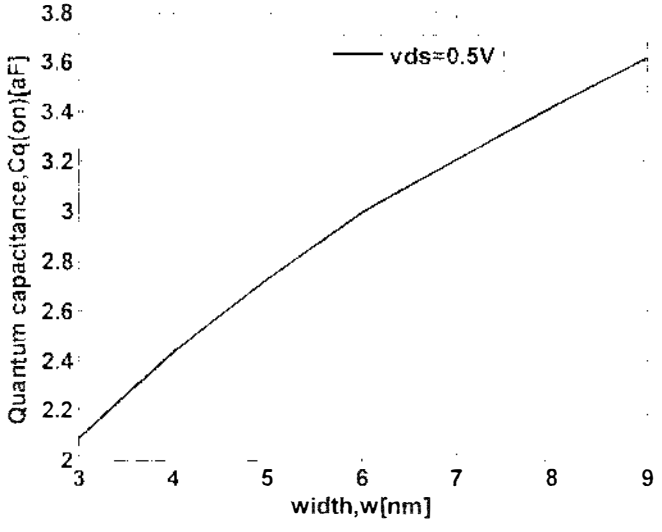

Figure 3.4.8: C_q versus width, drain to source bias 0.5V

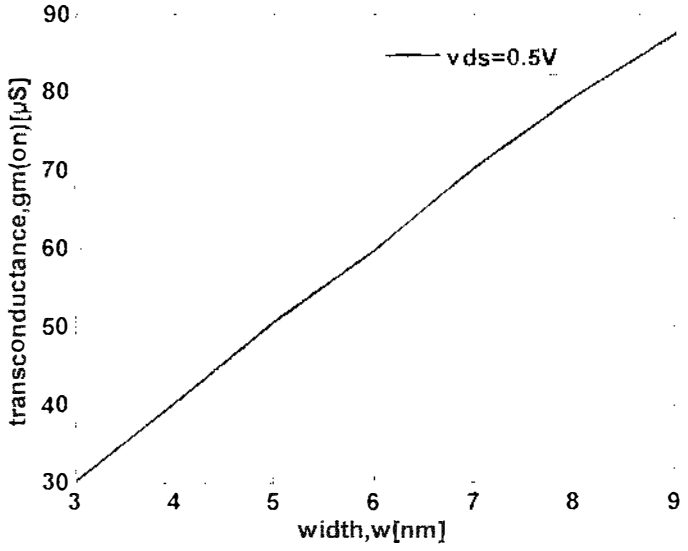

Figure 3.4.9: g_m versus width, drain to source bias 0.5V

From figure3.4.5 to figure3.4.9 are the on state current (Ion), Gate capacitance (C_g on), Quantum capacitance (C_q_on) and transconductance (g_m_on) versus wire width. The on-state values are defined at a gate bias of V_{GT}=0.2 V and V_{DS} =0.5 V. From the Characteristics we see that if we increase the width then band gap is decreased so the threshold voltage decreases. Gate capacitance (C_g on), Quantum capacitance (C_q_on) and transconductance (g_m_on) also increase wire width.

4. Conclusion

We have studied the I-V characteristics, threshold voltage, quantum and gate capacitance, transconductance, charge at barrier top, cutoff frequency, on current and energy of barrier top of silicon nanowire MOSFETs. For different width we observed these characteristics also. We see that if we increase width band gap is decreased and current increases. The quantum and gate capacitance, transconductance, charge at barrier top and cutoff frequency also increase with wire width. We also observed these characteristics at on-state.

5. References

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