Effects of Reduced Dimensionality on the Performance of Nano – Transistors

By

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Abstract

In this thesis we have represented the performance analysis of different types of nano-transistors such as single gate bulk MOSFET, double gate MOSFET, nanowire FET and CNTFET. Our observation is based on the ballistic transport at the top of the barrier model. The scattering effects on the current transport through the MOSFET are neglected in our observation.
FETToy simulation tool was used to calculate the On – Current (I_{on}) and transconductance (g_m) of different types of nano-transistors. We consider the change of insulator thickness (t_{ox}) and initial source Fermi level (E_F). Comparative discussion about the effects on I_{on} and g_m in terms of changing MOS parameters are studied in this thesis.

We observe that, the performance of nano-transistors improve with the switching of SG MOSFET to DG MOSFET, DG MOSFET to Si nanowire FET, Si nanowire FET to CNTFET. CNTFET has better On-Current (I_{on}) and transconductance (g_m) over the other devices. On the other hand FETToy cannot properly model Subthreshold Swing (S) and Drain Induced Barrier Lowering (DIBL) in the top of the barrier model.

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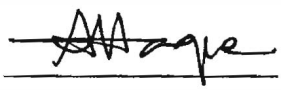
However, thoroughly expressing our thankfulness to our supervisor is simply beyond our ability to express in words.

Moreover, we apologize for any grammatical or spelling errors in our writing, if any.

Approval

The thesis titled "**Effects of Reduced Dimensionality on the Performance of Nano – Transistors**" submitted by Remon Ahmed (2006-2-80-045), Ahmed-Al-Nahid (2006-1-80-005), Md. Jahurul Islam (2006-2-80-044), session summer 2010, has been accepted satisfactory in partial fulfillment of the requirement of the degree of Bachelor of Science in Electrical and Electronic Engineering on August, 2010.

Supervisor



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1. INTRODUCTION

The MOSFET (metal-oxide-semiconductor field-effect transistor) size needs to be scaled down to fulfill the current demand of rising technological and informational improvement. These demands are related to high capacity performance, high speed capability in high degree of integration and low-power consumption [1]. MOSFET device technology has been leading very large scale integrated (VLSI) technology over the past forty years [2]. This technology is continuously changing with its features and up-dated versions of these transistors. In the latest types of transistors, steady improvements of cost, speed and power consumption is very much significant [3].

According to the Gordon Moore's empirical observation of 1965, the number of transistors in a chip doubles in every 18 months. The more the line width is reduced, the more the improvement of the design is observed. The technology generation is 180 nm, 130 nm, 90 nm, 65 nm and 45 nm generations and it does continue to shrink more. This reduction-process of the previous size is known as "scaling". The latest technology of integrated-circuit speed increased roughly around 30% [3].

Scaling of CMOS devices will eventually reach fundamental limits. It appears that the CMOS process will reach its fundamental limit in the near future, and quantum mechanical effects will be required to be considered. As device size decreases, gate leakage current rapidly increases due to direct tunneling. To overcome a number of issues associated with the continued MOSFET scaling, the updated material device concepts and alternative process techniques are important.

Device behavior and performance at the ballistic limits, has become more and more interesting as the channel length of the integrated circuit transistor continue to shrink towards 10 nm regime. In the ballistic or quasi-ballistic regimes, the conventional device equations based on drift diffusion theory are not appropriate, thus a new theory of ballistic transistor is required.

1.1. Background

In the year 1948, John Bardeen and Walter Brittain first invented the three-terminal transistor (i.e, the bipolar junction transistor). The solid state electronics has hugely increased over the last four decades [4]. MOSFET devices are attractive due to their simplicity. The MOSFET was first reported by D. Kahng and M.M Atalla in 1960 [5]. In 1965 Gordon Moore established the law which is known as Moore's law and geometric scaling followed by the law. The MOS technologies rapidly shrank in order to meet its increased performance level and reduced power usage.

In 1974, Dennard first introduced constant field scaling, which is called Dennard's scaling methodology. Initially, electric field across the gate dielectric remained constant because of dielectric thickness and operating voltage which were to be scaled at the same rate [6]. There are two types of limitations in constant field scaling, they are; subthreshold nanoscaling and power supply voltage. Constant voltage scaling will result in an extremely high electric field. It causes unacceptable leakage current, power consumption and also degrades the oxide integrity. On the other hand, geometric scaling is perfect for short channel effect.

1.2. Literature Review

During the last couple of years, there have been several technology improvements in the field of MOS technology. These improvements have maintained device characteristics without introducing entirely new material systems within the gate stack [4].

Conventional CMOS fabrication processes have supported many generations of shrinking in size. High-k gate dielectric has already been introduced in the 45 nm node by Intel. High-k stands for high dielectric constant. Actually, this is a kind of measurement of how much charge a material can hold. Different materials have different abilities to hold charge [7].

Semiconductor manufacturers have been investigating alternative transistor architectures such as DG (double-gate) MOSFET, SOI (Silicon on Insulator) technology, Si nanowire FET, CNTFET and Tri-gate technology. The main problem is in the manufacture of the processes. The CMOS technology will soon have a lower rate of performance increase as their size is reduced [8].

In near future SOI is also used for FinFET and other multi-gate MOSFET devices. All these device improvements have fallen behind by the introduction of high – k / metal gate stacks [4]. In SOI fabrication technology transistors are built on a silicon layer resting on an insulating layer of Silicon dioxide (SiO_2). The main advantage of SOI includes higher performance at equivalent V_{DD}, reduction of the temperature sensitivity and power savings [9].

DG MOSFET is comprised of a conducting channel surrounded by gate electrodes on either side. Its design objective is to reduce the short channel effect, maintaining good electrical characteristics and keeping the fabrication process simple. Double gate allows higher current drive capability and better control of short channel effects. This can also reduce the I_{off} current [10].

A tri-gate bulk MOSFET is designed to combine traditional channel doping with a multi-gate structure. This is proposed to provide an evolutionary pathway for bulk CMOS scaling. The tri-gate bulk MOSFET provides superior electrostatic integrity and reduced variability. As compared with SOI FINFET design, the tri-gate bulk MOSFET design is more scalable and less sensitive to device design parameters. Compared with the bulk FINFET design, the tri-gate bulk MOSFET offers comparable performance and variability. For that reason, the tri-gate bulk MOSFET is a promising structure for CMOS scaling at the end of the technology roadmap [11].

The silicon nanowire transistor (SNWT) has grabbed wide attention for its full three-dimensional cross-sections. The ballistic SNWT theory based on the effective-mass approximation has evaluated the upper performance limits of SNWTs with various dimensions such as, triangular, rectangular and cylindrical. Most SNW FETs use metals as source and drain and it operates in accumulation mode. Silicide formation is one of the most effective ways to control and improve the connections in silicon nanowires [12].

The CNTFET (carbon nanotube field effect transistor) can provide better transistor performance compared to normal MOSFET technology. This can be used in the semiconducting carbon nanotube as the channel. The physical structure of CNTFETs is very similar to that of MOSFETs. Their I-V characteristics and transfer characteristics are also supportive in the case of

replacement of the MOSFETs, in nanoscale electronics. The characteristic of the carbon nanotube that reduces scattering probability conducts on the surface (where all the chemical bonds form interface states); which makes CNTFET more promising as the usage in the future [13].

1.3. Objective

Our main purpose of this thesis is to study the comparison of different types of MOSFET structures. We compare the performance of different types of MOSFETs such as, single gate MOSFET, double gate MOSFET, Si nanowire FET and CNTFET. The semi-classic ballistic transport at the top of the barrier model was used for performance evalution. The effects of changing device parameters such as, insulator thickness (t_{ox}) and initial source Fermi level (E_F) are the main focus of this report. We used the FETToy simulation tool for calculation. In our study, we have discussed about the effects of changing the oxide thickness (t_{si}) and initial source Fermi level (E_f) on on-current (I_{on}) and transconductance (g_m).

1.4. Organization of the Thesis

In chapter 2, necessary review of MOSFET scaling, reason behind scaling and scaling trends of MOSFETs is given. In the chapter 3, there is a discussion of ballistic MOSFET and current-voltage characteristics of the ballistic MOSFET. In chapter 4, we observed the performance of different kinds of parameters in different types of devices associated with the ballistic MOSFET. Summary and future work is presented in the conclusion which is mentioned in chapter 5. Technology trends of the transistor are given in the appendix section.

2. DEVICE SCALING

2.1. MOSFET Scaling

The MOSFET devices have been the backbone of today's Semiconductor industry, since it was invented. For the past four decades, the expansion of IC industry is largely driven by the technology of MOSFET transistor minimization, which is called MOSFET down scaling [14].

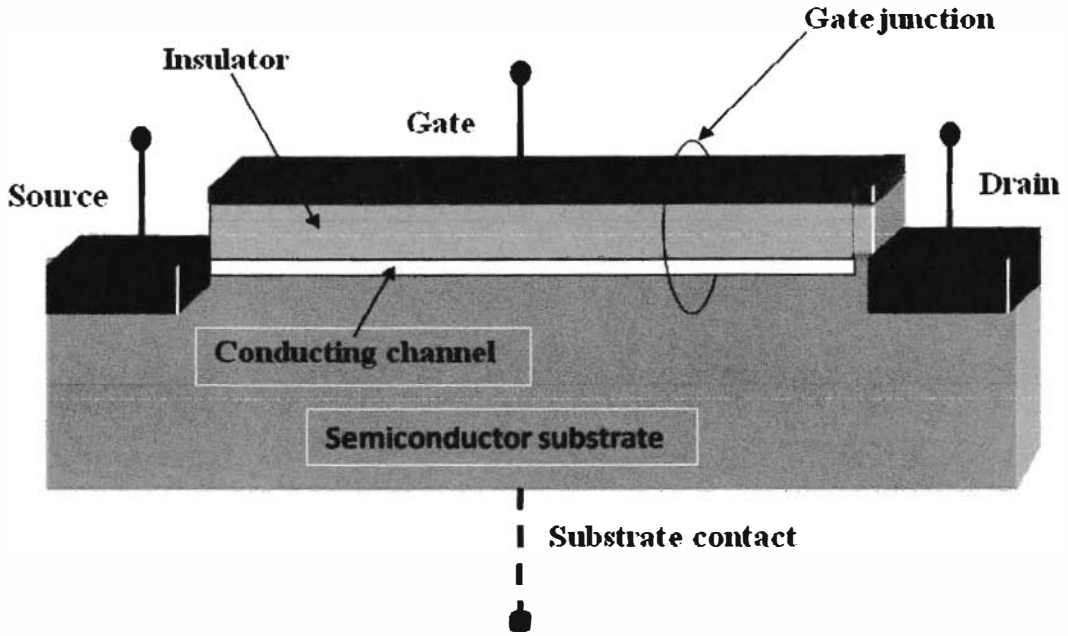

Figure 2.1 : Structure of MOSFET

Figure 2.1 shows the basic structure of a general MOSFET. The basic principle of MOSFET scaling, lies in scaling the device voltages and device dimensions (both horizontal and vertical), by the same factor so that the electric field remains unchanged. This assures that, the performance of the scaled-device is better than that of the original device [8]. A proper scaling of MOSFET requires not only reduction of gate length and width, but also needs the reduction of other device parameters such as gate oxide thickness, doping density and junction depth [14].

2.1.1. Reasons Behind MOSFET Scaling

Scaled-MOSFETs are desirable for a few main reasons. They allow more current to pass, when the MOSFET is in the on-state, it displays a resistive behavior between the drain and source terminals. In addition, scaled-MOSFETs have lower gate capacitance and the amount of charge on a gate is proportional to its capacitance (e.g. $Q_g = C_g V$). That is why, logic gates include scaled MOSFETs having less charge to move. These two factors contribute to lower switching times, and thus support higher operating speeds [8].

Another important reason behind MOSFET scaling is the reduction of area, which leads to the cost reduction. Due to scaling, the scaled MOSFETs can be packed more closely. This results in either smaller chips or chips with more computing power in the same area [15]. The cost of fabricating a semiconductor wafer is relatively fixed. So, the cost of producing integrated circuits is mainly related to the number of chips that can be produced per wafer. Hence, smaller integrated circuits allow more chips per wafer, reducing the price per chip [2]. In 1954, the average price of a transistor cost $5.52. In 2004, the average cost of one transistor was 191 nano-dollars [15].

2.1.2. MOORE'S Law

In 1965 Gordon Moore, co-founder of Intel, described a long-term trend in the history of computing hardware, which supposes to continue until 2015 or later [15]. His prediction was that, "the number of transistors per square inch on integrated circuits will be doubled in every upcoming year". He slightly changed the formulation of the law over time, for increasing the perceived accuracy of his law. Most remarkably, in 1975, Moore changed his projection to a doubling of "every two years". There is a popular misconception that, he also predicted a doubling of "every 18 months". But the latter case was predicted by David House, an Intel colleague of Gordon Moore [16]. Many sources today, refer the 18 months period.

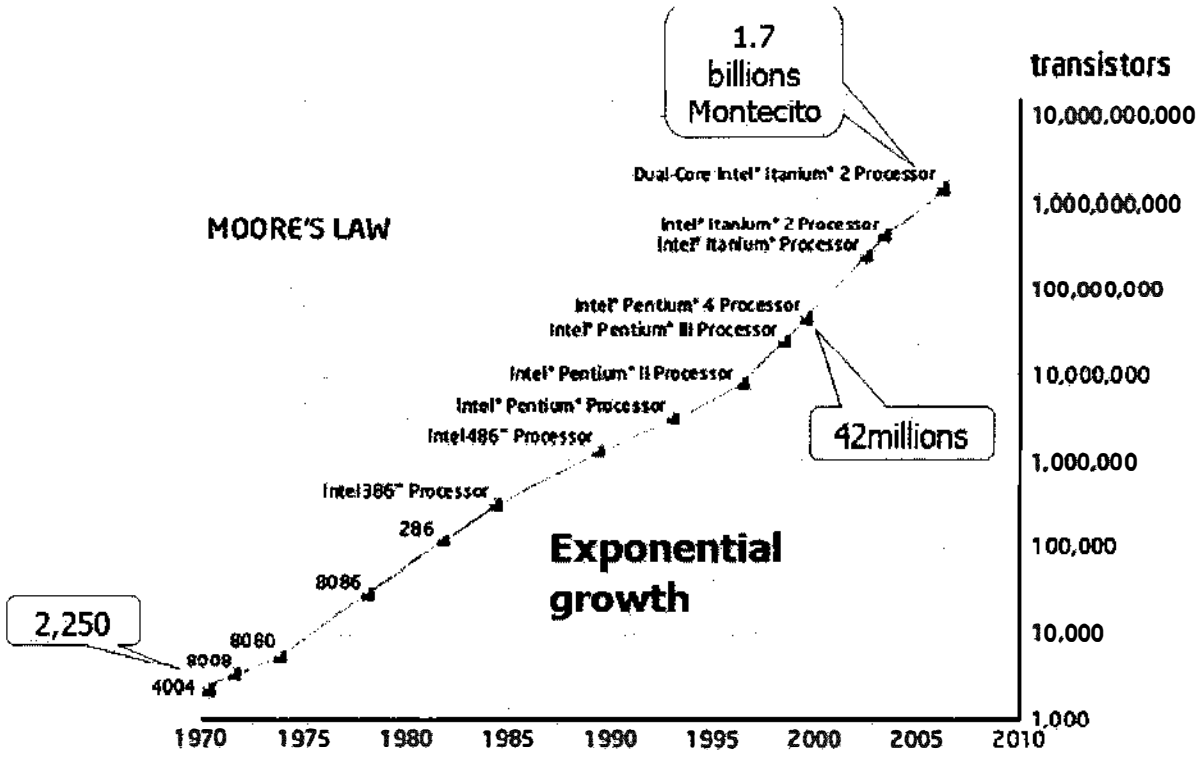

Figure 2.2: CPU transistor counts 1971-2006 and Moore's Law [17]

Fig. 2.2 shows the plot of transistor counts against dates of introduction. The curve shows the exponential growth of transistor number per processor and it seems that the number became doubled in every 18 months. In 1971 Intel first introduced Intel 4004 processor with 2,300 transistors, and recently in 2010 Intel introduced its latest processor 8-Core Xeon Nehalem-EX with 2,300,000,000 transistors. These numbers indicate the historical evolution in the MOSFET-scaling. Many things have been changed, but the trend which Mr. Moore predicted, is still the strongest ideology in IC fabrication.

2.1.2.1. Geometrical (Constant Field) Scaling

Geometrical scaling process is used in conventional CMOS, which refers to the nonstop reduction of physical feature sizes (e.g. horizontal and vertical), in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications [1]. The main function of this scaling is to reduce "design factors" (e.g. L, W and T_{ox}), followed by the basic principle of Moore's law.

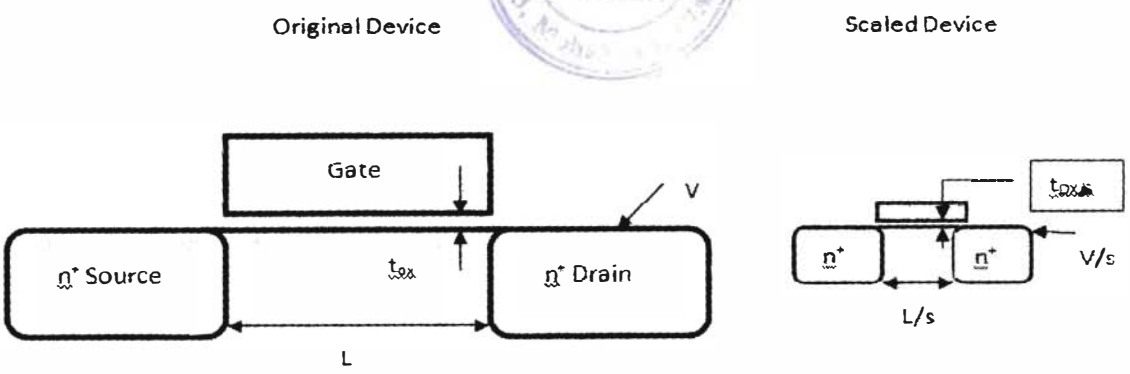

Figure 2.3 : MOSFET Constant Field Scaling

Figure 2.4 shows the original device along with the scaled device. Here the device is scaled by the dimensional scaling factor "S" and S is greater than 1 (e.g. S > 1). Thus, the scaled channel length, width and t_{ox} will become – L/S, W/S, t_{ox}/S.

2.1.2.2. Equivalent Scaling

Equivalent Scaling is the predominant scaling technology for conventional CMOS devices. This scaling process is the conjunction progress of continued geometrical scaling for 3-dimensional device structure ("Design Factor"). This improvement, plus other non-geometrical process techniques and new materials, affect the electrical performance of the chip [6]. Here, the non-geometrical process means, "Voltage Scaling". Potentials (V_{DS}, V_{GS}) are scaled by the supply voltage scaling factor "K". If the electric field is changed by the scaling then there will be dielectric breakdown, because of high electric field. That's why both "S" and "K" must be same, so that the electric field remains unchanged [18].

Figure 2.4 also represents the equivalently scaled device and Figure 2.3 is representing the MOSFET Scaling trends in terms of equivalent scaling.

2.1.3. More than MOORE'S Law

More than Moore's law focuses on system integration rather than transistor density. This trend has already begun from 2008. This already includes the new concept about the MOSFET scaling as "beyond CMOS". The rapid reduction of the dimensions of the chip, (e.g. constant field scaling) does not contain the pace of MOSFET scaling, (for example, MOSFET channel lengths

below 9 nm) trends which was predicted by Gordon Moore. In beyond CMOS, Scaling of CMOS is not completely dominated by the reduction of channel parameters. It depends on the continuous technological implementation of materials used in MOS devices (e.g. will be discussed in section. 2.3.1.1). The "More-than-Moore" law approaches the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board-level into a particular package-level, SIP (system- in-package), chip-level SOC (system-on- chip) potential solution for microprocessor, memory and logic device [1, 14, 17].

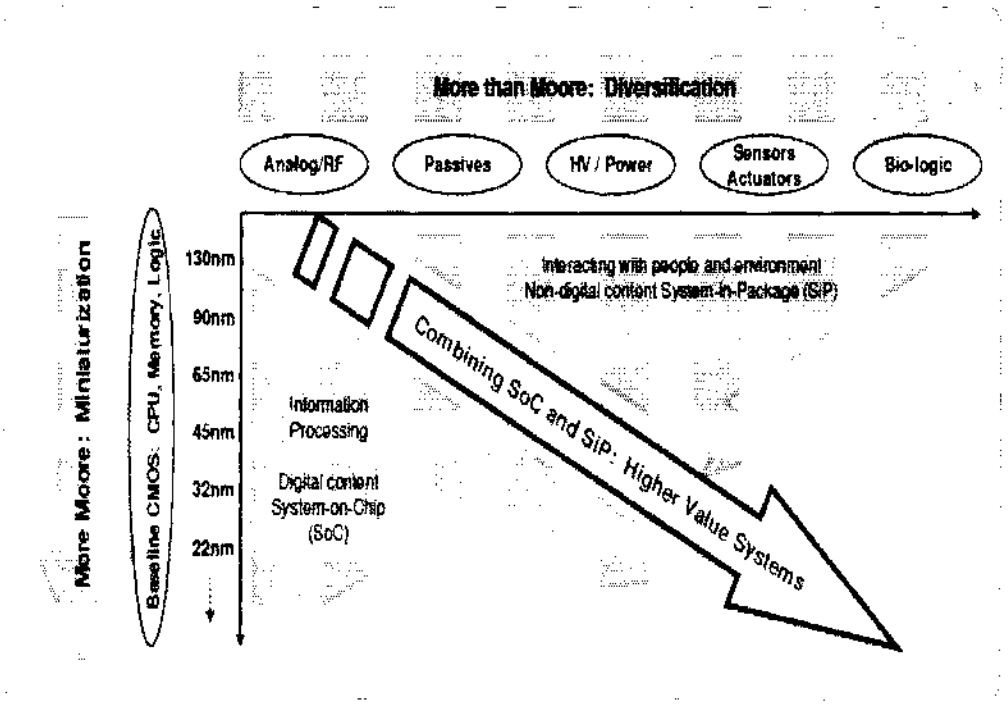

Figure 2.4 : Moore law and more [6]

Fig. 2.3 shows that the "More-than-Moore" scaling is equivalent to scaling (e.g. 2.1.2.2) vs. functional diversification of Baseline CMOS. This figure represents the continuous trends to combine of SOC and SIP with the continuous reduction of channel length of conventional MOSFET.

2.2. Scaling Trends

Moore's law is the most common trend in semiconductor industry. Within the last four decades rapid rate of improvement of products, especially integrated circuit has become very much significant [1]. Reduction of minimum feature size, switching time and cost per function with the increment of speed and density are the most vital trend. These trends have great role in the improvement of economic productivity and overall quality of life [1]. For these reasons, it is important to review the past trends and consider the possible future limits of MOS transistor evolution. The rise in circuit complexity and speed is accompanied by MOSFET scaling [18].

Table 2.1: Improvement Trends for ICs Enabled by Feature Scaling [1]

TREND	EXAMPLE
Integration Level	Components/chip, Moore's Law
Cost	Cost per function
Speed	Microprocessor throughput
Power	Laptop or cell phone battery life
Compactness	Small and light-weight products
Functionality	Nonvolatile memory, imager

The principal categories of improvement trends are shown in Table 2.1 with examples of each. Most of these trends have resulted principally from the industry's ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits.

2.3. Grand Challenges in Scaling of Future Transistors

The modern semiconductor technology is entering a new age as the industry begins to address the theoretical limits of CMOS scaling. There remain many technological challenges in modeling, complex materials, strain engineering particularly in CMOS device structures, junction leakage, process control and manufacture. Challenges also span system-on-chip (SOC) and system-in-package (SIP) integration of CMOS with new types of memory devices. All these will be the essential elements for the continuous growth of the semiconductor industry [1].

2.3.1. In the near term through 2016

Table 2.2 : ITRS Table Structure—Key Lithography-related Characteristics by Product [1]

YEAR OF PRODUCTION	2009	2010	2011	2012	2013	2014	2015	2016
Flash Uncontested Poly Si ½ Pitch (nm)	38	32	28	25	23	20	18	15.9
DRAM stagger-contacted Metal 1 (M1) ½ Pitch (nm)	52	45	40	36	32	28	25	22.5
MPU/ASIC stagger-contacted Metal 1 (M1) ½ Pitch (nm)	54	45	38	32	27	24	21	18.9
MPU Printed Gate Length (nm)	47	41	35	31	28	25	22	19.8
MPU Physical Gate Length (nm)	29	27	24	22	20	18	17	15.3

Table 2.2 is a technology requirement table from the year 2009 to 2016. This table is intended to indicate current best estimates of introduction timing for specific technology requirements.

2.3.2. In the long term beyond 2016

Table 2.3 : ITRS Table Structure—Key Lithography-related Characteristics by Product [1]

YEAR OF PRODUCTION	2017	2018	2019	2020	2021	2022	2023	2024
Flash Uncontacted Poly Si ½ Pitch (nm)	14.2	12.6	11.3	10.0	8.9	8.0	7.1	6.3
DRAM stagger-contacted Metal 1 (M1) ½ Pitch (nm)	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9
MPU/ASIC stagger-contacted Metal 1 (M1) ½ Pitch (nm)	16.9	15.0	13.4	11.9	10.6	9.5	8.4	7.5
MPU Printed Gate Length(nm)	17.7	15.7	14.0	12.5	11.1	9.9	8.8	7.9
MPU Physical Gate Length(nm)	14.0	12.8	11.7	10.7	9.7	8.9	8.1	7.4

Table 2.3 is a technology requirement table from the year 2017 to 2024. This table is intended to indicate current best estimates of introduction timing for specific technology requirements. It also shows that the transistor size will be under 10nm regime within 2024.

2.4. Scaling Beyond CMOS

The conventional path of CMOS scaling is accomplished by reducing the gate dielectric thickness, reducing the gate length and increasing the channel doping. This process might no longer meet the application requirements set by performance and power consumption [e.g. 2.1.3]. Semiconductor manufacturers have been investigating alternative transistor architectures such as DG (double-gated) MOSFETS, SOI (Silicon on Insulator) technology and Tri-gate technology. The major problem is in the manufacture of these processes; because the CMOS technology will soon have a lower rate of performance improvement as their size is reduced [8]. Introduction of new material systems, new device architecture, as well as continuous process control improvement are needed to break the scaling barriers beyond CMOS technology.

It is required to change the polysilicon as the gate material for the current CMOS devices, due to increment of gate capacitance and stress resistance due to aggressive scaling [2]. It is said that silicon can be scaled to 22 nm devices, but beyond this limit, higher mobility materials such as Ge, SiGe, and III-V compound such as InGaAs (i.e. indium gallium arsenide), may be used as channel material [19]. This limiting will increase the gate tunneling currents, due to the band-gap narrowing, which is also challenging for the near future.

The strain Si can be introduced by some layer added to the silicon. This layer may expand or in some other way it may stretch the silicon. This layer forces the silicon to stretch to make the bonds. This allows the holes and electrons to flow more freely, which will reduce device resistance and other properties effected by electron or hole mobility. While this technique is implemented, it has the disadvantage that from a fabrication stand point, it is not compatible with many of the other new technology [20].

Nitride SiO_2 gate dielectric is replaced by a hafnium-based dielectric (e.g. HfO_2) with a dielectric constant (κ). In 2008, the dielectric constant (κ) was approximately twenty [1]. ZrO_2 and HfO_2 emerged as promising high-k dielectrics for ultra-thin gate dielectric application and both films have promising characteristics such as low leakage current, good interface properties (Dit $\sim 10^{11} 1/eV - cm^2$) and excellent reliability properties [2].

2.5. Implement of NON-CLASSICAL CMOS channel Materials

To attain sufficient drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced thermal velocity and injection at the source end appears to be required. Eventually, high transport channel materials such as III-V or germanium thin channels on silicon, or even semiconductor nanowires, carbon nanotubes, graphene or others may be needed. Non-classical CMOS devices need to integrate physically or functionally onto a CMOS platform [19]. Thus integration requires epitaxial growth of foreign semiconductor on Si substrate which is challenging. The desired material or device properties must be maintained through and after high temperature and corrosive chemical processing. Reliability issues should be identified and addressed early in the technology development [1].

2.6. Reasons Behind Ballistic MOSFET

To attain adequate drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced thermal velocity and injection at the source end appears to be required [21].

MOSFET channel lengths continue to shrink rapidly towards the sub-10 nm dimensions according to the International Technology Roadmap for Semiconductors [1]. United with the use of high-mobility channel materials, nanoscale channel lengths open up the possibility of near-ballistic MOSFET operation. As MOSFET scaling continues, molecular transistors (e.g. CNTFET) that could replace them are also being explored [22].

As the MOSFET dimensions are reduced further in the sub 10 nm regime, ballistic transport will become a very important factor in governing the current characteristics. The maximum current a MOSFET can physically carry and the fastest it can operate is governed by the ballistic transport in the channel. Therefore, we should thoroughly understand this fact, by the use of physical models and device simulations. To realize a device with 100% ballistic transport, efforts have to be directed to address the issues that hamper the ballistic transport, like reducing the channel scattering, improving the Si-SiO_2 interface and usage of double gate structures [23].

3. BALLISTIC MOSFET

In ballistic MOSFET, the main feature is the ballistic transport. Ballistic transport actually means that the electrons pass from the source to the drain through the channel without any scattering. In the ballistic MOSFET, flow of the electrons in the channel, simply follow the Newton's second law [24].

For the ideal case of ballistic transport, the electrons are not scattered in the length of L. In this case, L denotes the channel length of the ballistic MOSFET [24].

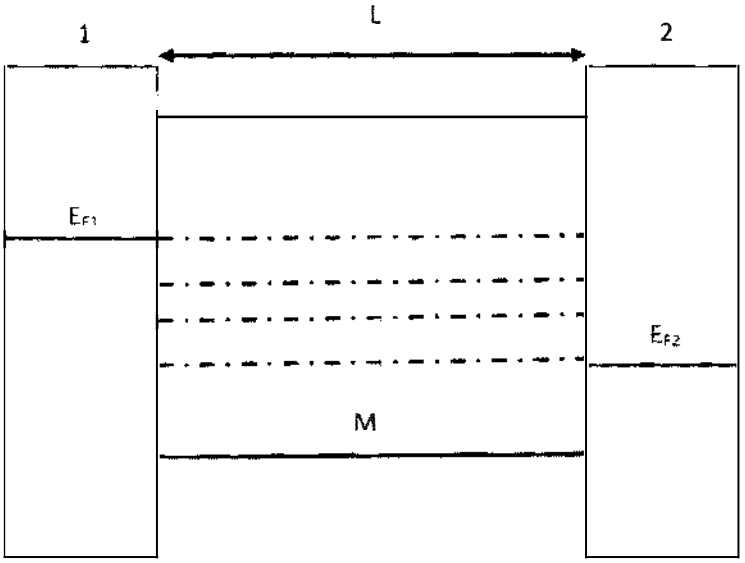

Figure 3.1: A Ballistic Conductor

In this Fig. 3.1, the L represents the channel length between the two electrodes 1 and 2. E_{F1} and E_{F2} represent the source and drain Fermi level respectively. M represents the number of channels for the electrons to pass from the electrodes 1 to 2. The dotted lines in Fig. 3.1, represents the electrons passing through the channel of the ballistic MOSFET.

The wave vector k is defined by position of the source and the drain Fermi level. If $k>0$, then electron passes from the source to drain. On the other hand, if $k<0$, then, electron passes from the drain to source. The wave vector k states are given by the Fermi functions for the left and right contacts.

Fig. 3.1 shows that $E_{F1}>E_{F2}$, so the electrons pass through the source to drain. We considered the channel to be ballistic, that is why electron passes through the source to drain without scattering and the velocity of electrons is also much higher.

The deca-nanometer MOSFETs will achieve its success in device scaling within the near future. Since the mean free path of a carrier in the device will be in the 10 nm range, the events of scattering probability due to downscaling will be intensified. If the device size L, is sufficiently larger than the mean free path λ, the carrier flow is controlled by the diffusive transport [25]. On the other hand, if the L is smaller than λ then the scattering probability in the channel is negligibly small. Thus, the ballistic transport and the device current are completely controlled by the carrier injection from the source into the channel [25].

3.1. Theory of the Ballistic MOSFET

We have presented an overview of the theory of the ballistic MOSFET as proposed by Natori [25]. In the Natori's theory, E – k relation shows the top of the barrier transport model, and also shows the source and drain Fermi level [25]. The k state is occupied by the source and drain Fermi level.

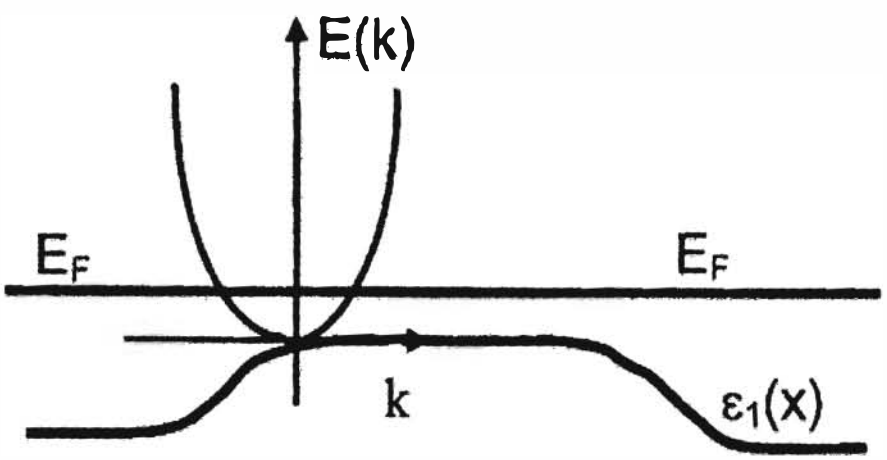

Figure 3.2: E –k relationship, at V_{DS}=0 [26]

In Fig. 3.2 shows the E-k relationship at V_{DS}=0. The positive and negative k states are equally occupied for V_{DS}=0. In this case, the average velocity is zero and the drain current, I_D=0 [25].

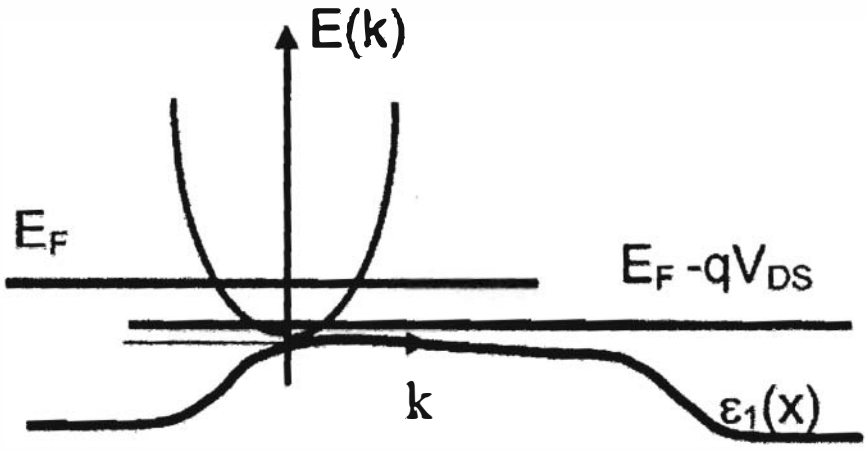

Figure 3.3: E –k relationship, at small V_{DS} [26]

In Fig. 3.3 a small drain voltage is applied. For that reason the drain Fermi level is lowered and fewer negative k states are occupied. The net velocity is positive. The drain current is proportional to the V_{DS} [25].

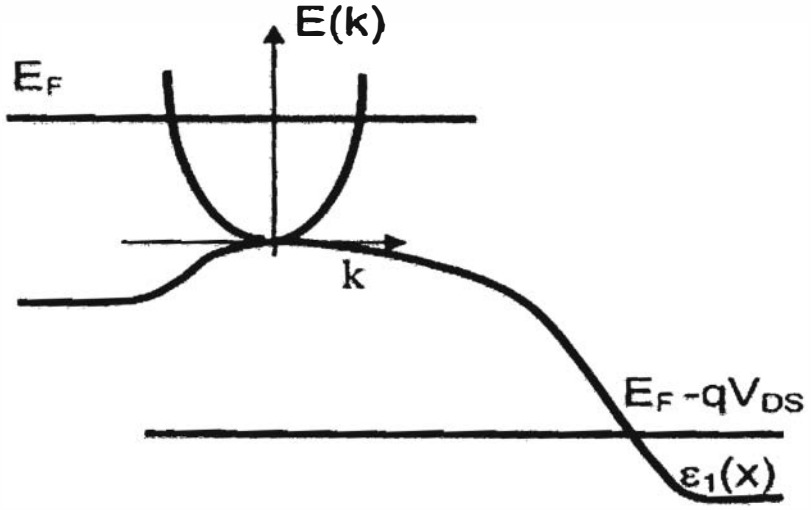

Figure 3.4: E –k relationship for large V_{DS} [26]

For large V_{DS}, the negative k states are empty in Fig. 3.4. The gate voltage determines the velocity of the electrons in the channel. Here, the average velocity has been saturated, which determines the location of the Fermi level within the conduction band. In this case drain current is saturated and the drain current is called on – current [26].

In the positive and negative halves of the E – k relationship, we can relate the carrier populations and it depends on the respective Fermi levels. At the top of the barrier the total carrier density is approximately independent of drain voltage. So we find the equation of Fermi level is -

$$n_s^+(E_f)+n_s^-(E_f- qV_{DS}) = Q(0)/(-q)\approx C_{ox}(V_{GS}-V_T)/(-q) \quad (3.1)$$

In equation (3.1), n_s^+ and n_s^- are defined by the two-dimensional carrier densities at the top of the barrier. We found that the two – dimensional carrier densities are

$$n_s^+ = \frac{N_{2D}}{2} F_0\left[(E_f - \varepsilon)/k_B T_L\right] \quad (3.2)$$

$$n_s^- = \frac{N_{2D}}{2} F_0\left[(E_f - qV_D - \varepsilon)/k_B T_L\right] \quad (3.3)$$

In equation (3.1), E_f is the source Fermi level, $E_f - qV_{DS}$ is the drain Fermi level, q as the electron charge, V_T, V_{DS} and V_{GS} are the threshold voltage, drain voltage and gate voltage respectively. The gate capacitance is C_{OX}. Q(0) represents the charge at the top of the barrier. Equation (3.1) determines the location of the Fermi level as a function of gate and drain voltage. If the drain voltage is increased then n_s^- decreases, as a result E_f have to increase to maintain the change balance [26]. In the equation (3.2) and equation (3.3), we found that N_{2D} and F_0 represent the two-dimensional density of states and the Fermi-Dirac integral of the order of 0 respectively. k_B is the Boltzmann constant and ε represent the lowest subband level at the top of the barrier and also referred as the energy at the top of the barrier.

3.2. Filling states in Ballistic MOSFET

Filling states in the ballistic MOSFET are directly depended on the source and drain carrier injection. In this case the positive k – states are filled by injection from the source according to

the source Fermi level, E_F and negative k – states are filled from the drain according to the drain Fermi level, $E_F - qV_{DS}$ [26].

We find the total energy from the simple effective mass approximation,

$$E = E_c(x) + E(p) = E_c(x) + \frac{p^2}{2m^*} \tag{3.4}$$

In this equation $E_C(x)$ is the conduction band minimum versus position. Here, p is the momentum and m* is the effective mass.

We knew from the arguments of equilibrium condition, the proper distribution function of total energy is the Fermi-Dirac function, which is defined as follows,

$$f_0(E) = \frac{1}{1+e^{(E-E_F)/K_BT}} \tag{3.5}$$

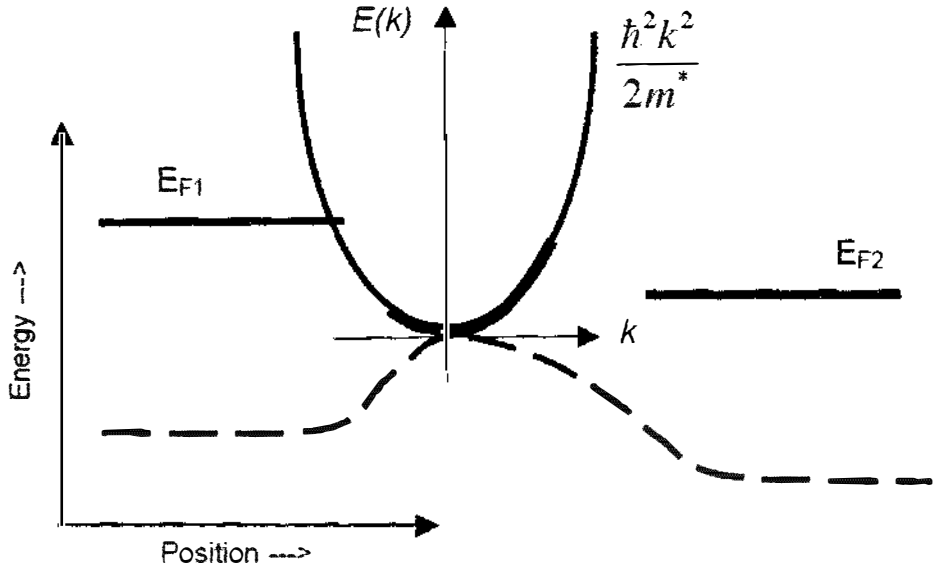

Figure 3.5: The E (k) relation at the top of the barrier of ballistic device [27]

In Fig. 3.5, of the ballistic device, the electrons come from the source have positive velocities at the top of the barrier. If the electrons come from the drain, it contains negative velocities [27].

3.3. Current Voltage Characteristics

The current in the ballistic MOSFET can be expressed in terms of elementary parameters. In the ballistic MOSFET current does not depend on the mobility. It is proportional to the width of the device and the oxide capacitance [23].

For low V_{DS}, the MOSFET behaves like a resistor and for a high V_{DS}, it behaves like a current source. As V_D increases, the magnitude of the negative component will be negligible [25]. For any type of MOSFET, the gate voltage controls the conductivity of the channel by raising or lowering the height of an energy barrier between the source and channel [26].

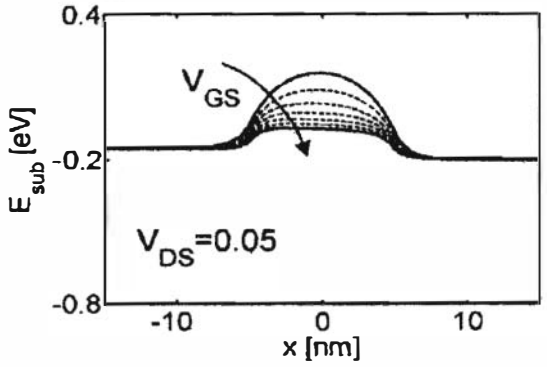

Figure 3.6: Minimum energy vs. position at low gate voltage [26]

In Fig. 3.6, under low voltage, the device operates like a resistor and the gate voltage controls the resistance [27]. The energy barrier is slightly lowered by applying the lower drain bias.

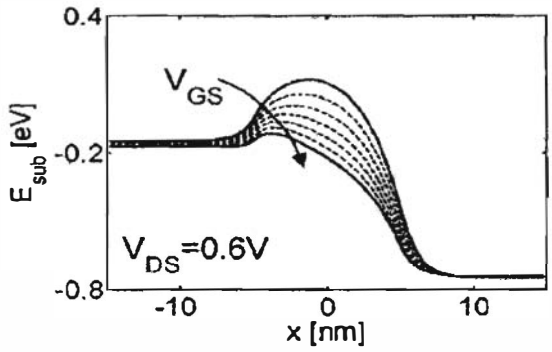

Figure 3.7: Minimum energy vs. position at high gate voltage [26]

In Fig. 3.7 the device behaves like a current source and the gate voltage control the magnitude of the current [26]. The energy barrier becomes lower by the application of the higher drain bias.

Current is the most important feature of ballistic MOSFETs. We found the current equation as follows:

$$n_s^+(0) = \frac{N_{2D}}{2}\log\left(1 + e^{(E_F-\varepsilon_1)/k_BT_L}\right) = \frac{N_{2D}}{2}F_0(\eta_F) \tag{3.6}$$

$$n_s^-(0) = \frac{N_{2D}}{2}\log\left(1 + e^{(E_F-qV_D-\varepsilon_1)/k_BT_L}\right) = \frac{N_{2D}}{2}F_0(\eta_F - U_D) \tag{3.7}$$

In these equations, η_F and U_D are defined as,

$$\eta_F = (E_F - \varepsilon_1)/k_BT_L$$

$$U_D = V_D/\left(\frac{k_BT_L}{q}\right)$$

Here, η_F is the location of the Fermi level, which is also referred as the normalize Fermi energy level. U_D represent the drain potential.

Positive and negative velocities of the electrons are defined below:

$$v^+ = v_T\frac{F_{1/2}(\eta_F)}{F_0(\eta_F)} \tag{3.8}$$

$$v^- = v_T\frac{F_{1/2}(\eta_F-U_D)}{F_0(\eta_F-U_D)} \tag{3.9}$$

Due to the positive and negative velocity there are positive and negative currents which are define as follows:

$$I^+ = qWn_s^+v^+ \tag{3.10}$$

$$I^- = qWn_s^-v^- \tag{3.11}$$

In these expressions, F_0 is the Fermi-Dirac integral of order 0 and $F_{1/2}$ is of the order 1/2. Using these equations, we found

$$\frac{n_S^-(0)}{n_S^+(0)} = \frac{F_0(\eta_F - U_D)}{F_0(\eta_F)} \tag{3.12a}$$

and

$$\frac{v^-}{v^+} = \frac{F_{1/2}(\eta_F - U_D)}{F_{1/2}(\eta_F)} \frac{F_0(\eta_F)}{F_0(\eta_F - U_D)} \tag{3.12b}$$

Using these results in eqn. (3.12), we found the general I-V characteristic as

$$I_D = qWn_S v_T \left[\frac{1 - \frac{F_{1/2}(\eta_F - U_D)}{F_{1/2}(\eta_F)}}{1 + \frac{F_0(\eta_F - U_D)}{F_0(\eta_F)}} \right] \tag{3.13}$$

Where the injection velocity is defined as,

$$v_T = \sqrt{\frac{2k_B T_L}{\pi m^*}} \left(\frac{F_{1/2}(\eta_F)}{F_0(\eta_F)} \right) \tag{3.14}$$

The location of the Fermi level, η_F, is determined by how much charge the gate induces in the semiconductor, which defines as,

$$C_{ox}(V_{GS} - V_T) = \frac{qN_{2D}}{2} [F_0(\eta_F) + F_0(\eta_F - U_D)] \tag{3.15}$$

Equations (3.13) - (3.15) specify the $I_D(V_{GS}, V_{DS})$ characteristics.

For high drain bias, the factor in square brackets reduces to unity and as a result we found that the on-current as is

$$I_D(on) = WC_{ox}v_T(V_G - V_T) \tag{3.16}$$

4. ANALYSIS & COMPARISON

In this section, FETToy simulation tools based on MATLAB are used to calculate the current in ballistic field-effect transistors [28]. We analyzed different types of MOSFETs such as, single gate bulk MOSFET, double gate MOSFET, nanowire transistor and CNT FET. We actually compared on-current (I_{on}) and transconductance (g_m), in terms of changing device parameters such as gate oxide thickness (t_{ox}) and initial source Fermi level (E_f) for different types of transistors.

The main limitation of the model we implemented are that, the off-current (I_{off}) and the output conductance (g_d) remains almost constant due to further changing of device parameters. On the other hand, FETToy can't properly model Subthreshold Swing (S) and Drain induced Barrier Lowering (DIBL). That's why; comparison of these parameters is neglected from FETToy result.

4.1. Different Types of Devices

In this simulation process we have fixed some parameters. These parameters are like: gate insulator thickness (t_{ox}) which is set at 1.5 nm, gate insulator dielectric constant (ε_r) which is set at 3.9, silicon body thickness (t_{Si}), is set at 1 nm, temperature (T) is set at 300 K.

The position of the Fermi level within the band gap in source and drain regions can be determined by the function of electron and hole concentrations. In this thesis, we have determined the source Fermi level as a function of donar concentration (n type) for silicon at T = 300 K. As the doping levels decrease, the Fermi energy level moves closer to the valence band. That's why the gap between source Fermi level and conduction band increase, thus the flow of electrons from source will decrease eventually. As a result, the on-current will decreased with further reduction of doping concentration [29]. Initial source Fermi level (E_F) is set at -0.32 eV.

Gate control parameter (α_G) is set to get correct gate control and Drain control parameter (α_D) is set to produce the correct Drain induced Barrier Lowering (DIBL). α_G is set at 0.88 and α_D is set at 0.035.

4.1.1. Single gate bulk MOSFET

In the single gate bulk MOSFET, the gate controls the channel. We know that the oxide thickness should be small for good control of the device. Because of the small length of channel, the source is influenced by the drain. In single gate bulk MOSFET, leakage current is much higher than the other types of device.

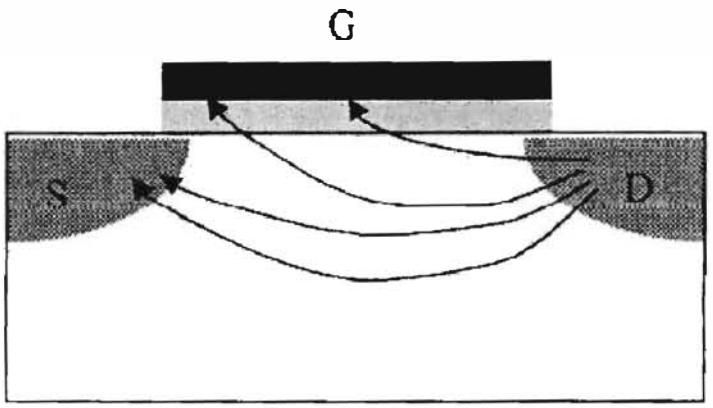

Figure 4.1: Drain electric field lines in single gate MOSFET

According to the Fig. 4.1 in single gate bulk MOSFET, the electric field lines are influenced by the channel potential as they are near the source [26]. Thus leakage current is induced in the single gate bulk MOSFET. In this case the gate could not be properly controlled by the channel. In the bulk MOSFET, the carrier injection velocity and transconductance are low.

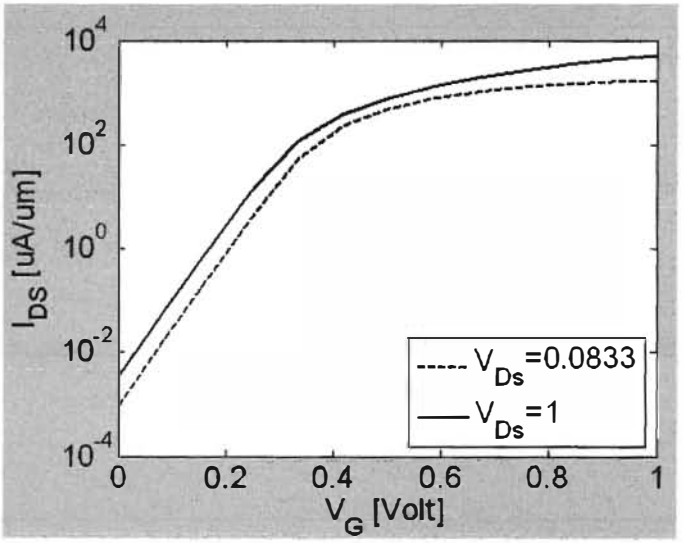

Figure 4.2: I_{DS} vs. V_G for SG bulk MOSFET

In Fig. 4.2 we see that, the current saturates with the change of gate voltage in the semi-log scale. The current is shown in the log scale and the gate voltage is shown in the normal scale. The drain current saturates after a minimum gate voltage variation. In Fig. 4.2, the upper line represents the drain current. We get it for the drain voltage equal to 1V. The dotted line represents the drain current for the drain voltage which is equal to 0.0833V.

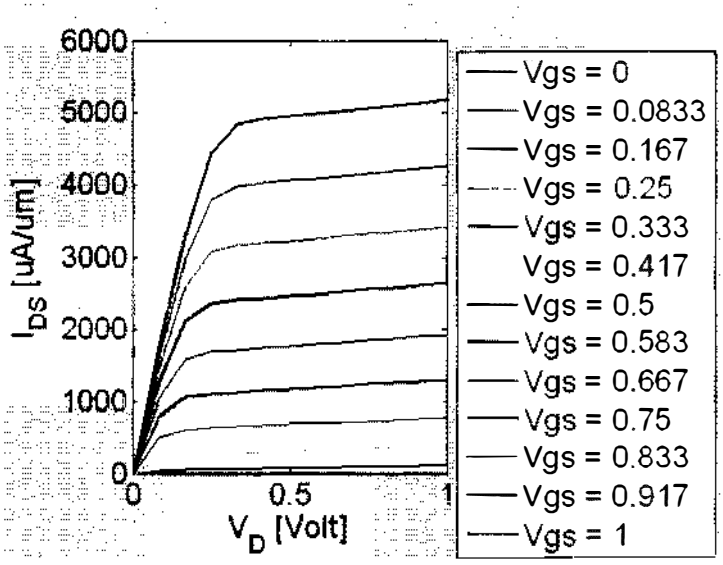

Figure 4.3: I_{DS} vs. V_D with V_{GS} as a parameter

In Fig.4.3, we see that, for low drain voltage the MOSFET operates like a gate voltage dependent resistor. On the other hand, for high V_{DS} it operates like a gate voltage controlled current source. After a minimum drain voltage the drain current is saturated. The magnitude of the current is depending on the gate voltage. If the gate voltage increases the magnitude of the current also increases.

4.1.2.Double gate MOSFET

DG MOSFET has a smaller geometric scaling length. The DG MOSFET has two gates, one is the front gate and the other is the back gate. Thus, there is an excellent channel control in the DG MOSFET. DG MOSFET can overcome the short channel effect which is mentioned in the ITRS roadmap [1].

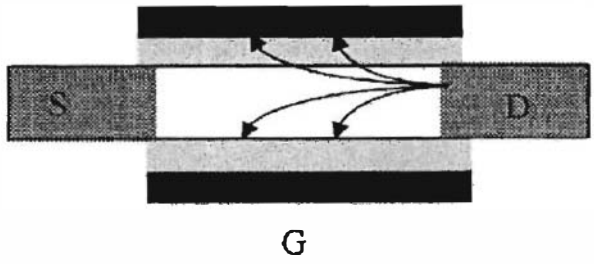

Figure 4.4: Drain electric field lines in DG MOSFET

Fig. 4.4 shows that, the drain potential does not have any influence over the source. The channel control over the gate is adequate. DG MOSFET has very good control in the case of short channel effects. In the DG MOSFET the carrier injection velocity and transconductance are higher than the bulk MOSFET. The ITRS roadmap defines that, the DG MOSFET has produced an ideal subthreshold swing.

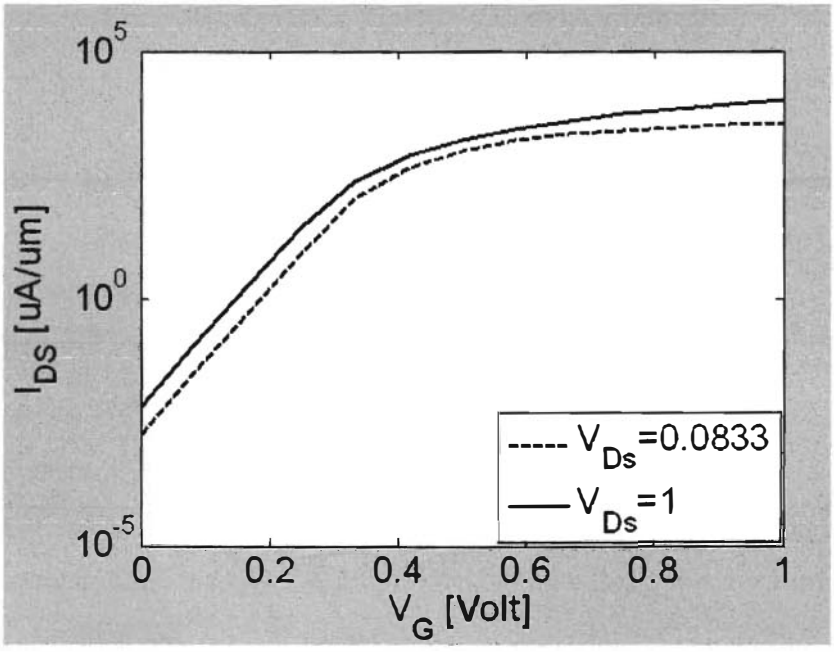

Figure 4.5: The I_{DS} vs. V_G characteristic curve for the DG MOSFET

Fig. 4.5 shows that the current is saturated after a threshold value. The on-current is almost one order of magnitude greater than the bulk MOSFET. In Fig. 4.5, the dotted line represents the low V_{DS} and the upper line represents the larger V_{DS}. The gate voltage controls the electric field and determines the current flow through the channel.

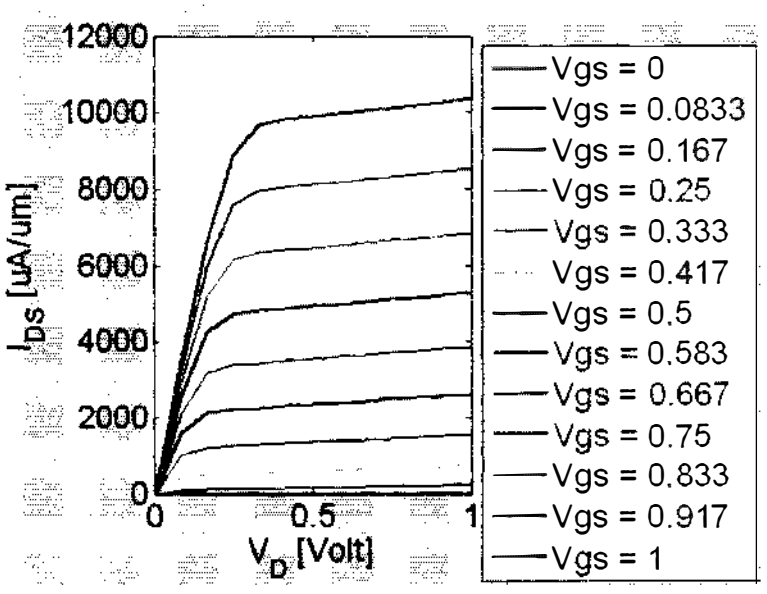

Figure 4.6: The I_{DS} vs. V_D characteristic curve with V_{GS} as a parameter

In Fig. 4.6, we see that the magnitude of current is almost double than the bulk MOSFET. In double gate MOSFET, the current magnitude depends on the gate voltage and the drain voltage.

In DG MOSFET the most common mode of operation is to switch both gates together. Another mode of operation is the switching of any one gate and applying fixed bias to the other gate. In DG MOSFET, maintenance of good electrical characteristics such as, I_{on}/I_{off} ratio is very high than the bulk MOSFET.

4.1.3. Nanowire FET

Si nanowire MOSFET is one of the most promising candidates for future extension of the device for its decrease of size [30]. Nanowire MOSFET uses metal as source and drain contact and it operates in accumulation mode [31]. The gate bias is induced to the majority carriers [31].

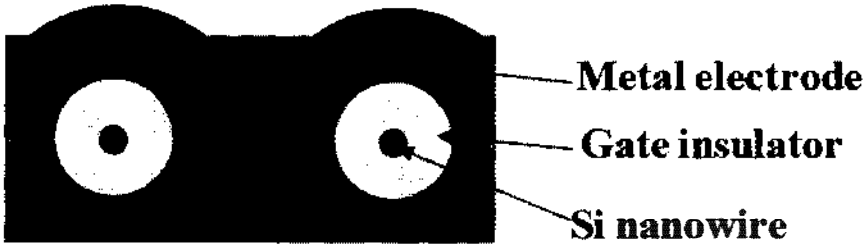

Figure 4.7: Schematic diagram of nanowire MOSFET [30]

Fig. 4.7 shows a schematic diagram of nano wire MOSFET. Here, we observe that the gate insulator is surrounding the nanowire. Thus in the channel, high carrier mobility induced, is good for conduction current. In nanowire, high performance occurs.

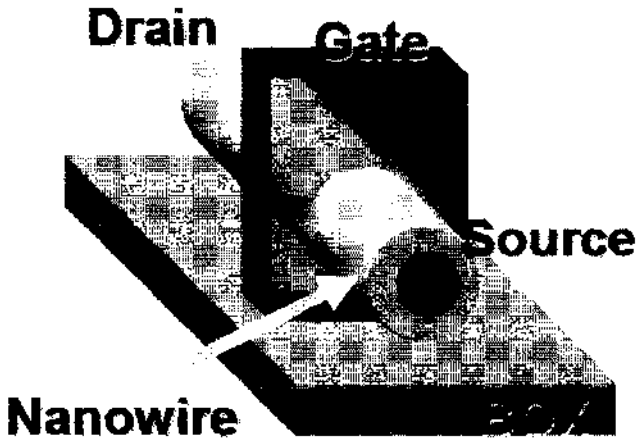

Figure 4.8: Gate all around in Nanowire MOSFET [30]

In Fig. 4.8 we see that, the gate surrounds the nanowire. Thus the gate has a good control over the channel [30]. For this reason of GAA (Gate all around), the nanowire obtained high I_{on}/I_{off} ratio [30].

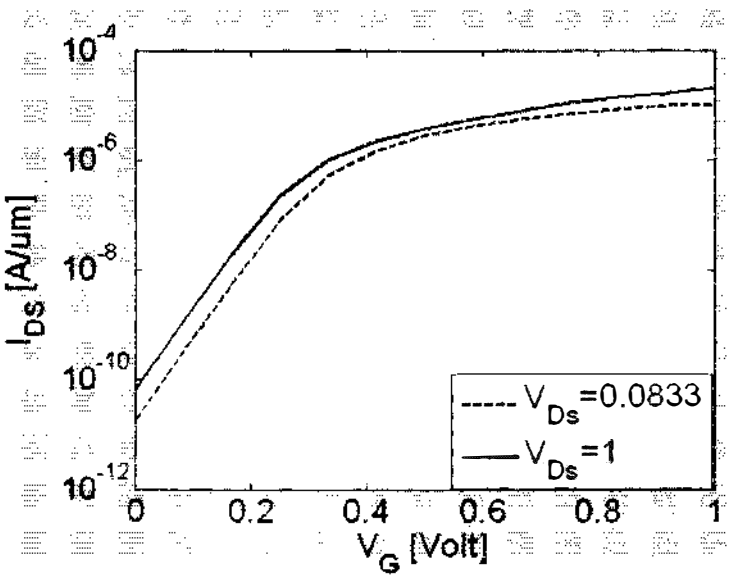

Figure 4.9: The I_{DS} vs. V_G characteristic curve for Nanowire FET

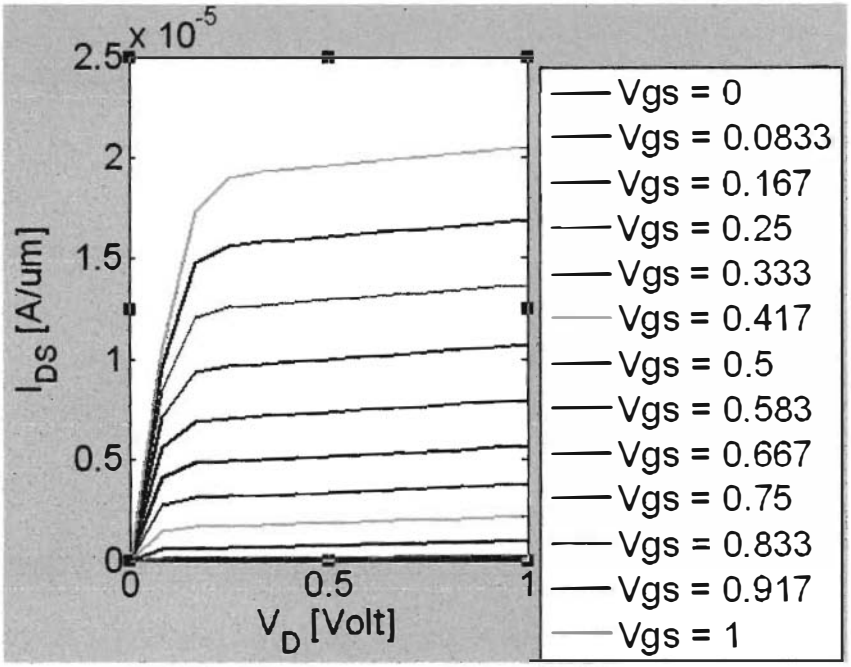

Figure 4.10: The I_{DS} vs. V_D characteristic curve with V_{GS} as a parameter

In Fig.4.9 and Fig. 4.10 the current is saturated after a threshold value. We see that the drain current is higher than the SG MOSFET and DG MOSFET. Here also, the gate voltage controls the magnitude of the drain current.

Nanowire MOSFET has the best cross-section for the surrounding gate. It has scalable nanostructure with correctly controlled critical dimensions.

4.1.4. CNTFET

In 1998 the first CNTFET operation has been verified and the recent year's device performance has been significantly improved. In the room temperature CNTFET operates in ballistic regime along with very small drain and gate voltage [32]. Thus CNTFETS are promising candidates for the nano-scale electron devices. CNTFETs promises intrinsic performance comparable to Si based MOSFET technology. CNTFET can provide almost linear operation over a wide range of input signal strengths [32].

CNT is significantly equivalent to a two dimensional graphene sheet rolled into a tube. CNTFET has three types of structures. These are ZIG ZAG, Arm chair and Chiral structure.

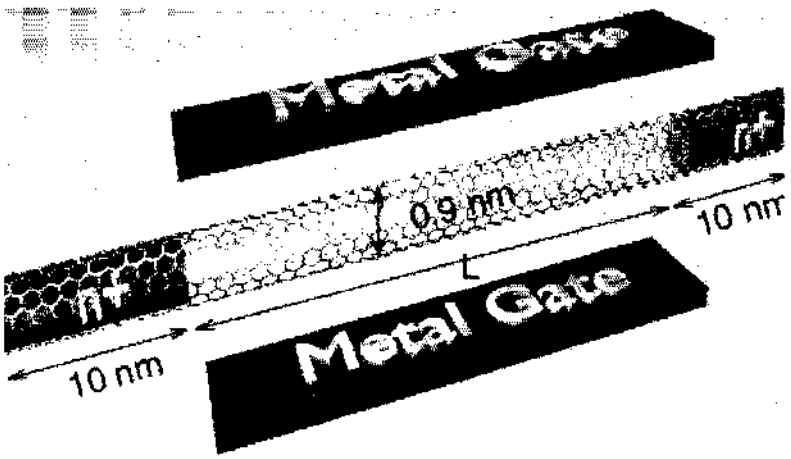

Figure 4.11: Structure of a CNTFET [32]

Fig. 4.11 shows a CNTFET structure. Here we observed that, the more gates around the channel the more the metal is used in the gate structure.

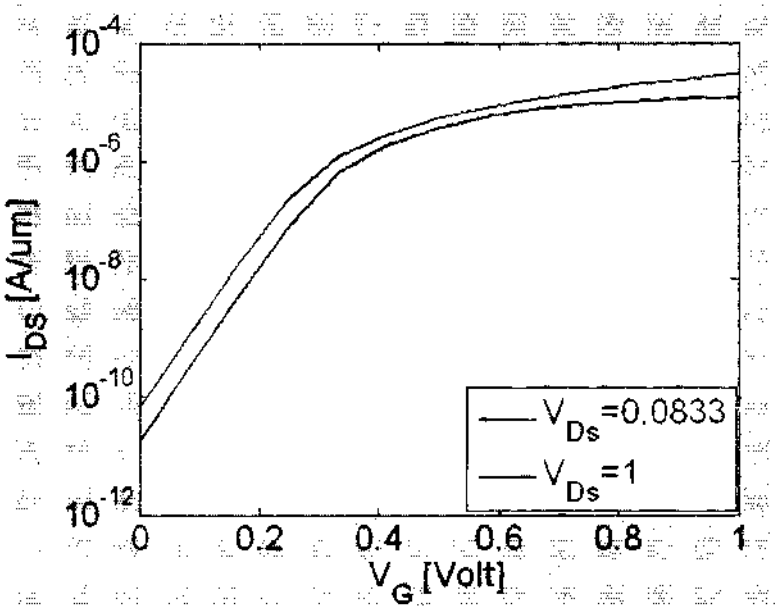

Figure 4.12: The I_{DS} vs. V_G characteristic curve

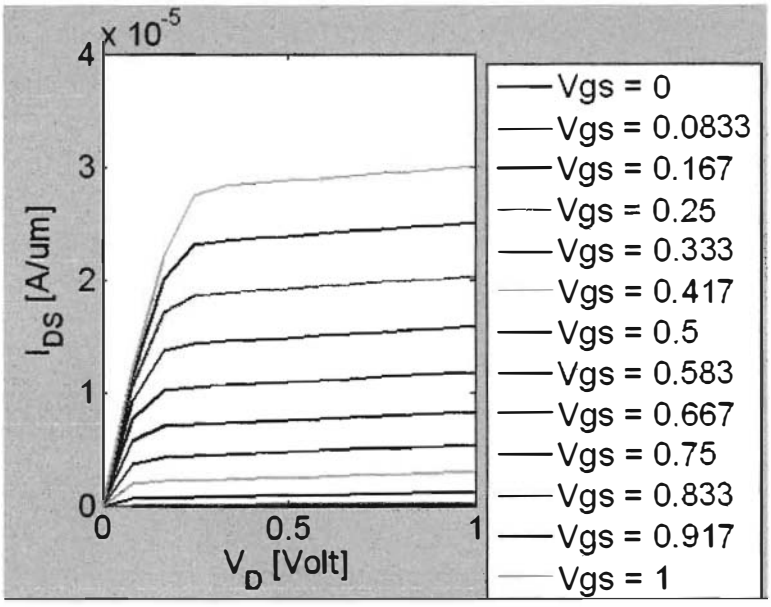

Figure 4.13: The I_{DS} vs. V_D characteristic curve with V_{GS} as a parameter

In the simulation result of Fig. 4.12 and Fig. 4.13 we saw that, the current is saturated after the threshold voltage. In the CNT FET channel is ballistic and carrier injection velocity is high. The most significant feature of CNT FET is that, drain current is much higher than the nanowire transistor. This is a very good significance for nano-electronic device.

4.2. Comparison between different types of Device

In this section we compare the different types of output parameters in several nano – devices.

4.2.1. Effect of changing Gate oxide thickness on Different types of Devices

In this section the effect of changing gate insulator thickness for different types of devices are discussed. It is important to know the changing effects, because the rapid shrinking of gate insulator thickness let the overall device size to be reduced. We only discussed about the changing effect on I_{on} and g_m. Other parameters remain constant with the varying of the gate insulator thickness in the top of the barrier model.

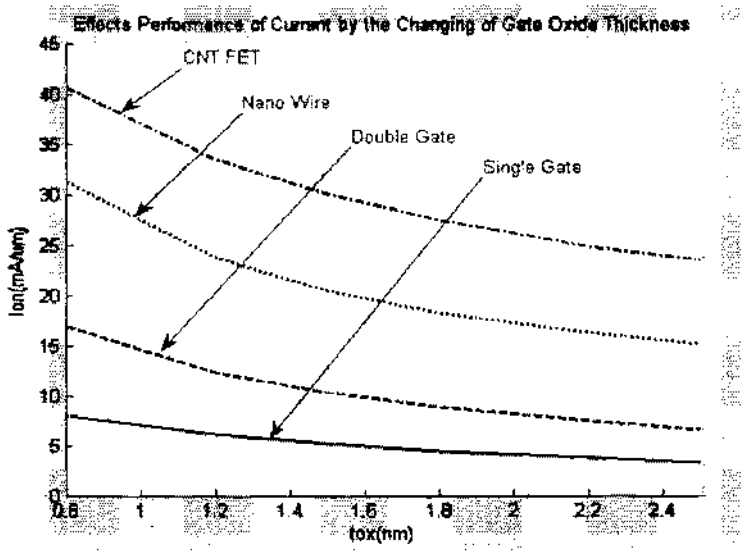

Figure 4.14: Effects of performance of current (I_{on}) by varying the gate oxide thickness (t_{ox})

ig. 4.14 shows that the increment of the gate insulator thickness will cause the decrement on the n current of SG MOSFET, DG MOSFET, Carbon Nanowire and CNTFET. On the other hand, is visible that, for a constant t_{ox}, the performance is increasing as one move from SG MOSFET o DG MOSFET, DG MOSFET to Si nanowire and Si nanowire to CNTFET. These movements emain same for the different values of insulator thickness. From this observation we can onsider CNTFET as the better MOS device, because it allows more current flow through the hannel than the other devices.

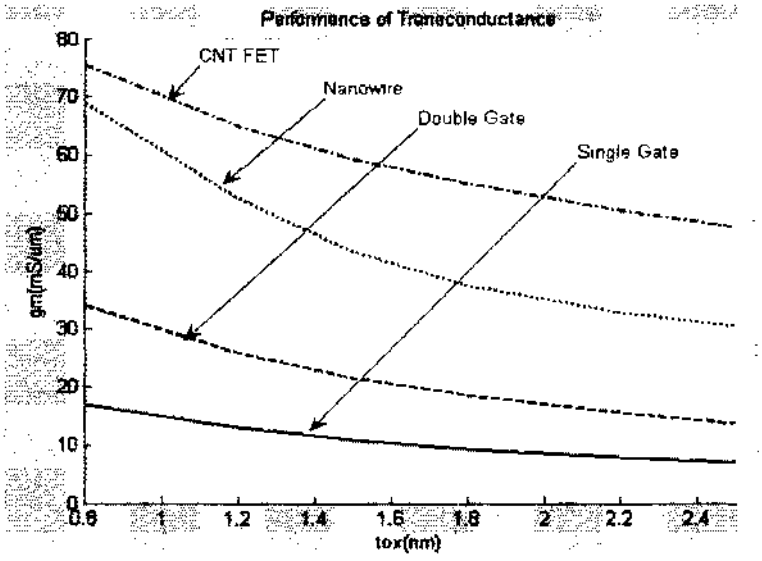

Figure 4.15: Effects on transconductance (g_m) by varying the gate oxide thickness (t_{ox})

g. 4.15 represents that the g_m is decreasing with the increment of gate oxide thickness of SG OSFET, DG MOSFET, Nanowire and CNTFET. Here again we have observed that, for a nstant t_{ox}, g_m is increasing as the movement from SG MOSFET to CNTFET. Greater nsconductance means more curreent between drain and source terminals. That's why NTFET is much better than the other MOSFET devices in terms of transconductance. The pid decrement of oxide thickness increases the performance of the devices.

2.2. Effect of Changing Initial Source Fermi Level (E_F) on different types of Devices

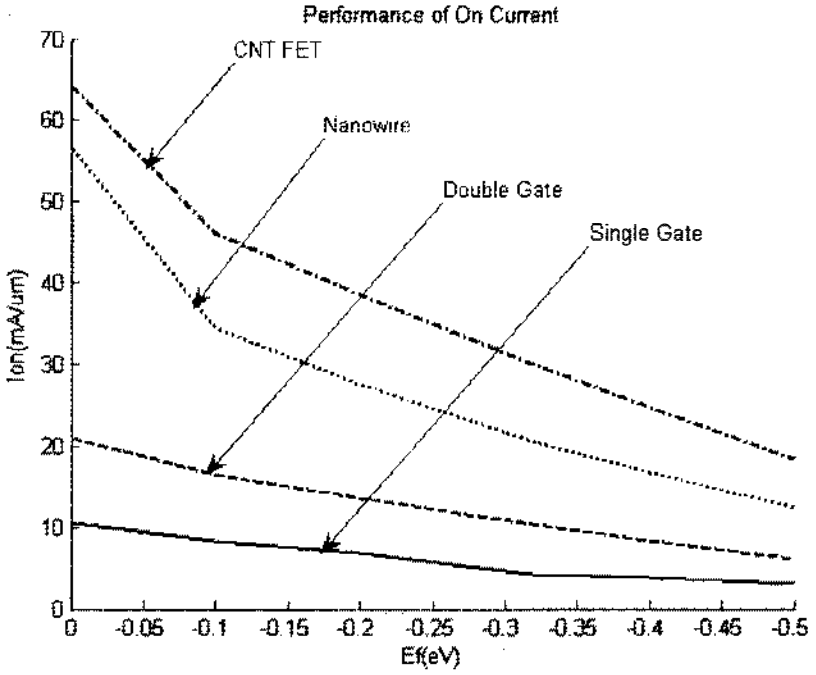

Figure 4.16: Effects on On Current (Ion) by varying the initial source Fermi level (Ef)

g. 4.16 describes the changing of the on-current of the SG MOSFET, DG MOSFET, nanowire and NTFET with respect to the change of the source Fermi level. Here we observed that with the decrement the value of the source Fermi level, the on-current value for each and every case also decreases. For ch device the on-current (I_{on}) is decreasing with the decrement of initial source Fermi level. On the ner hand, the performance is increasing, while diversifying from SG MOSFET to CNTFET for constant urce Fermi level for each device.

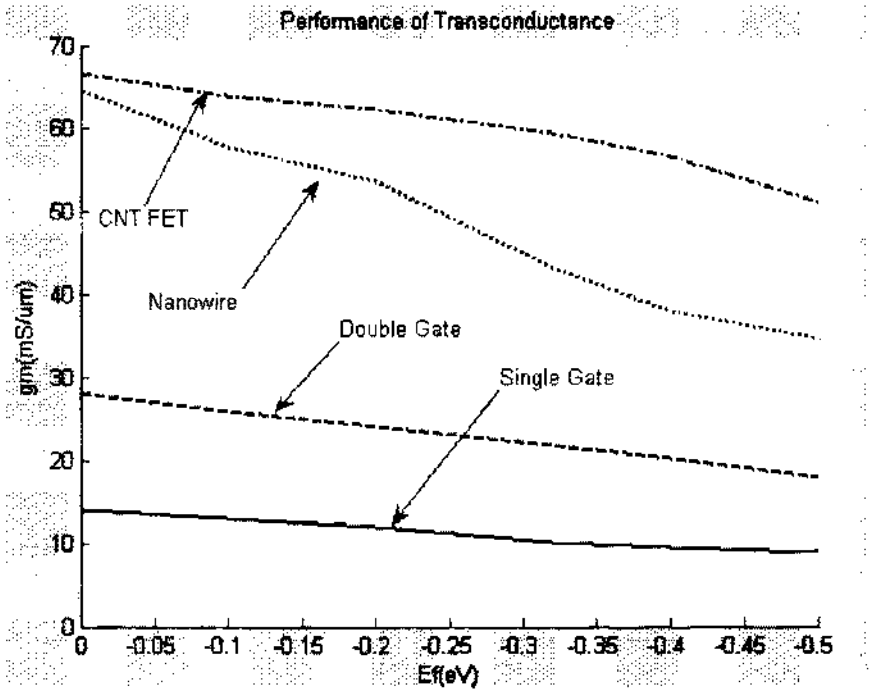

Figure 4.17: Effects on transconductance (gm) by varying the initial source Fermi level (Ef)

Fig. 4.17 shows that, the changing of the transconductance of the single gate MOSFET, double gate MOSFET, Nanowire and CNTFET with respect to the change of the source Fermi level. Here the value of the transconductance decreases with respect to the decrement of the value of the source Fermi level. The effect of further reduction of initial source Fermi level of transconductance (g_m) is identical with the effect of on-current (I_{on}). The CNTFET also shows better performance than the other devices with higher transconductance.

5. Conclusion

n this thesis we have focused on the evolution of the present development of nanoelectronic levices and the projection of future devices. Here we observed the performance of different kinds of MOS devices such as SG MOSFET, DG MOSFET, Si nanowire FET and CNTFET. FETToy simulation tool was used for numerical calculation to observe the changes of different parameters such as, insulator thickness and initial source Fermi level. This was based on the emi-classic ballistic transport theory of MOSFET according to the top of the barrier model. The cattering effects on the current transport through the MOSFET and two dimensional effects are lso neglected here.

5.1. Summary

n this thesis we have discussed about the effect of changing device type and device parameters en the On-Current (I_{on}) and the transconductance (g_m). The simulated results for the SG MOSFET, the DG MOSFET, nanowire and CNT FET were also shown in this report.

Among all this devices, the CNT FET has the best performance in terms of the On-Current and ransconductance parameters. We have also observed that the performance of MOSFET ncreases with the movement of technology used in MOS structure. These technologies are nainly the reduction of size of the MOSFET and the usage of new material. When the value of ie gate oxide thickness (t_{ox}) parameter is decreased, simultaneously the performances of the MOSFETs increase. When the value of the source Fermi level (E_f) is increased, the performances f the MOSFETs increased. The performance of MOSFET devices increase with the switching om SG MOSFET to DG MOSFET, DG MOSFET to Si nanowire FET, Si nanowire FET to NTFET. CNTFET has better On- Current (I_{on}) and transconductance (g_m) over the other vices. In near future, we have predicted that the current passing through the channel will be ssible without any scattering.

. Future Work

his thesis, we have analyzed the performance of On-Current (I_{on}) and transconductance (g_m) with erent types of transistors. The main limitation of this thesis is that FETToy cannot properly del Subthreshold Swing (S) and Drain Induced Barrier Lowering (DIBL). Further study can be formed using a more advanced model that overcomes these limitations. In future work, scattering cts should also be included.

6. References

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Appendix

Technological Trend of IC fabrication of Intel Corporation from 1971 – 2007