SIMULATION OF HIGH EFFICIENCY HIT SOLAR CELL

By

Jannate Bulbul
and
Razia Sultana Moyna

Submitted to the

Department of Electrical and Electronic Engineering
Faculty of Sciences and Engineering
East West University

In partial fulfillment of the requirements for the degree of
Bachelor of Science in Electrical and Electronic Engineering
(B.Sc. in EEE)

Fall, 2014

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Approved By

________________	________________
Thesis Advisor	Chairperson
Dr. Anisul Haque	Dr. Halima Begum

ABSTRACT

HIT (Heterojunction with Intrinsic Thin layer) solar cells have attracted growing attention among all Si based PV technologies because of their prospect of further improvisation of efficiency and cost reduction. A high efficiency a-Si:H (n)/a-Si:H (i)/c-Si (p)/uc-Si (p+) HIT solar cell is simulated and studied here. AFORS-HET simulation tool is used for simulation purpose. In this thesis, the I-V characteristics and energy band diagram of HIT cell are analyzed. The impacts of the variations of emitter, intrinsic layer and substrate thicknesses on the photovoltaic characteristics of solar cell are discussed. We have varied the emitter, the intrinsic layer and the substrate thicknesses and observed that only the substrate thickness variation affects the conversion efficiency significantly. The increase of substrate thickness leads to increase of efficiency. We have simulated our HIT structure using optimized values of thicknesses. With the optimized parameters combination, this HIT cell reaches a high performance with conversion efficiency (η) of 24.25%, fill factor (FF) of 85.73%, open circuit voltage (V_{OC}) of 783.1 mV, and short circuit current density (J_{SC}) of 36.12 mA/cm^2.

ACKNOWLEDGEMENT

At first we are grateful to the Almighty Allah for giving us this opportunity to complete the thesis. And then we are grateful to our parents for their support.

Our sincere gratitude to the honorable supervisor, Dr. Anisul Haque, professor, Department of Electrical and Electronic Engineering (EEE), East West University (EWU), Dhaka for his regular guidance, supervision and constructive suggestions. Special thanks to the Chairperson of the department, Dr. Halima Begum, for every co-operation.

We would like to thank our honorable teachers, who have taught us to develop our understanding on subject matters throughout the process.

We also thank to all of our friends and well wishers for their moral support and helpful discussion during this thesis.

AUTHORIZATION PAGE

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

Solar energy can make an important contribution to meet the challenges posed by the ever-growing energy consumption worldwide. But the energy provided by solar cells is still a small fraction of the world energy needs. This fraction could be considerably increased by lowering solar cell costs which can be achieved by economizing the material and thermal budgets, as well as increasing cell efficiency.

Solar cell or photovoltaic cell is an electrical device that directly converts sunlight into DC electricity using the photovoltaic effect which was first discovered by Becquerel in 1839 [1]. From the beginning of 20^{th} century Silicon solar cell has been continuously paid attention as one of the important ways of harvesting solar energy. Silicon solar cells can be divided into two main groups: homojunction wafer-based crystalline silicon (c-Si) solar cells and thin-film silicon solar cells.

Homojunction wafer-based crystalline silicon (c-Si) solar cells are one of the main groups of Silicon solar cells. Standard cells are produced using monocrystalline and polycrystalline Si. The efficiencies with standard cell structures are in the range of 16–18% for monocrystalline substrates and 15–17% for polycrystalline substrates [2]. However, cost reduction is the main challenge for wafer-based c-Si solar cells due to the use of expensive wafers and the requirement of high temperature (~800-900°C) processing during junction formation. For these limitations thin-film silicon solar cells are introduced.

Thin-film silicon solar cells are another main group of Silicon solar cells which are based on hydrogenated amorphous silicon (a-Si:H) and hydrogenated microcrystalline silicon (c-Si:H). In comparison to wafer-based c-Si solar cells they provide low cost due to their low material consumption and low temperature (<600°C) processing. However, a low efficiency of around 6 to 9% is the main limitation for this technology resulting from the poor electronic properties of the absorbers [1]. Improvement of the efficiency of thin-film silicon solar cells is an essential requirement which is the reason for approaching heterojunction solar cells.

The heterojunction silicon solar cells are the combination of both wafer-based c-Si and thin-film silicon with different bandgap energies. It combines many advantages, such as lower temperature processing, higher efficiency, higher open circuit voltage, lower temperature coefficient etc.

1.2 LITERATURE REVIEW

The major goal of photovoltaic is the cost reduction of the generated energy and their world wide availability. One way to achieve this goal is the further improvement of the efficiency of the solar cells. Silicon based hetero-junction solar cells represent a possible concept for reaching the desired efficiency level.

The first crystalline silicon solar cell was fabricated in Bell Laboratory in 1953 with 4.5% efficiency [3]. Later in 1954 the efficiency was improved to 6% [3]. In early 1979 the amorphous silicon solar cell of multilayered p-i-n unit cell structure was developed with a high open voltage of 2.0 V [4].

The idea of using two different semiconductors to form a heterojunction was discovered in the late 1950s [1]. In 1974 Walther Fuhs and coworkers first fabricated heterojunction silicon solar cells, where the absorber is p (n) type c-Si, while the emitter n (p) a-Si:H layer is deposited by the standard plasma-enhanced chemical vapor deposition (PECVD) technique at ~200ºC in the University of Marburg, Germany [5].

In 1990 Japanese company Sanyo, which is currently part of Panasonic began work on the growth of low temperature junctions on c-Si and developed a new type of heterojunction solar cells called HIT, with high conversion efficiency [6]. They began commercial production of HIT solar cells in 1997 [1]. Their research has been continuously improved to yield an outstanding 23% efficiency by 2010 [7]. This innovation was possible for the introduction of thin films of intrinsic a-Si:H, BSF, the Transparent Conductive Oxide (TCO) and optimization of material and processing.

Inspired by the outstanding performance of Sanyo HIT cells, many research groups throughout the world have been working with these cells. The front surface of cells was textured in order to improve the conversion efficiency [8]. Also additional textured photonic crystal and backside reflector were fabricated at the back surface to ease the efficient light trapping [9]. Hetero-junction solar cells with textured surface have a high conversion efficiency of over 23% for laboratory cells and over 19.5% for mass production cells [7].

The forerunner of electrical modeling of a-Si:H solar cells was Hack and Shur and their work was published in 1985 [10]. Some other mentionable models for the simulation of solar cells are AMPS (Analysis of Microelectronic and Photonic Structures) by Fonash's group [11], the ASDMP (Amorphous Semiconductor Device Modeling Program) program by

Chatterjee [12], the ASA (Amorphous Semiconductor Analysis) program by von der Linden developed in 1992 [13] etc. Modeling of HIT cells was started by van Cleef in 1998 using the AMPS computer code, but this code does not have proper built-in optical model [14]. Then the numerical simulation software AFORS-HET (Automat for Simulation of Heterostructures) has been developed particularly for simulating HIT solar cells [15].

Having a large numbers of processing variables, like the thickness of the layers, the defect density, the band gap of the different layers etc, it is tough to scrutinize the effect of each variable on the performance of the solar cell experimentally. In such cases AFORS-HET provides a convenient way to evaluate the role of the various parameters present in the fabrication processing of HIT solar cells.

1.3 OBJECTIVE

This thesis is intended to optimize the high efficiency HIT Solar Cell through simulation where n-type amorphous Si and p-type crystalline Si layers are used as emitter and base respectively and an intrinsic amorphous Si buffer layer is embedded between them. And finally a microcrystalline Si layer is used as back surface field.

Our aim is to simulate, analyze and optimize the heterostructure using the simulation tool AFORS-HET. AFORS-HET is a generalized computer simulation tool for analyzing and designing the HIT (Heterojunction with intrinsic thin layer) solar cells. By using this software the values of open circuit voltage, short circuit current density, fill factor, efficiency and energy-band diagram of the structure can be determined.

1.4 ORGANIZATION OF THE THESIS

In chapter 2 essential reviews of HIT solar cell, basic HIT structure and the structure that we considered are discussed. Next in the chapter 3, a brief discussion about AFORS-HET and simulation of HIT cell with AFORS-HET are given. Then in chapter 4, results and discussions are presented. Finally in chapter 5, summary and conclusions, proposed work for the future are arranged.

CHAPTER 2

HIT SOLAR CELL

2.1 INTRODUCTION TO HIT SOLAR CELL

HIT solar cell is a structure in which a very thin intrinsic a-Si layer is deposited between p (n)-type a-Si and n (p)-type c-Si. The heterojunction combines the strengths of amorphous and crystalline silicon to create very efficient and stable device. This type of heterostructure was originally investigated for a low-temperature junction fabrication technique. These structures have raised growing attention among all Si based PV technologies because of their prospect of further improvisation of efficiency and cost reduction.

Crystalline wafer is the base of HIT cells whereas the emitter and intrinsic layer are made of amorphous Si. The crystalline silicon has high efficiency, but it is costly. The cost reduction and growing efficiency of HIT solar cells mainly depends on the properties of the deposited hydrogenated amorphous silicon (a-Si:H) on the crystalline silicon (c-Si) [1]. The main advantages of amorphous silicon are: excellent passivating properties, a low temperature and large area deposition, high absorption coefficient and low cost. The amorphous layers can be deposited on the wafer using plasma enhanced chemical vapor deposition (PECVD) which is a relatively low temperature deposition method [1]. The p (n)-type a-Si emitter layer forms the p-n junction in the cell, which creates the desired band bending in the c-Si wafer close to the a-Si:H/c-Si interface and thereby enables charge separation.

The thin intrinsic a-Si buffer layer plays an important role in the performance of the HIT cell. Actually, it is this layer that gives name “HIT”. This thin intrinsic amorphous silicon layer between the doped amorphous layer and the crystalline wafer increases the open circuit voltage (V_{OC}) markedly [16]. Besides, this layer passivates c-Si surface defects effectively and passes carriers through the passivating layers without significant loss [17]. There are also TCO layers and metal electrodes on both sides of HIT cell. The TCO layer serves as an antireflection coating and reduces series resistance losses. Some results show that the a-Si/c-Si heterojunction is hypersensitive to the TCO work function and it should be large enough to achieve high conversion efficiency [18].

Altogether HIT solar cells provide several advantages, such as, (1) excellent surface passivation which plays important roles in heterojunction solar cell performance, (2) low processing temperature (~200°C) resulting in low thermal budget, (3) higher efficiency, the best reported efficiency is 23%, (4) higher open circuit voltage, the best recorded open-circuit voltage is above 700 mV, (5) a lower temperature coefficient describing the reduction of performance with increasing temperature, and (6) reduced material cost leading to overall cost reduction [7], [19].

2.2 BASIC HIT CELL STRUCTURE

The basic structure of HIT cell is shown in Figure 2.1. Sanyo had focused on this (p-a-Si:H/n-c-Si) HIT structure. This cell is fabricated with n-type c-Si wafer of thickness ~200 µm. The p-n junction is formed by the deposition of intrinsic a-Si and p-type a-Si layers on the n-type c-Si substrate. Finally on the top of the doped a-Si layer, TCO layer and metal electrode are formed. All processes are done at temperature below 200 ºC. HIT solar cell with this structure gives a conversion efficiency of around 18% [16].

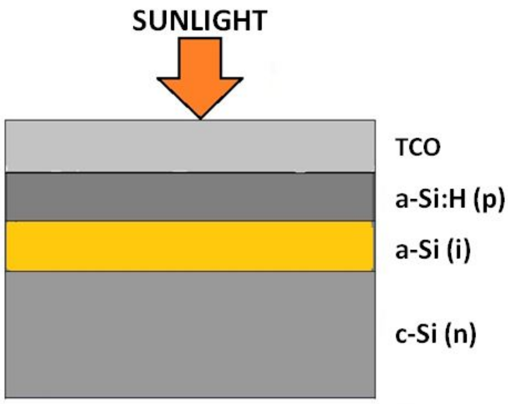

Figure 2.1: Schematic diagram of a basic HIT cell.

The energy-band structure of the basic n-type c-Si heterojunction cell at thermal equilibrium condition is shown in Figure 2.2. Here, E_{c1} and E_{V1} are the conduction band and valance band energies of a-Si (p) layer. E_{c2} and E_{V2} are the conduction band and valance band energies of c-Si (n) wafer. At the front side the a-Si:H layer is shown as a wide bandgap layer of 1.72 eV that acts as the semi permeable membrane over c-Si of bandgap 1.1 eV. ΔE_c and ΔE_V are band offsets at conduction and valence bands, respectively. The exact values of those offsets are difficult to measure. The early reported values were 0.1 eV for ΔE_c and 0.4 eV for ΔE_V, and recent measurements have generally agreed well [5]. At the emitter side, the low ΔE_c allows electrons to move into the c-Si substrate and the high ΔE_V blocks holes at the interface. Thus the high ΔE_V prevents holes from moving freely to the c-Si substrate. So the n-type c-Si heterojunction is nearly ideal for electron collection.

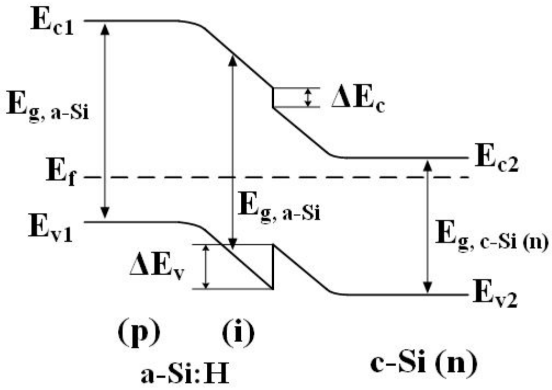

Figure 2.2: Energy-band structure of a basic HIT cell.

2.3 OUR HIT CELL STRUCTURE

Figure 2.3 represents the HIT cell a-Si:H (n)/a-Si:H (i)/c-Si (p)/µc-Si (p+) under our consideration. In this HIT solar cell a p-type c-Si wafer of thickness 30 µm is used as the absorber. An intrinsic a-Si layer of thickness 3 nm is deposited on c-Si wafer for forming a good HIT cell. On the front side of the cell, a-Si:H of thickness 5 nm is deposited with opposite doping type to the c-Si wafer. It is called the emitter layer. The role of this emitter layer is to collect electrons. Finally on the back side of the cell, a µc-Si of thickness 5 nm with the same type of doping as the c-Si wafer is deposited as the back surface field (BSF). This BSF layer collects holes. We use 1.72 eV for band gap of a-Si:H layer. Band gap of bulk c-Si is 1.12 eV and that of µc-Si BSF is 1.5 eV [20].

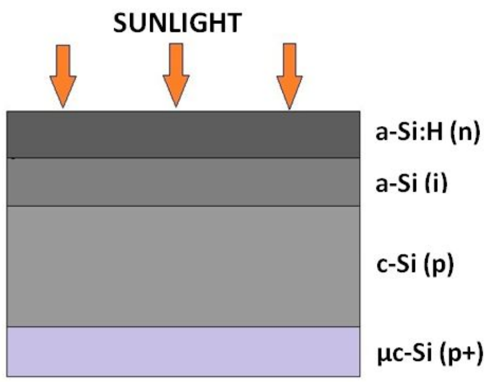

Figure 2.3: Schematic diagram of HIT cell.

CHAPTER 3

SIMULATION USING AFORS-HET

3.1 INTRODUCTION TO AFORS-HET

In order to investigate heterojuntion solar cells, different types of electrical simulation tools were developed, AFORS-HET is one of the preferable tools. It is a simulator program and typical characterization method for heterojunctoin as well as homojunction solar cells [1]. This software was first introduced by Helmholtz-Zentrum Berlin. AFORS-HET is now widely used for simulation purpose.

For electron and hole generation rate due to photon absorption, two categories of generations are considered which are super bandgap generation (where, $E_{ph} \geq E_g$) and sub bandgap generation (where, $E_{ph} \leq E_g$) [1]. The visible-light portion of the electromagnetic radiation spectrum consists of photons, each of which contains a particular amount of energy that depends on the wavelength. AFORS-HET simulation calculation module is divided into 2 parts, namely, optical simulation and electrical simulation.

1. **Optical Simulation:** Optical modeling can only calculate the super-band gap generation rate as it is independent of the local particle densities. Two types of optical models are implemented in AFORS HET: Lambert-Beer absorption and the coherent/incoherent internal multiple reflections [1].

   The optical generation rate can be calculated from equation (3.1),

   $$G(x,t) = G_n(x,t) = G_p(x,t) \tag{3.1}$$

   Where, $G(x,t)$ is super bandgap electron-hole generation rate [1].

2. **Electrical Simulation:** Sub-band gap generation can be calculated within the electrical modeling part as it depends on the local particle densities. Here, an arbitrary stack of semiconductor layers are modeled. For all these layers, Poisson's equation and continuity equation for electrons and holes have to be solved to perform the electrical simulation [1].

   Poisson's equation is expressed as (3.2),

   $$\nabla^2\phi = -\frac{\rho}{\epsilon} \tag{3.2}$$

Where, ϵ is the electric permittivity of silicon, ϕ is the electric potential across the interface and ρ is the local charge density [1].

And the one dimensional continuity equation for transport of electrons is,

$$-\frac{1}{q}\frac{\partial j_n(x)}{\partial x} = G_n(x) - R_n(x) - \frac{\partial n(x)}{\partial t} \quad (3.3)$$

With,

$$j_n(x) = q\mu_n n(x)\frac{\partial E_{Fn}(x)}{\partial x} \quad (3.4)$$

$$E_{Fn}(x) = E_c(x) + \mathrm{kT}\, ln\left(\frac{n(x)}{N_c(x)}\right) \quad (3.5)$$

For transport of hole,

$$\frac{1}{q}\frac{\partial j_p(x)}{\partial x} = G_p(x) - R_p(x) - \frac{\partial p(x)}{\partial t} \quad (3.6)$$

With,

$$j_p(x) = q\mu_p p(x)\frac{\partial E_{Fp}(x)}{\partial x} \quad (3.7)$$

$$E_{Fp}(x) = E_v(x) - \mathrm{kT}\, ln\left(\frac{p(x)}{N_v(x)}\right) \quad (3.8)$$

Where, $j_n(x)$ and $j_p(x)$ are electron and hole currents respectively, E_{Fn} and E_{Fp} are the quasi-Fermi levels of electrons and holes respectively, μ_n and μ_p are electron and hole mobility respectively, $R_n(x)$ and $R_p(x)$ are recombination rates of electrons and holes respectively, $\mathrm{E_c}$ and $\mathrm{E_v}$ are conduction and valence band energies respectively and N_c and N_v are effective density of states in conduction and valence bands respectively [1].

AFORS-HET provides various advantages to its user, such as [1]:

- It is capable of modeling an arbitrary sequence of semiconducting layers.
- It can include the interface defects that enable it to calculate both bulk recombination and interface recombination.
- Here, two external boundaries of the semiconductor stack (the front and back contact) can be calculated as Schottky boundary, insulator boundary or metal/insulator/semiconductor boundary, which means different experimental configurations can be modeled.
- In addition, a variety of characterization methods can be simulated, such as current voltage (I-V), internal and external quantum efficiency (QE), capacitance-voltage (C-V), capacitance-temperature (C-T) and capacitance-frequency (C-f).
- This program allows for simulated arbitrary parameter variations to match with real measurements.

3.2 SIMULATION OF HIT SOLAR CELL

Simulation of an a-Si:H/c-Si solar cell is a demanding task due to the advanced physics in models and the large number of material parameters involved. We do the simulation with a device temperature of 300 K. In our simulation process, the solar AM1.5 radiation was adopted as the illumination source with a power density of 100 mW/cm^2. For all of the layers the optical bandgap and the layer density are set as 1.124 eV and 2.328 gcm^{-3} respectively. The thermal velocities of both electrons and holes are set as 10^7cm/s [20]. Other parameters used in the simulation are given in Table 3.1.

Table 3.1: The parameters used for HIT solar cell simulation.

Parameters	**a-Si (n)**	**a-Si (i)**	**c-Si (p)**	**uc-Si (p+)**
Thickness (nm)	5	3	30000	5
Dielectric constant	11.9	11.9	11.9	11.9
Electron affinity (eV)	3.9	4	4.05	4
Bandgap (eV)	1.72	1.72	1.12	1.5
Effective conduction band density (cm^{-3})	10^{20}	10^{20}	2.8×10^{19}	10^{20}
Effective valence band density (cm^{-3})	10^{20}	10^{20}	1.04×10^{19}	10^{20}
Electron mobility (cm^{2}V^{-1}s^{-1})	5	5	1041	10
Hole mobility (cm^{2}V^{-1}s^{-1})	1	1	412	3
Acceptor concentration (cm^{-3})	0	0	1.5×10^{16}	10^{17}
Donor concentration (cm^{-3})	2.49×10^{19}	100	0	0

Different input parameters are used to simulate the energy-band diagram and the I-V characteristics of the HIT solar cell that we have considered. Figure 3.1 is a screenshot of parameter input window in AFORS-HET.

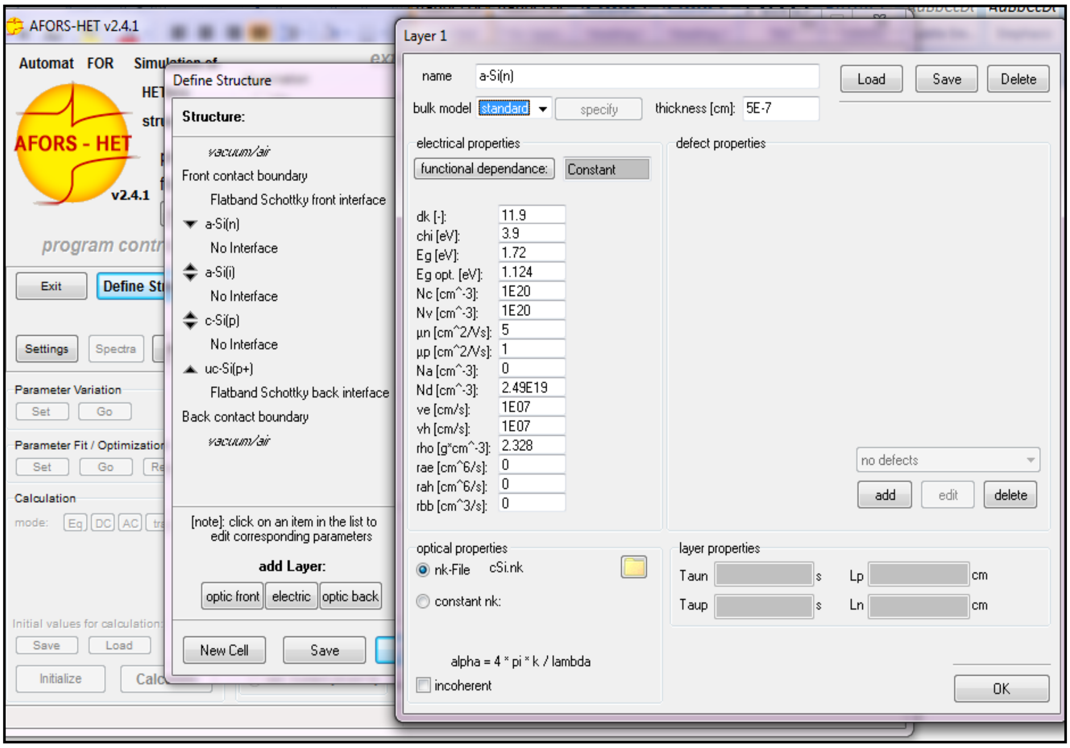

Figure 3.1: Screenshot of AFORS-HET parameter input window.

After defining the structure in AFORS-HET, a number of I-V characteristics are simulated by changing different layer thicknesses. The layer thickness of emitter is varied from 3 nm to 10 nm. Similarly, the thickness of the intrinsic layer is varied from 2 to 6 nm. Finally the thickness of the wafer is varied from 30 to 200 µm. Then the values of V_{OC}, J_{SC}, fill factor (FF) and efficiency (η) are determined.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 CURRENT-VOLTAGE CHARACTERISTIC

The I-V curve shown in Figure 4.1 is related with the current produced by the HIT cell to the voltage across it for AM1.5 incident light. The simulation is performed with the parameters of Table 3.1. From the I-V diagram it is shown that as voltage is increased across the solar cell, current initially reduces slowly and there comes a point when the current drops rapidly. The open-circuit voltage (V_{OC}) is the maximum output voltage of the cell at zero current. The short-circuit current (J_{SC}) is the maximum current through the cell when the voltage across it is zero. Short-circuit current is the photo-current due to the generation and collection of light-generated carriers.

The photovoltaic properties are V_{OC} =783.1 mV, J_{SC} =36.12 mA/cm^2, FF =85.73% and η =24.25%.

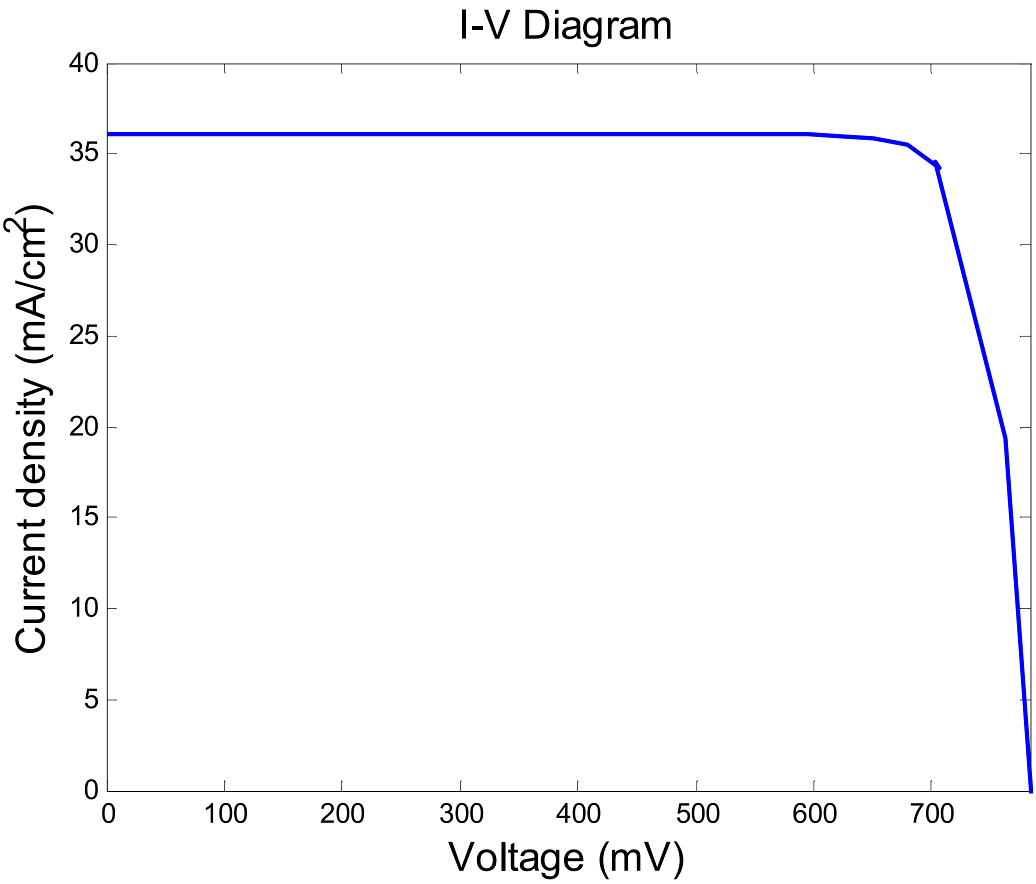

Figure 4.1: The illuminated J-V characteristic under AM1.5 light.

4.2 ENERGY-BAND DIAGRAM

Figure 4.2 is the simulated energy-band diagram of our HIT structure without illumination. It is seen in the energy-band diagram that, a high potential barrier is formed at the valence band and a low potential barrier is formed at the conduction band at the interface between the absorber and the thin BSF layer.

Figure 4.3 is the energy-band diagram under illumination where Fermi level (E_f) is splitted into Quasi Fermi energy of holes (E_{fp}) and Quasi Fermi energy of electrons (E_{fn}). The separation between E_{fp} and E_{fn} represents $V_{OC.}$

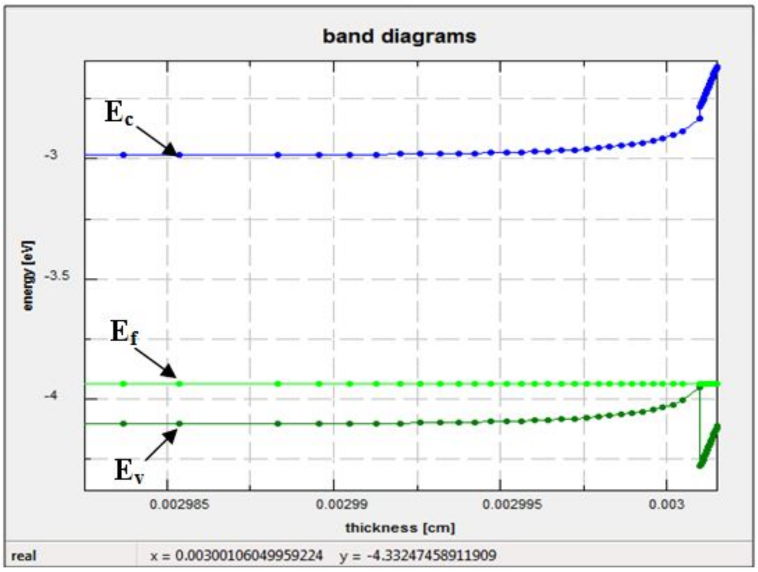

Figure 4.2: The energy-band diagram of HIT cell without illumination.

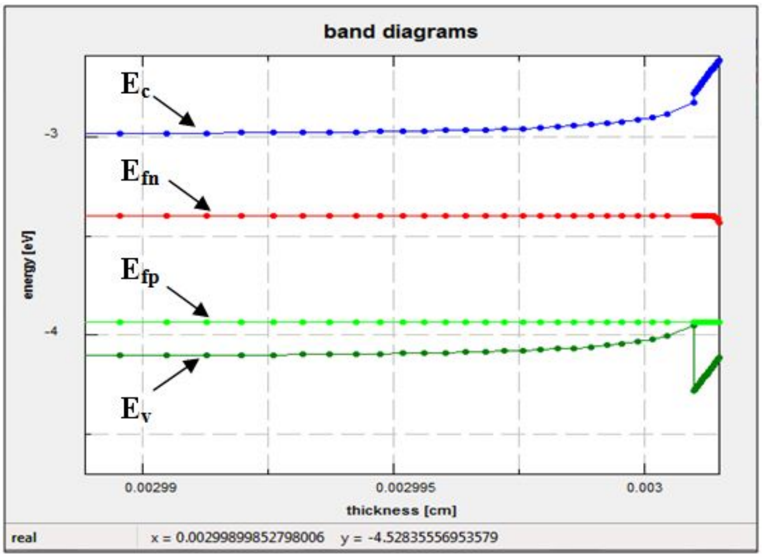

Figure 4.3: The energy-band diagram of HIT cell under AM1.5 light and short-circuit condition.

4.3 OPTIMIZATION OF HIT SOLAR CELL

4.3.1 OPTIMIZATION OF THE EMITTER THICKNESS

Figure 4.4 shows the influence of emitter thickness on the photovoltaic properties of HIT cell. From Figure 4.4 it can be seen that when the emitter thickness increases, the open circuit voltage is unchanged, while the short circuit current is reduced a little. This is because when the emitter thickness increases, the absorption of the photons in the emitter has increased. Thus the photo-induced carriers are interrupted to reach the edge of space charge region and contribute to reduced current. Fill factor decreases because of increasing series resistance with the increase of n layer thickness [20]. Hence the efficiency also reduces. But the changes in all the properties are relatively small which can be neglected with the variation of the emitter layer thickness. Therefore considering conversion efficiency, the emitter thickness may be chosen at about 5 nm.

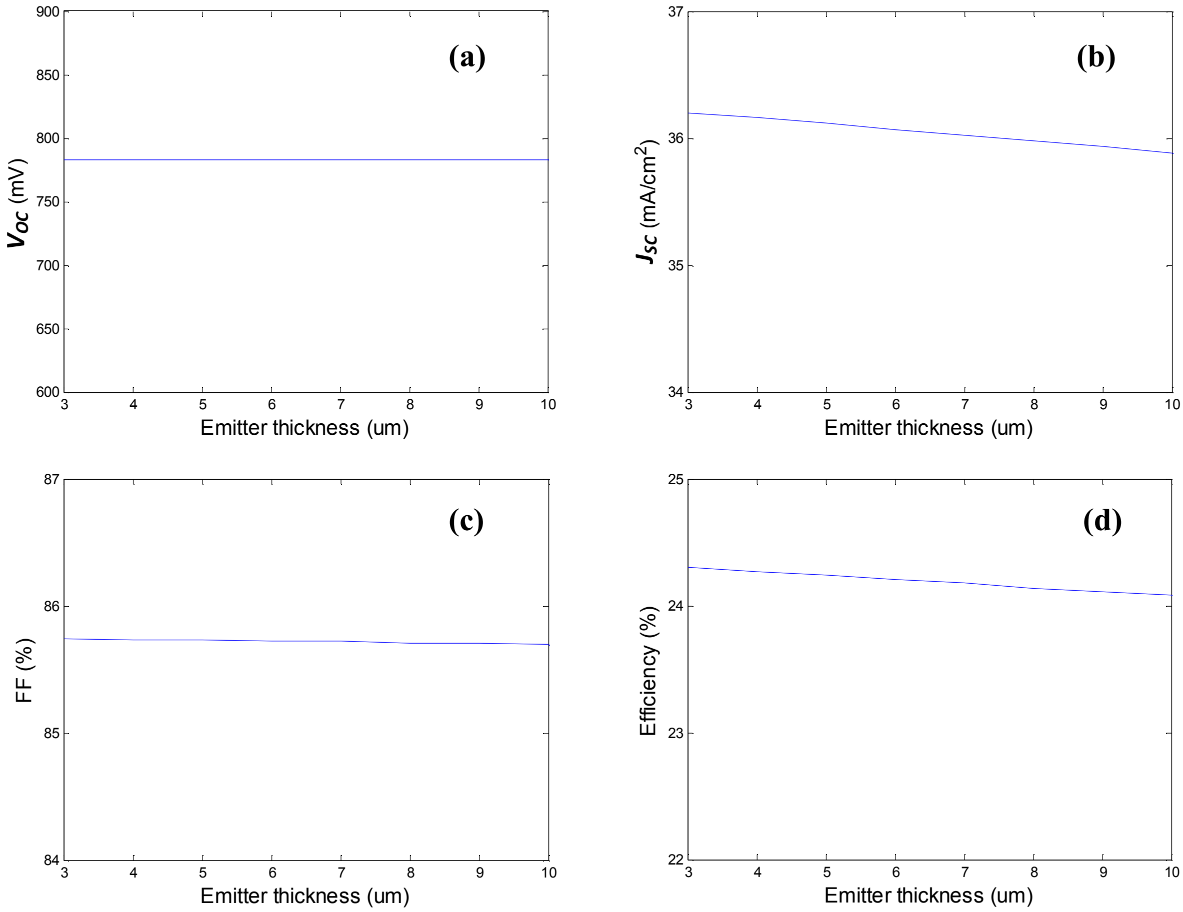

Figure 4.4: The impact of emitter thickness on (a) V_{OC}, (b) J_{SC}, (c) FF and (d) η of HIT solar cell.

4.3.2 OPTIMIZATION OF THE INTRINSIC LAYER THICKNESS

In Figure 4.5, we can see that with the increase of intrinsic layer thickness, the open circuit voltage keeps unchanged, while the short circuit current density decreases slightly because the light-induced carriers cannot be effectively collected when intrinsic layer thickness increases. Fill factor remains almost unchanged where conversion efficiency decreases slightly. As the intrinsic layer thickness should be as thin as possible, the optimum intrinsic layer thickness can be set at 3 nm.

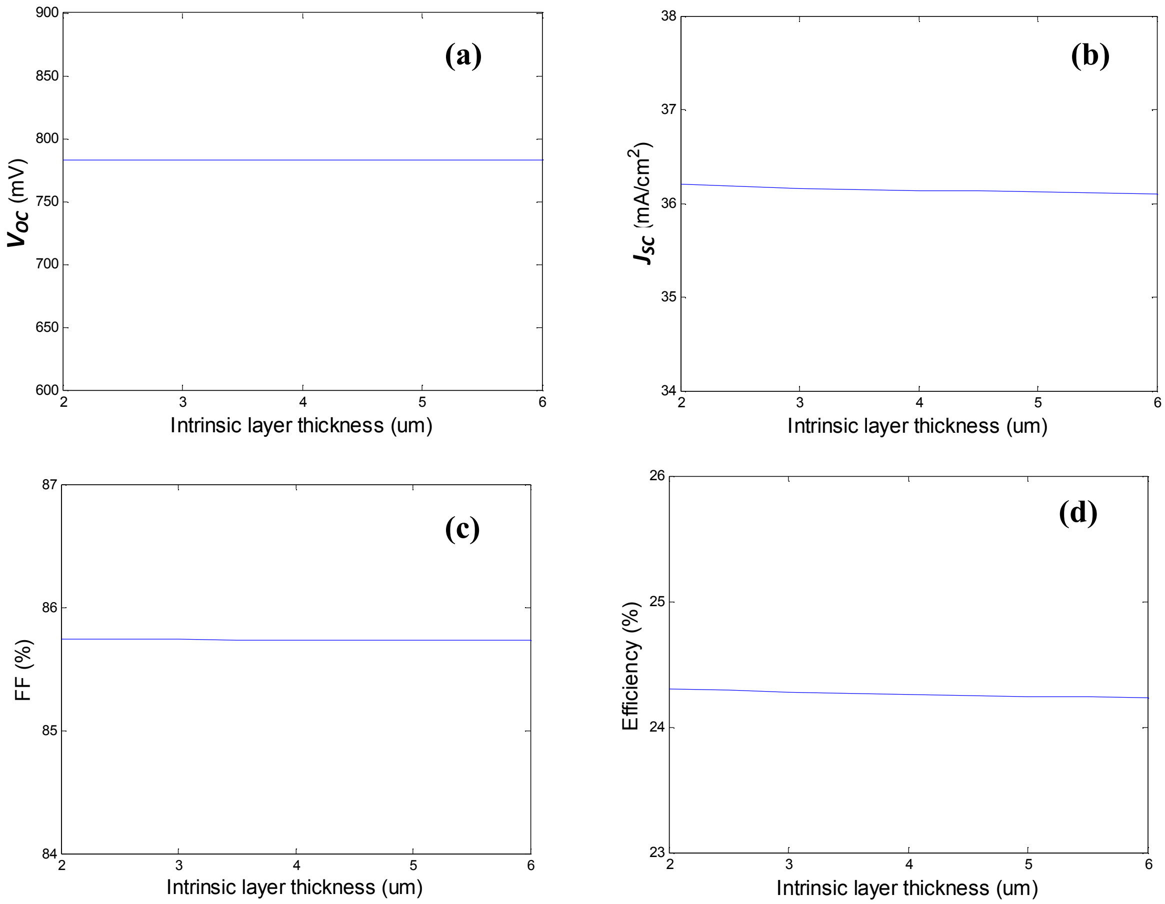

Figure 4.5: The impact of intrinsic layer thickness on (a) V_{OC}, (b) J_{SC}, (c) FF and (d) η of HIT solar cell.

4.3.3 OPTIMIZATION OF THE SUBSTRATE THICKNESS

From Figure 4.6 we can see that when the thickness increases, the open circuit voltage increases slightly. But the short circuit current increases significantly and as a result cell efficiency is also increased. It is very beneficial but the cost is increased a lot because this increment of efficiency requires large amount of expensive c-Si in the substrate. For the increment of efficiency by 4%, the layer thickness is increased by 7 times.

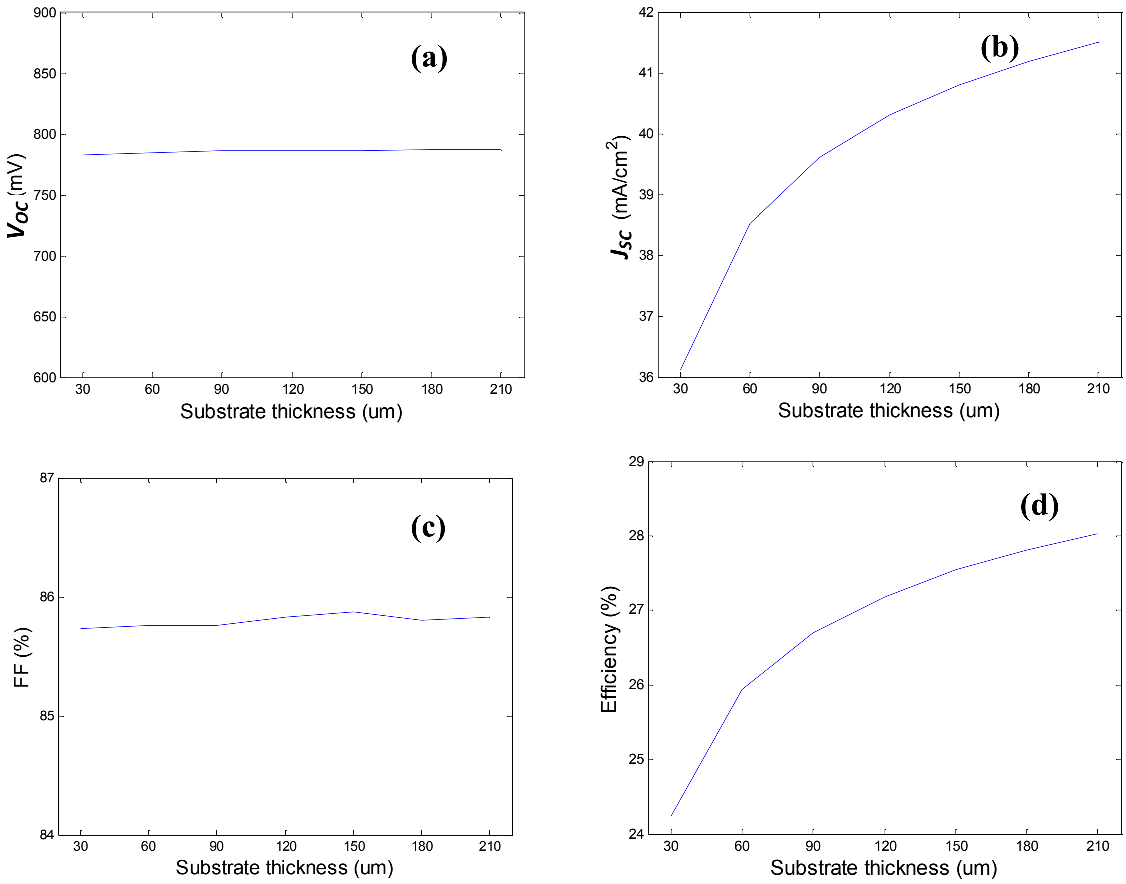

Figure 4.6: The impact of substrate thickness on (a) V_{OC}, (b) J_{SC}, (c) FF and (d) η of HIT solar cell.

CHAPTER 5

SUMMARY

5.1 CONCLUSIONS

In our study a HIT solar cell on p-type c-Si absorber is simulated with the simulation software AFORS-HET 2.4.1 where the emitter is hydrogenated n-type a-Si. This type of solar cell has drawn attention because it offers a simple and less expensive technology. It combines wafer technology with thin-film techniques which is capable of large area deposition and allows low process temperatures.

In HIT cell structure a-Si emitter performs the electron-hole separation created from incident light photons. All the holes are absorbed in the c-Si substrate. We have observed that the introduction of thin intrinsic amorphous silicon layer between a-Si (n) and c-Si (p) layers mainly increases the short-circuit current density which leads to increase of efficiency.

We have also optimized the device structure. We have varied the thickness of emitter from 3 nm to 10 nm and the thickness of the intrinsic layer is varied from 2 to 6 nm. But these two variations do not bring any significant change on photovoltaic characteristics. So, 5 nm and 3 nm are considered as optimum for the emitter thickness and the intrinsic layer thickness respectively. Finally we made a sequence of changes to the p-type substrate to better understand what factors control V_{OC}, J_{SC}, FF and η by varying the thickness from 30 μm to 200 μm. A large change has been observed from this variation. The more we increase the wafer thickness the higher the efficiency becomes. If we consider the wafer thickness 200 μm, an efficiency of 28.03% can be obtained with V_{OC} of 787 mV. But large amount of c-Si is necessary in the substrate for this increment of efficiency which is cost expanding.

After the simulation of the structure with optimized parameters, we found that this HIT cell has a high η of 24.25%, FF of 85.73%, V_{OC} of 783.1 mV, and J_{SC} of 36.12 mA/cm^2.

5.2 FUTURE SCOPE OF WORK

This thesis is only limited in simulation of few photovoltaic characteristics in a simple HIT structure. Further extension of our work can be done more precisely and comprehensively. We have simulated the HIT structure with only a n-type a-Si, an a-Si thin intrinsic layer, a p-type c-Si and a μc-Si BSF layer. This simulation can be performed in a more complex structure with multiple junctions and layers. For more realistic result defect density can be included as good passivation of these defects is the key to attain high efficiency in these structures. TCO should be also included so we will be able to observe the effect of TCO work function.

The impact of amorphous/crystalline valence band discontinuity can be observed. Tunneling current analysis and multi-tunneling phenomenon are not analyzed in our work. But these phenomena have a crucial impact on HIT structure as they are important form of charge transport in heterojunctions. HIT cell output is also influenced to some extent by the minority carrier lifetime in c-Si wafer and it can be studied in our work.

For an eventual future utilization of this kind of solar cells in electrical power generation, more research is needed.

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