Influence of Interface Trap States and Quantum Mechanical Effects on the Drain Current of III-V Semiconductor MOSFETs

By

Mohammad Atif Bin Shafi

Subrata Sutradhar

Kaushik Debnath

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Thesis Advisor	Chairperson
Dr. Anisul Haque	Dr. Khairul Alam

Abstract

Effects of interface trap charges and quantum mechanical correction have been incorporated into the I-V characteristic of III-V semiconductor MOSFETs. MOS structures fabricated on III-V semiconductors are proving to be one of the most attractive replacements of currently used Si based MOSFETs. $In_{0.53}Ga_{0.47}As$ channel transistors show immense potential in that field and hence used in this paper as the channel material of concern. An extracted version of density of interface trap states is used in order to make the analysis more practical. A physically based explicit analytical model for the QM correction has been used. Effects of interface trap states on the drain current have been included via a surface potential based analytical model. Degradation of mobility due interface charges is also considered. However influence of interface states due to variation of voltage across drain and source and existence of parasitic resistances and capacitances have been ignored. Analyzing I-V characteristics has given some staggering results where the drain current in saturation reduces to even 98.6% from the ideal condition. Subthreshold swing also showed some significant changes. Incorporating QM correction does not change the subthreshold swing much as expected but interface states drastically degrades the swing.

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Approval

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Supervisor

_____

Professor Anisul Haque

Department of Electrical and Electronic Engineering

East West University, Dhaka-1212, Bangladesh

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Mohammad Atif Bin Shafi

Subrata Sutradhar

Kaushik Debnath

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Chapter 1

Introduction

In 1948 three American physicists, Shockley, Bardeen and Brattain invented bipolar transistor at the Bell Laboratories which is arguably one of the greatest invention in 20^{th} century [1]. This device, along with it's field-effect counterpart, has had enormous impact on virtually every era of modern life.

Over the past decade, the complexity of MOS IC's has redoubled at an astonishing rate. The diminution of transistor dimensions has allowed for an exponential increase with time in the number of components per chip and its operational speed [2]. At the same time more complex phenomena such as short channel effects, effects of interface states and Quantum Mechanical (QM) effects have started to play vital roles in terms of performance of the MOSFETs. The interface states although are not of significance in case of thicker gate oxides, but study of devices with gate oxide thickness ($\leq$ 2nm) shows that these almost negligible states have remarkable impact on the drive current [3]. Earlier this effect was barely noticeable, but the introduction of nanotechnology has made possible MOSFET's with ultra-thin oxides. QM correction is another phenomenon which was neglected in the early days but as the device technology progresses into the deep submicron regime, with higher semiconductor substrate doping and high surface electric fields, QM effects have become a significant part of modern devices.

In this work, both, Quantum Mechanical effects and effects of interface states, have been incorporated and I-V characteristics of MOSFET are analyzed. Currently used Si MOSFETs are reaching to the limit of scaling process and high mobility channel materials (e.g. III-V materials) are highly regarded as a replacement. In this work, we will consider $In_{0.53}Ga_{0.47}As$ MOSFET and study the I-V characteristics of the device. Results will be discussed analyzed.

1.1 Background

With continual scaling of CMOS technology classical physics is meager to explain the behavior of a MOSFET. For modern day physics, where the metal-oxide-semiconductor (MOS) devices are down-scaled to the nanometer regime, interface trap charges and QM effects have become an essential part.

Interface trap charge exists at the oxide semiconductor interface. It is caused by the defects at the interface, which gives rise to charge "traps"; these can exchange mobile carriers with the semiconductor, acting as donors or acceptors. When interface traps are present, more charges on the gate are necessary to create a given surface potential. When a voltage is applied across the metal and the semiconductor, the interface trap levels move up or down in energy with the valence and conductance bands while the Fermi level remains fixed. A change of charge in an interface trap occurs when it crosses the Fermi level.

To obtain high density integration for MOS devices, it is necessary to reduce the gate oxide thickness and increase the substrate doping concentration. This results in a narrow and deep potential well. Electrons get confined at the semiconductor-insulator interface and it becomes necessary to take QM effects into consideration [4-9]. In the state-of-the-art MOSFET's due to increased vertical electrical field the carrier energy quantization has become significant. The energy quantization and the shift of the inversion charge centroid delays the formation of inversion charge (threshold voltage (V_{th}) shift) and reduces the current driving capability (increase the effective oxide thickness). QM effects also result in an increase in the magnitude of ψ_s for a given gate overdrive voltage.

The growing demand to gauge QM effects into the device has led numerous universities and institutions merge their efforts in to develop QM simulators. At the moment, we differentiate between two categories of device models namely numerical device simulation models and compact models. Numerical device simulation is used when there a need of precise and detailed information about the device performance. It requires rigorous computation and huge amounts of memory as it takes in to account various details (such as external electrical, thermal or optical boundary conditions) of the structure [10]. Classical models describe the terminal properties of the device by means of a simplified computationally efficient set of equations. So many researchers have tried to integrate QM effects into the classical models for device and circuit level simulation using empirical analytical expressions. This approach is term as QM correction.

CMOS has enjoyed decades of prosperity with reliance on core materials, such as silicon for the transistor channel, and silicon dioxide for the gate dielectric. But due to the continuous scaling of the transistors, Si MOSFETs are nearly reaching its fundamental limits. Focus has shifted during the last decade with the introduction of new materials, such as silicon germanium for the ohmic contact region of p-channel transistors, and hafnium-based gate dielectrics to improve device performance and energy efficiency. Truly revolutionary changes may still lie ahead with the

envisioned replacement of the very essence of CMOS: the silicon channel. Besides alternative channel materials, such as germanium and rather exotic options like graphene, future CMOS generations may finally draw momentum from a rather unlikely contender: III-V semiconductors [11], which have been used in commercial applications, such as communications and optoelectronics, for years.

III-V compound semiconductors are becoming increasingly important for a wide range of potential applications such as optoelectronic devices and high-speed, low-power logic applications, owing to their high electron mobility, direct bandgap, and high breakdown voltages [12]. Nearly all these devices employ oxide-semiconductor, metal-semiconductor, or semiconductor-semiconductor interfaces.

$In_{0.53}Ga_{0.47}As$ is a convenient III-V compound semiconductor for n-type MOSFET channel material due to its high electronic mobility (~14,000 $cm^2 V^{-1} s^{-1}$), high breakdown field, and its ability to be grown lattice matched on the semi-insulator substrate, InP. Therefore among many of the III-V materials, InGaAs is found to be the most attractive one to replace Si n-type MOSFETs, due to its improved performances [13].

1.2 Literature review

For the past 40 years, the semiconductor industry and academia have relentlessly pushed transistor scaling. Along with scaling, the MOSFET transistor evolved from the P-ch MOSFET in the 1960's to the N-channel MOSFET in the 1970's. A good understanding of gate oxide quality, such as interface traps, fixed and mobile charges, and a good control of gate oxide quality in a manufacturing environment enabled industry to make the transition from PMOS technology to a higher-performing NMOS technology in 1970's. In addition the experiment in improving the device performance has been continued and it has been achieved through the gradual replacement of silicon by III-V semiconductor. The indium gallium arsenide semiconductor is a prominent semiconductor and can be a very good replacement of silicon and can give a powerful performance as electronic devices. The III-V material is of a great interest because of its high electron mobility over silicon.

In the early 1980s, CMOS became the technology of choice for general-purpose integrated circuit applications. The designers rely on the simulation of their design before building a prototype. To simulate a circuit, simulators make use of element models, which provide a mathematical description of the element behavior in the circuit. The compact MOSFET models provide most of the designers with the essential information concerning electrical properties of the components associated with the manufacturing process of the chip.

Introducing interface trap charges into the calculation has its own short story. Different approaches were made over the period of time. A theoretical treatment on the process of hot electron emission from silicon into SiO_2 was carried out by Ning [14]. He considered avalanche and non-avalanche injection mechanism to calculate emission probability of the carriers at Si/SiO_2 interface. Yamabe and Miura [15] observed experimentally the flat band voltage shift due to the generation of interface states because of electron trapping in the SiO_2 film. They suggested that the interface states, where electrons can be trapped, are generated due to the collisions of electrons at the Si/SiO_2 interface. Khosru and others [16] observed that holes are created by ionizing radiation that produces new electronic states at the $Si\text{-}SiO_2$ interface resulting in the formation of interface traps. They also found a threshold voltage shift due to the trapping of carriers inside the SiO_2 layer. In a recent approach, Wen, Li and Wu [17] showed that the generated electron traps at the Si/SiO_2 interface enhance the degradation of MOSFET characteristics. To determine the interface trapped charges in a Si/SiO_2 interface Goreseneken and others [18] used the charge pumping method introduced by Brugler and Jespers [19] and presented a very keen analysis of energy distribution of interface trapped charges.

Quantum mechanical correction involved much more difficulties as it steps ahead from semi-classical regime. Accurate modeling of energy quantization in MOSFETs requires the solution of the Schrödinger and Poisson equations [20-23]. One of the approaches to model the quantum mechanical problem is to use approximations in solving these equations. These equations upon solving give the energies and the surface potentials which are caused by the energy quantization process in the channel. These are then used to obtain the inversion charge densities further giving the accurate analytical equations for C-V and I-V analysis in sub 100 nm MOSFETs. Furthermore, analytical solutions are preferable because of their simplicity and fast computational speed. With these analytical solutions, it becomes easier to predict device scalability and circuit performance for future technology generations. The other approach to tackle energy quantization problem is the numerical approach which deals with the actual self-consistent solution (i.e. compatible to a large extent with the solution of each other or with a minimum error in solution matching) of the Poisson's and the Schrödinger's equations. These can be solved in both one dimension and two dimensions. The one-dimensional modeling primarily involves the analysis of the quantization of the energy levels and the variation of the surface potential only in the transverse direction i.e. along the depth of the channel or normal to the oxide/silicon interface. In this, the Poisson's and the Schrödinger's equations are solved only in one dimension. Traditional modeling approaches have been of one dimension self-consistent solving of Poisson's - Schrödinger's equations. This type of modeling approach is not sufficient to analyze the MOSFET at high drain voltages at which the two dimensional short channel effects such as drain induced barrier lowering etc. are prominent. Only at very low drain voltages analysis can be done using one dimension modeling [24]. The two-dimensional modeling approach which is more complex, considers the quantization of the energy levels and the variation of the potential in the transverse as well as in the

longitudinal directions. In this, the Poisson's and the Schrödinger's equations are solved in the direction normal to the oxide/silicon interface and also along the channel [23]. Numerical solutions are obtained by solving Schrödinger equation and the Poisson equation using iterations. It is not used as an approach in standard circuit simulators because of its complexity and more computationally intensive due to iterative solutions but used as a reference because of its high accuracy.

MOSFETs based on III-V semiconductors promise to combine III-V high frequency performance with scalability and integration known from silicon. InGaAs MOSFET technology may find future use in low power logic circuits. The technology may also have a unique advantage in regard to integration. For CMOS applications, novel device architectures, high-κ gate dielectrics, metal gates and high mobility channel materials will be required to continue CMOS device scaling according to Moore's Law and the ITRS. Modern CMOS applications prefer single supply operation using enhancement-mode (for a definition, see [26]) FETs. The GaAs enhancement-mode MOSFET, however, has remained elusive for decades [27]. Recent developments including the discovery of the low defect Ga_2O/GaAs interface [28], [29], the use of GdGaO/Ga_2O_3 dielectrics [30]-[32] and suitable epitaxial layer structures [33], and the invention of an implant free MOSFET design [34], [35] have finally delivered GaAs enhancement mode devices which realize their performance potential. Recent study shows significance of InGaAs [13]. InGaAs is an alloy of gallium arsenide and indium arsenide. In a more general sense, it belongs to the InGaAsP quaternary system that consists of alloys of indium arsenide (InAs), gallium arsenide (GaAs), indium phosphide (InP), and gallium phosphide (GaP). As gallium and indium belong to Group III of the Periodic Table, and arsenic and phosphorous belong to Group V, these binary materials and their alloys are all III-V compound semiconductors. The InAs/GaAs alloy is referred to as $In_xGa_{1-x}As$ where x is the proportion of InAs and 1-x is the proportion of GaAs. The challenge is that while it's possible to make thin films of $In_xGa_{1-x}As$ by a number of techniques, a substrate is required to hold up the thin film. If the thin film and the substrate do not have the same lattice constant, then the properties of the thin film will be severely degraded.

For lots of reasons, the most convenient substrate for $In_XGa_{1-X}As$ is InP. High quality InP substrates are available with diameters as large as 100 mm. $In_xGa_{1-x}As$ with 53% InAs is often called "standard InGaAs" without bothering to note the values of "x" or "1-x" because it has the same lattice constant as InP and therefore the combination leads to very high quality thin films [36].

1.3 Objective

Our objective behind this work is to analyze and understand the influence of Quantum Mechanical correction and interface states on the drain current of $In_{0.53}Ga_{0.47}As$ MOSFET.

For distribution of interface trap charges we have used the D_{it} – energy relationship extracted in [37]. And for QM correction, Karim model [25] has been used. Few minor modifications, to keep the model consistent with $In_{0.53}Ga_{0.47}As$, have been made which will be discussed at chapter 5.

Changes in I-V characteristics including these secondary effects, QM correction and interface states, will be analyzed. The resultant sub-threshold swing will also be calculated. Degradation of mobility due to interface states has also been incorporated to make the results more meaningful.

1.4 Organization of the thesis

In chapter 2, reviews of basic MOS physics and charge sheet model are discussed. In the following chapter 3, a brief explanation on QM effects and interface states and their theoretical derivations are given. Then in chapter 4, effects of these secondary conditions on MOSFET performance are explained. Verification and comparison of these effects are presented in chapter 5, focusing on how these effects change I-V characteristics. And at chapter 6, summary of results of the whole work, conclusion and proposed work for the future are given.

Chapter 2

Surface Potential Based Model

Surface potential is the total potential drop across the semiconductor region from the surface to a point in the bulk. In MOS literature the top surface of the semiconductor is commonly referred to "the surface" [38]. ψ_S , the potential at the Si/SiO_2 interface is a function of the terminal voltages. ψ_S is shown in figure (2.1).

2.1 Importance of Surface Potential Based Model

The surface potential based model enhances the physical content of the compact model and makes it more suitable for modeling advanced MOS devices. This has allowed to shift from the threshold voltage-based (V_t) [39] to surface-potential-based ψ_S approach [40], [41-47]. Thus, the ψ_S based approach provides substantial advantage in the improvement of compact models. It also allows one to increase the physics content of the model. Furthermore, surface potential is a physical variable and a single expression, which is valid in all regions of the MOSFET operation and can be derived by using the ψ_S based approach. All the compact ψ_S based MOSFET models are based on the charge-sheet approximation [41], [43] justified by comparison with the Pao-Sah double integration formula.

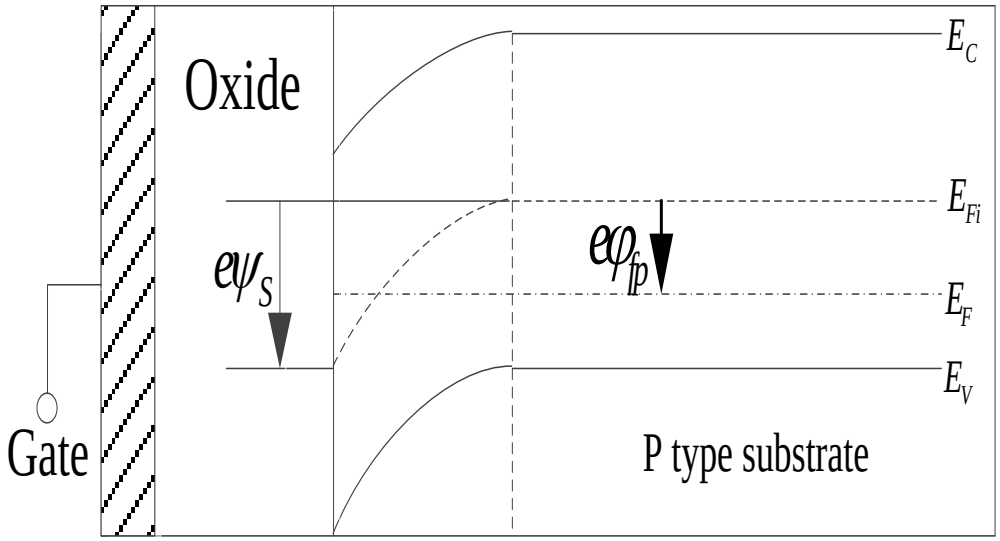

Figure 2.1: Energy band diagram representing surface potential (ψ_S).

2.2 Introduction to two Terminal MOS Structure.

In our gradual development toward the complete four terminal MOS transistor, our discussion will start with a basic two terminal MOS structure followed by some theoretical analysis on its behavior when gate-substrate voltage is applied .We will consider various potentials and charges developed when gate voltage is applied. This structure is often referred to as MOS capacitor. At first the gate terminal is short circuited to the body terminal. This develops a contact potential going from the gate through the external connection to the bulk or the body terminal. Due to this contact potential developed, it causes a net concentration of charges (usually positive) to appear in the substrate.

An external voltage (V_{FB}) can be applied between the gate and bulk to keep the semiconductor neutral and cancel the effects of the contact potential. This voltage is known as the flat-band voltage V_{FB}.

$$V_{FB} = \varphi_{ms} - \frac{Q_O^{'}}{C_{OX}^{'}} \tag{2.1}$$

Where, $C_{OX}^{'}$ is the oxide capacitance per unit area and φ_{ms} is the work function difference between the metal and the semiconductor and $Q_O^{'}$ is the effective oxide charge per unit area.

2.3 Potential balance and charge balance

We now discuss how the substrate is affected when an externally applied voltage V_{GB} assumes values different from the flat band voltage. Considering an example a MOS structure with p-type substrate. An arbitrary value of V_{GB} will in general cause charges to appear within a region adjacent to the top surface of the semiconductor. We define the surface potential ψ_S as the total potential drop across the region, defined from the surface to a point in the bulk. Four kinds of potential drops form a loop as follows:

$$V_{GB} = \psi_{OX} + \psi_S + \varphi_{ms} \tag{2.2}$$

Where, V_{GB} = Gate voltage, ψ_{OX} = Potential drop across the oxide.

According to overall charge neutrality in the system.

We have:

$$Q_G + Q_O + Q_C = 0 \tag{2.3}$$

Where, Q_G = Gate charge, Q_O = Effective oxide charge, Q_C = Charge in the semiconductor under the oxide.

Or in terms of charge per unit area,

$$Q_G^{'} + Q_O^{'} + Q_C^{'} = 0 \tag{2.4}$$

2.4 Effect of gate substrate voltage on surface condition

When V_{GB} increases above flat band voltage, the total charge in the gate becomes more positive than that of the flat band condition. To maintain charge neutrality the positive change in $Q_G^{'}$ must be balanced by a negative change in $Q_C^{'}$. The positive change in V_{GB} is shared among ψ_S and ψ_{OX}. If V_{GB} is not much higher than V_{FB}, the positive potential at the surface with respect to the bulk drives away the holes from the surface leaving it depleted. This condition is known as depletion shown in figure (2.2). More precisely as V_{GB} is raised above V_{FB}, the hole density keeps on decreasing well below the doping concentration value N_A. With the continual increase in V_{GB} more acceptor atoms are uncovered. Surface potential (ψ_S) becomes adequately positive to attract significant number of electrons to the surface. Eventually with a sufficiently high V_{GB} the density of electrons exceeds the density of holes at the surface. This condition is called inversion shown in figure (2.3). The electron concentration at the surface to that in the bulk can be related by:

$$n_{surface} = N_A e^{(\psi_S - 2\varphi_F)/\varphi_t} \tag{2.5}$$

Where, φ_F is the Fermi potential and φ_t is the thermal voltage. $\psi_S = 2\varphi_F$ is the onset of strong inversion.

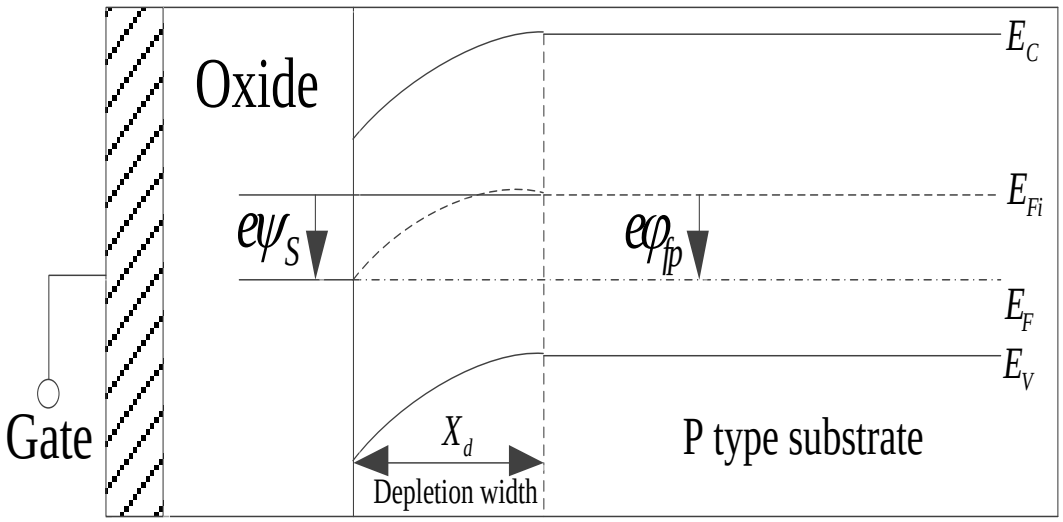

Figure 2.2: Energy band diagram for depletion mode.

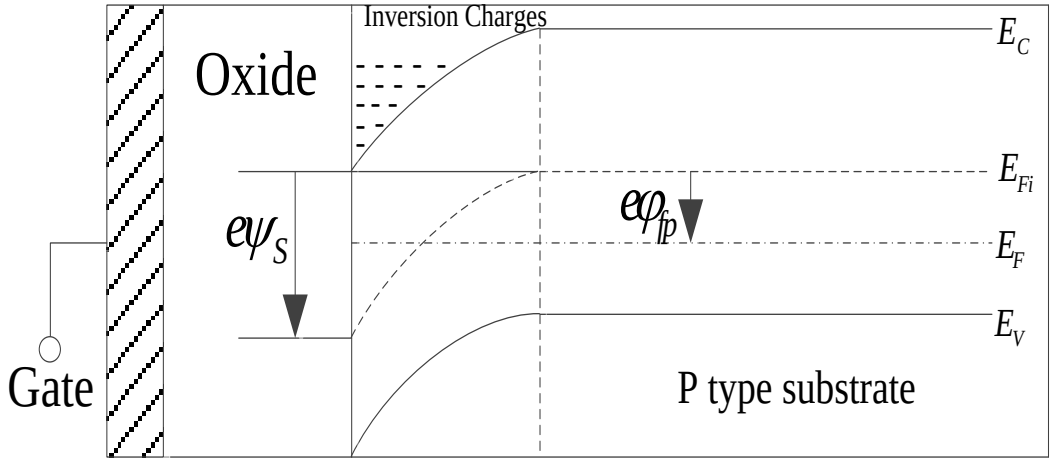

Figure 2.3: Energy band diagram for strong inversion mode.

2.5 General relations in the region of inversion

The total charge per unit area in the substrate $Q_C^{'}$ can be derived as [48]:

$$Q_C^{'} = \pm\sqrt{2q\varepsilon_S N_A}\sqrt{\varphi_t e^{-\psi_S/\varphi_t} - \psi_S - \varphi_t + e^{-2\psi_S/\varphi_t}(\varphi_t e^{\psi_S/\varphi_t} - \psi_S - \varphi_t)} \tag{2.6}$$

And the gate voltage can be expressed as:

$$V_{GB} = \psi_S - \frac{Q_I^{'}(\psi_S) + Q_B^{'}(\psi_S)}{C_{OX}^{'}} \tag{2.7}$$

Where,

$Q_I^{'}$ is the inversion layer charge per unit area and $Q_B^{'}$ is the depletion region charge per unit area due to uncovered acceptor atoms.

Finally we get a simplified version of equation between V_{GB} and ψ_S as given by:

$$V_{GB} = V_{FB} + \psi_S + \gamma\sqrt{\psi_S + \varphi_t e^{(\psi_S - 2\varphi_F)/\varphi_t}} \tag{2.8}$$

Where,

$$\gamma = \frac{\sqrt{2q\varepsilon_S N_A}}{C_{OX}^{'}}$$

A typical surface potential vs. gate voltage characteristics has been shown in figure (2.4) where $\psi_S = \varphi_F$ and $\psi_S = 2\varphi_F$ is the onset of weak inversion and moderate inversion respectively. Strong inversion begins at a surface potential of $\psi_S = 2\varphi_F + \varphi_{ZO}$.

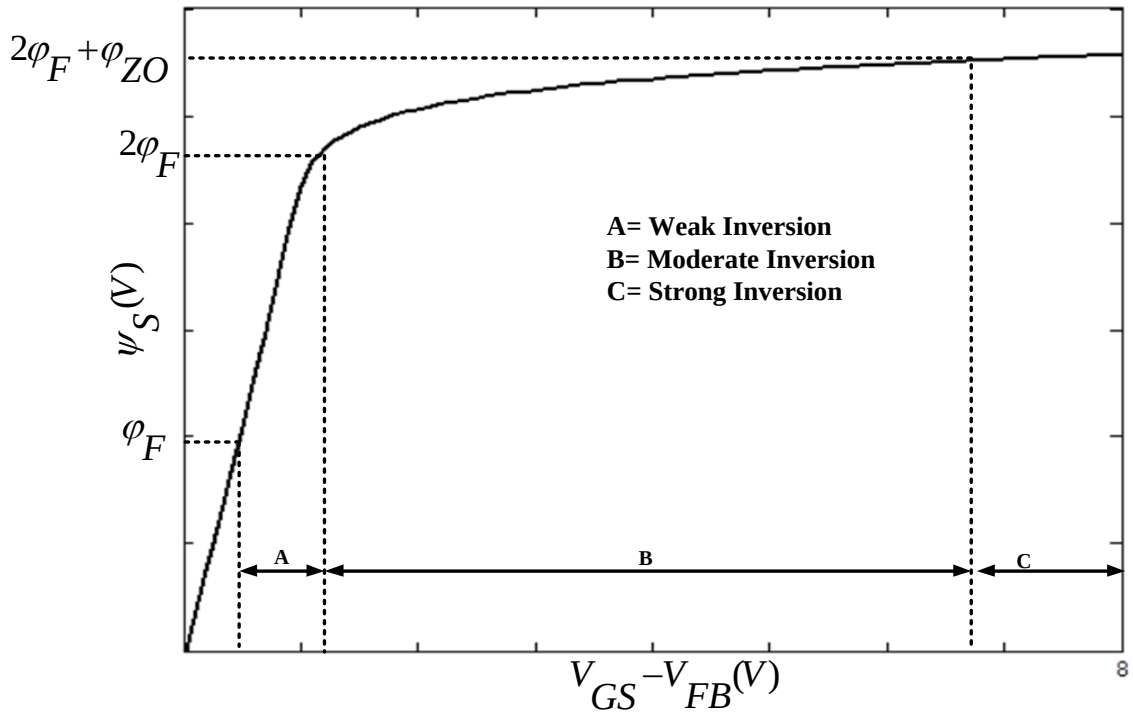

Figure 2.4: Surface potential vs. Gate voltage.

2.6 Contacting the Inversion Layer

Now the basic two-terminal MOS structure has been modified by adding a n^+ region. This is the three-terminal MOS structure. A n^+p junction is formed by this region and the substrate. The depletion region on the p side contains ionized acceptor atoms and the n^+ region contains ionized donor atoms. Connection is made between the n^+ region terminal and the substrate terminal and a voltage source V_{CB} is placed as shown in figure (2.5). The value of V_{CB} is greater than zero to ensure that the n^+p junction is reversed biased. The gate and substrate terminals are also connected to produce a surface potential ψ_S.

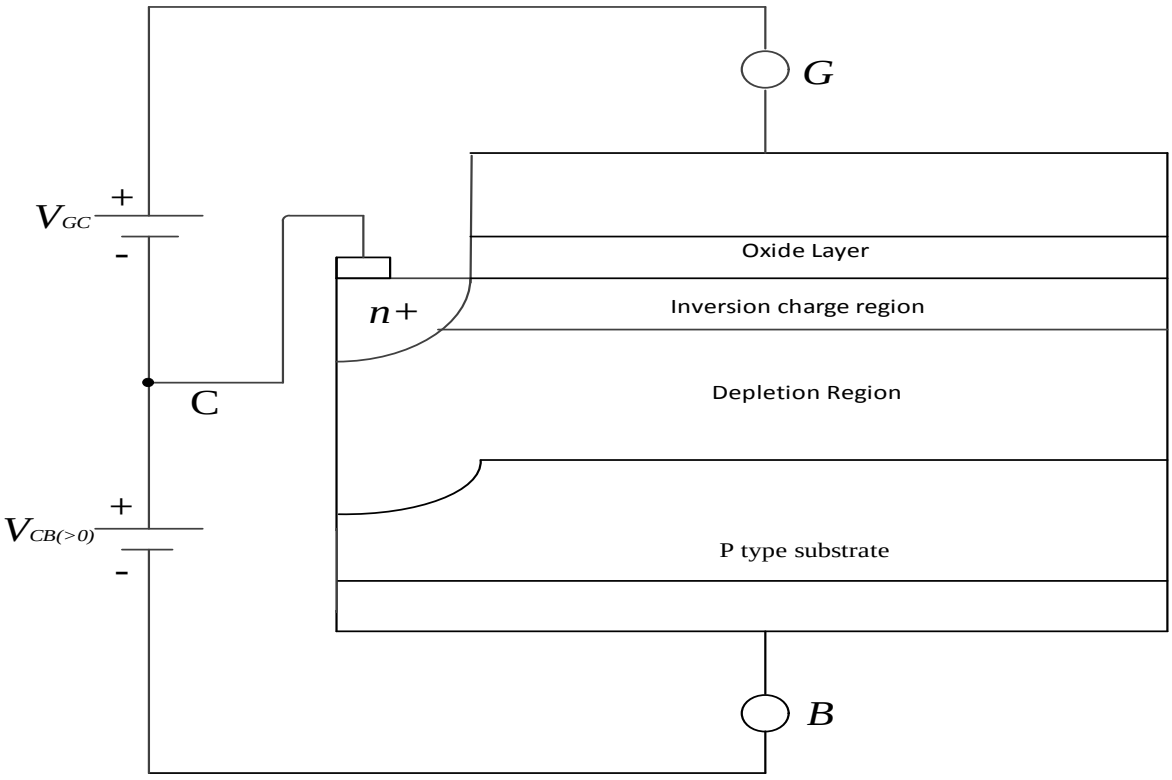

Figure 2.5: Three terminal MOS structure with n^+ region, biased at V_{CB} (>0) with voltages referred to the terminal C.

When $V_{CB} = 0$, for a certain V_{GB} a surface potential ψ_1, such that there is inversion occurs. With the increasing value of V_{CB}, the region becomes more positive. Electrons are attracted from the inversion layer by this positive potential towards the n^+ region, and from it to the top terminal of the voltage source. With the rise in V_{CB}, depletion region under the n^+ region becomes wider and the inversion layer under the surface keeps decreasing. The inversion layer may also disappear if V_{CB} is quite large. So to restore the surface to its previous condition, the surface potential must be increased by the same amount the potential of the n^+ region has increased. So, the surface potential must be increased from ψ_1 to $\psi_1 + V_{CB}$, as shown in figure (2.6). This is achieved by increasing V_{GB} by an appropriate amount. Then the surface will be at the original level of inversion again. The electron concentration at the surface is fixed by $\psi_s - V_{CB}$. Thus the electron concentration at the surface to that in the bulk can be related by:

$$n_{surface} = N_A e^{[\psi_S - (2\varphi_F + V_{CB})]/\varphi_t} \tag{2.9}$$

Thus in order to increase the level of inversion ψ_S is counterbalancing against $2\varphi_F + V_{CB}$. Figure (2.6) shows how the energy band is modified by V_{CB}.

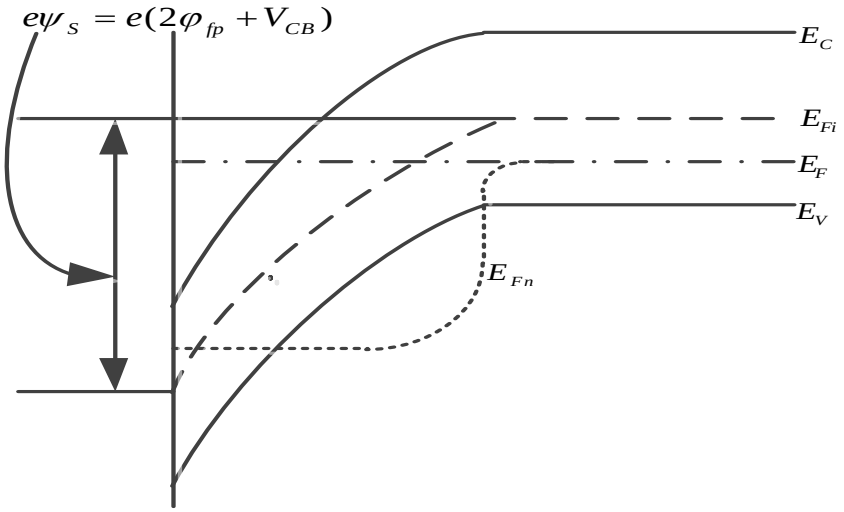

Figure 2.6: Modified Energy band after V_{CB} is applied at the third terminal of the MOS structure.

The relation between V_{GB} and ψ_S can be derived the same way as for the two-terminal structure, which is as follows [48]:

$$V_{GB} = V_{FB} + \psi_S + \gamma\sqrt{\psi_S + \varphi_t e^{[\psi_S - (2\varphi_F + V_{CB})]/\varphi_t}} \tag{2.10}$$

A typical surface potential (ψ_S) vs. $(V_{GB} - V_{FB})$ for different V_{CB} is shown in figure (2.7).

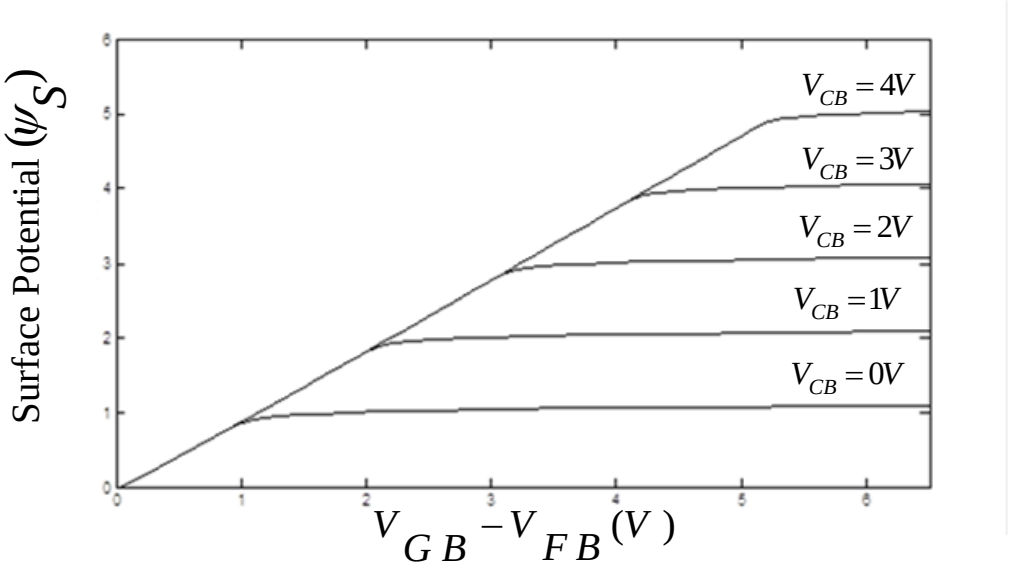

Figure 2.7: Surface potential (ψ_S) vs. $(V_{GB} - V_{FB})$ for different V_{CB}.

2.7 Surface Potential Based Drain Current Model

Throughout this section it is assumed that the channel is sufficiently long and wide, and the substrate is uniformly doped. The charge sheet approximate is also considered.

The contact potential V_{CB} at the source end is replaced with V_{SB}. Similarly at the drain end of the channel V_{CB} is replaced by V_{DB}. Both pn junctions should be in reversed bias for emphasizing the normal operation of a MOS transistor.

When $V_{DB}=V_{SB}$, an electric field in the semiconductor, perpendicular to the surface is obtained. If $V_{DB}\neq V_{SB}$, a nonzero component of electric field in the horizontal direction appears. This is much smaller than the vertical component of electric filed. So, the gradual channel approximation can be applied here, and only the vertical component of electric filed is considered.

There are two components of channel current, I_{DS}, the drift and diffusion current. Drift current, I_{DS1} occurs for the minority carriers (electrons and holes) due to drift in the presence of electric field. The diffusion current I_{DS2} occurs for the movement of charge appeared in the channel due to difference in charge concentration between the source and drain terminal of the MOSFET.

$$I_{DS} = I_{DS1} + I_{DS2} \tag{2.11}$$

I_{DS1} due to drift is given by,

$$I_{DS1} = \frac{W}{L}\int_{\psi_{SO}}^{\psi_{SL}} \mu(-Q_I^{'})d\psi_S \tag{2.12}$$

Where, μ is the electron mobility in the channel, ψ_{SO}, ψ_{SL} are the surface potential at the source end and at the drain end respectively. I_{DS2} due to presence of diffusion is given by,

$$I_{DS2} = \frac{W}{L}\varphi_t \int_{Q_{IO}^{'}}^{Q_{IL}^{'}} \mu dQ_I^{'} \tag{2.13}$$

Where, $Q_{IO}^{'}$ and $Q_{IL}^{'}$ are the inversion layer charge per unit area at the source and drain end respectively.

Assuming μ is constant along the channel, we have,

$$I_{DS1} = \frac{W}{L}\mu\int_{\psi_{SO}}^{\psi_{SL}} (-Q_I^{'})d\psi_S \tag{2.14}$$

$$I_{DS2} = \frac{W}{L}\mu\varphi_t(Q_{IL}^{'} - Q_{IO}^{'}) \tag{2.15}$$

To evaluate I_{DS1} and I_{DS2}, we need $Q_I^{'}$ as a function of ψ_S which is

$$Q_I^{'} = -C_{OX}^{'}(V_{GB} - V_{FB} - \psi_S + \frac{Q_B^{'}}{C_{OX}^{'}}) \tag{2.16}$$

Where,

$$Q_B^{'} = -\gamma C_{OX}^{'}\sqrt{\psi_S} \tag{2.17}$$

$Q_B^{'}$ is the charge due to the ionized acceptor atoms in the depletion region.
Thus $Q_I^{'}$ becomes,

$$Q_I^{'} = -C_{OX}^{'}(V_{GB} - V_{FB} - \psi_S - \gamma\sqrt{\psi_S}) \tag{2.18}$$

Using equation (2.18) in (2.14), we get the drain current component due to the presence of drift as [48]:

$$I_{DS1} = \frac{W}{L}\mu C_{OX}^{'}[(V_{GB} - V_{FB})(\psi_{SL} - \psi_{SO}) - \frac{1}{2}(\psi_{SL}^2 - \psi_{SO}^2) - \frac{2}{3}\gamma(\psi_{SL}^{3/2} - \psi_{SO}^{3/2})] \tag{2.19}$$

Using equation (2.18) in (2.15), we get the drain current component due to the presence of diffusion as [48]:

$$I_{DS2} = \frac{W}{L}\mu C_{OX}^{'}[\varphi_t(\psi_{SL} - \psi_{SO}) + \varphi_t\gamma(\psi_{SL}^{1/2} - \psi_{SO}^{1/2})] \tag{2.20}$$

ψ_{SL}, ψ_{SO} can be evaluated from the externally applied voltages, by replacing V_{CB} by V_{SB} at source end of the channel and V_{DB} at the drain end of the channel [48].

$$\psi_{SO} = V_{GB} - V_{FB} - \gamma\sqrt{\psi_{SO} + \varphi_t e^{(\psi_{SO} - 2\varphi_F - V_{SB})/\varphi_t}} \tag{2.21}$$

$$\psi_{SL} = V_{GB} - V_{FB} - \gamma\sqrt{\psi_{SO} + \varphi_t e^{(\psi_{SO} - 2\varphi_F - V_{DB})/\varphi_t}} \tag{2.22}$$

Where, the surface potential at the source and the drain end are denoted by ψ_{SO} and ψ_{SL} respectively.

A typical I-V characteristics curve found from equations (2.19) and (2.20) is shown in figure (2.8).

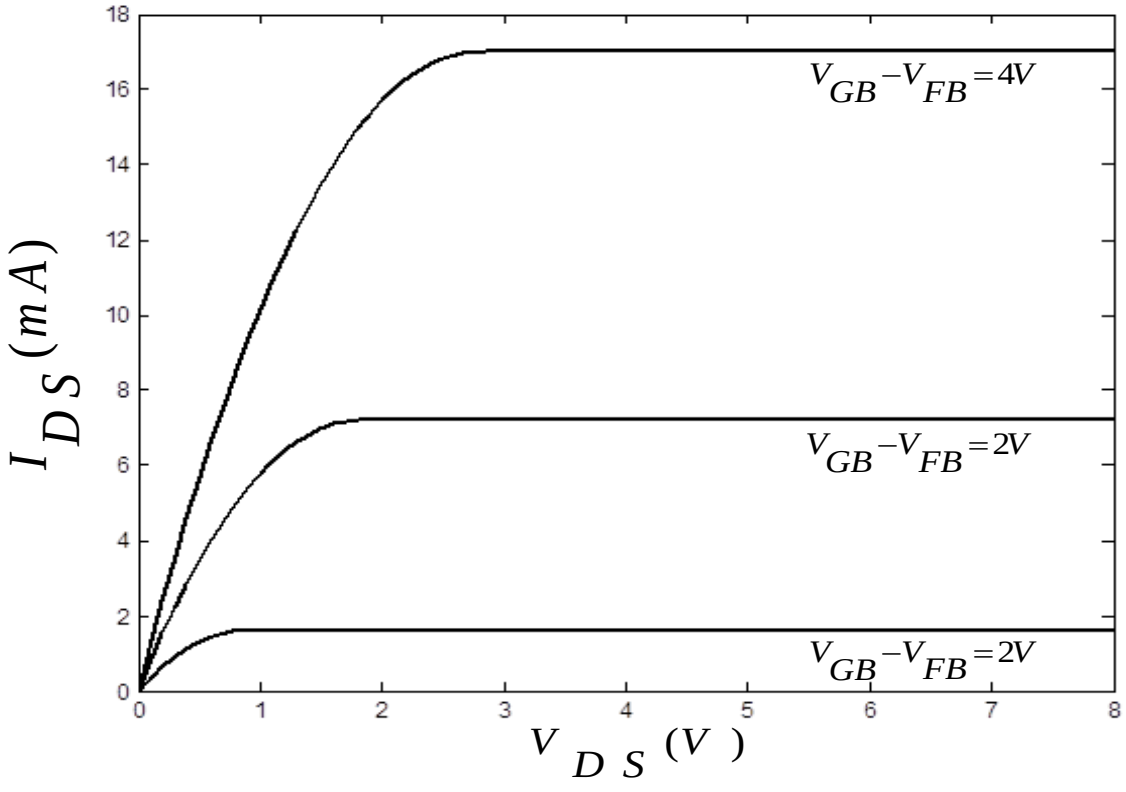

Figure 2.8: Drain current vs. Drain voltage for increasing $V_{GB}-V_{FB}(V)$.

Chapter 3

Interface States and Quantum Mechanical Effects

3.1 Interface States

The interface states arise from the native defects, such as Ga or As dangling bonds and Ga–Ga or As–As like-atom bonds created by oxidation. Each of these unsaturated bonds behaves as an interface defect which traps charges. These trap charges cannot move freely as there is relatively large distance between the neighboring interfacial traps states (these levels are localized and isolated from each other). As these levels can effectively trap the mobile electrons and holes (from the conduction and valence band respectively), these are called interface states. Interface states at the semiconductor/oxide interface in a metal-oxide-semiconductor structure play a vital role in determining the electrical characteristics of MOSFETs [49], which include the threshold voltage (V_T), the channel mobility (μ), the trans-conductance (g_m) and the sub threshold slope (S).

Interface trap charge (Q_{it}) (sometimes also called as surface states [50], fast states [51] or interface states [52]) is positively or negatively charged. Unlike a fixed oxide charge, an interface trapped charge interacts strongly with the underlining semiconductor and thus can be charged or discharged, depending on the surface potential. Now the question arises whether the interface trap (or interface state) is acceptor or donor-like. Ma and Knoll have suggested that the interface traps in the upper half of the silicon band gaps are acceptor-like and those in the lower half are donor-like [53-54]. Gray and Brown originally proposed this distribution and claimed that density and distribution of acceptor traps and donor traps in the silicon band gap are almost symmetrical [52]. In general, interface traps are classified as donor-like (positive when empty) or acceptor-like (negative when filled with electrons).

When a voltage is applied to the gate metal of a MOS structure, the Fermi level in the semiconductor moves up or down with respect to the band edges, thereby changing the occupation probability of the interface states. When the Fermi level energy, E_F coincides with the charge-neutrality level E_{CNL}, the whole interface is charge neutral. A slight deviation of E_F from E_{CNL} causes the interface states to be charged: the interface states will be negatively charged if E_F is higher than E_{CNL} and positively charged if E_F is below than E_{CNL}.

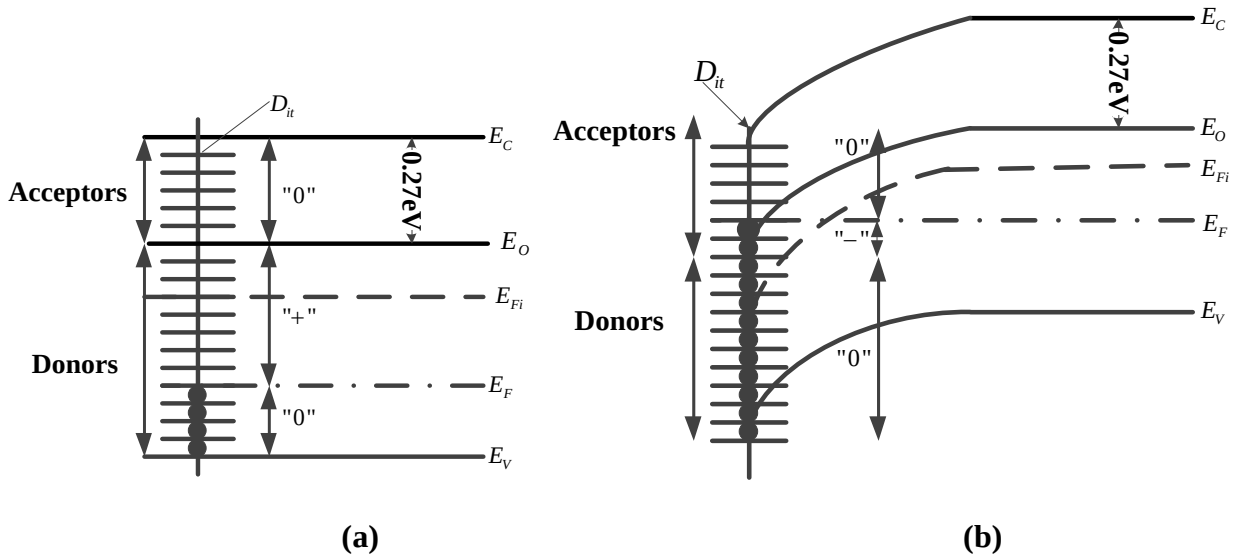

Figure 3.1 Band diagram of the $In_{0.53}Ga_{0.47}As$ Substrate of a n-channel MOS device showing the occupancy of interface traps and the various charge polarities (a) for positive interface trap charge at flat-band and (b) for negative interface trap charge at inversion. Each of the small horizontal lines represents an interface trap. It is either occupied by an electron (solid circle) or occupied by a hole (unoccupied by an electron), shown by the lines.

As can be seen from Fig. (3.1a) at flat-band voltage, where electrons occupy states below the Fermi energy, they are neutral (designated by "0"), being occupied donor states. Those between charge neutrality level (E_{CNL}) or E_o and the Fermi energy are positively charged (designated by "+"), being unoccupied donor states and those above E_o are neutral (unoccupied acceptors). For n-channel MOSFET at inversion, shown in Fig. (3.1b) the fraction of interface traps between E_o and the Fermi level is now occupied acceptors, leading to negatively charged interface traps (designated by "-"). Here charge neutrality level is not at the mid-band range, unlike Si. E_{CNL} for GaAs and InAs are 0.8 eV lower and 0.2 eV higher than the conduction band minima (E_{CBM}) respectively. E_{CNL} for $In_xGa_{1-x}As$ is estimated by linear interpolation between the two binary semiconductors InAs and GaAs. $E_{CN:}$ of $In_{0.53}Ga_{0.47}As$ is calculated to be 0.27 eV below E_{CBM}.

In this work, we have used $In_{0.53}Ga_{0.47}As$ as mentioned earlier. The distribution pattern of interface states against Fermi energy is shown in Fig. (3.2).

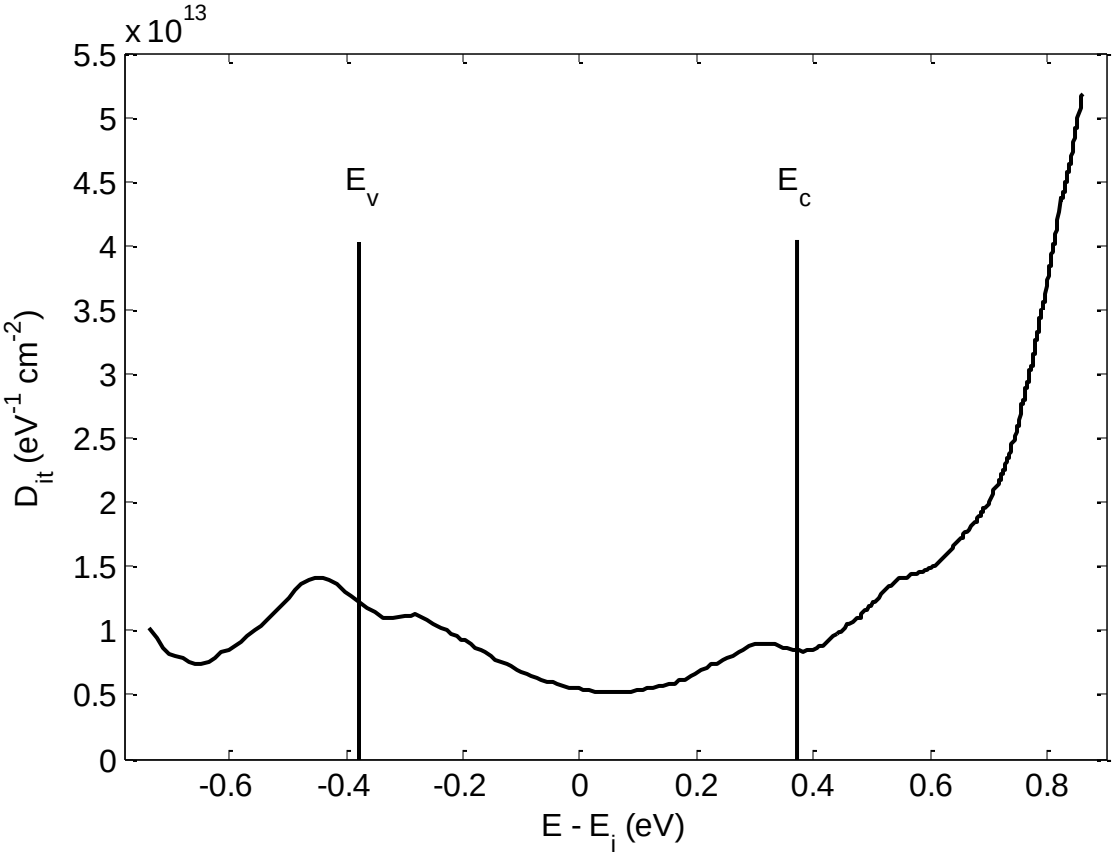

Figure 3.2: Variation of density of interface states with energy

This distribution has been extracted in [37] using measured low frequency characteristics.

Here the point to be noticed is that the interface trap states (D_{it}) keeps on increasing even after when energy level exceeds the conduction band minima.

3.2 Calculation of interface trap charges in MOS semiconductor/oxide interface

In recent years there has been an increased interest to find an accurate modeling and characterization of interface traps through the band gap, mostly using capacitance, and conductance and charge pumping methods [39]. Interface traps are now one of the most important non-idealities found in MOS structures. Interface trap charge is evaluated by

$$Q_{it} = q\int_{E_V}^{\alpha} f(E).D_{it}(E).dE \tag{3.1}$$

Where D_{it} is the interface trap charge density per cm^2 per eV. *f(E)* is Fermi-dirac distribution where E is the energy. *f(E)* may be approximated by its zero temperature distribution as a step function. As interface trap charges Q_{it} is effective in between Fermi energy level and E_{CNL} we can get Q_{it} by writing equation (3.1) as,

$$Q_{it} = q\int_{E_F}^{E_0} .D_{it}(E).dE \tag{3.2}$$

These charges are interrupting the electric field which comes from gate to semiconductor for positive applied gate voltage. That is why, because of the presence of these interface trap charges, effective gate voltage becomes,

$$V_G = V_G(D_{it} = 0) - \frac{Q_{it}}{C_{ox}} \tag{3.3}$$

Interface trap charges also alter the required flat band voltage (V_{FB}) as because of the same factor stated above. We know

$$V_{FB} = \varphi_{ms} + \frac{Q_{SS}^{'}}{C_{ox}} \tag{3.4}$$

Where φ_{ms} is the work function difference and $Q_{SS}^{'}$ is the equivalent trap charges per unit area including both fixed oxide charges and interface trap charges at flat band condition. So we get,

$$V_{FB} = \varphi_{ms} + \frac{Q_{SS} - Q_{it}}{C_{ox}} \tag{3.5}$$

Where Q_{SS} is the fixed oxide charges and Q_{it} is the interface trap charges.

3.3 Quantum Mechanical Effects (QME)

Quantum mechanical (QM) effects are playing a significant role in MOSFETs surface potential characteristics due to the ever shrinking feature size [57]. When the dielectric thickness of the MOSFET device is reduced below 4 nm, quantum mechanical (QM) effects near the silicon/silicon-oxide interface become significant [58-60]. The major quantum mechanical effects occurring in a MOSFET at deep sub-micron and the nanometer scales are the gate oxide tunneling, energy quantization in substrate and source to drain tunneling. Usually quantum mechanical effects are vital for designing sub 90 nm devices of MOSFET. Semi-classical models hence are inadequate and will lead to erroneous and misleading predictions of critical device structure and electrical behavior parameters such as the physical oxide thickness, threshold voltage, drive current, gate capacitance and sub-threshold swing.

As the MOSFET dimensions approach deep submicron and nanometer regions, the classical movement of the charge carriers is greatly affected by the non-classical behavior of electrons in the MOSFET. Due to aggressive scaling of the MOSFETs, the gate oxides are also scaled to nanometer regions. Also, the substrate doping is increased tremendously to negate the short channel effects at the deep sub-micrometer or nanometer scales. This results in very high electric fields in the silicon/silicon oxide interface and hence the potential at the interface becomes steep. This results in a potential well between the oxide field and the silicon potentials. During the inversion condition, the electrons are confined in this potential well. Due to confinement, the electron energies are quantized and hence the electrons occupy only the discrete energy levels [52-56]. This results in the electrons residing in some discrete energy levels which are above the classical energy level by some fixed value of energy as shown in Fig. (3.3). This is more important as the oxide thickness becomes smaller with each technology generation.

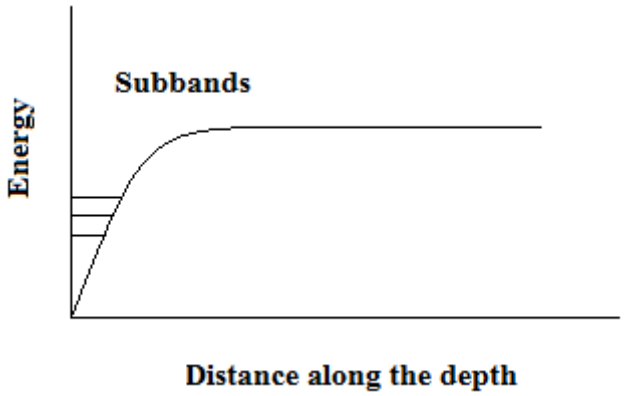

Figure 3.3 Discrete energy levels due to quantization (in the channel).

The potential well is narrow that the motion of the carriers of the surface channel is quantized in the direction perpendicular to the interface; consequently the carrier (probability) density is at maximum inside the well and not at the boundaries, as shown in Fig. (3.4). Therefore, the operation of deeply scaled MOS transistors cannot be accurately described by semi-classical physics, accurate calculation of the inversion charge requires introducing concepts derived from quantum mechanics (QM).

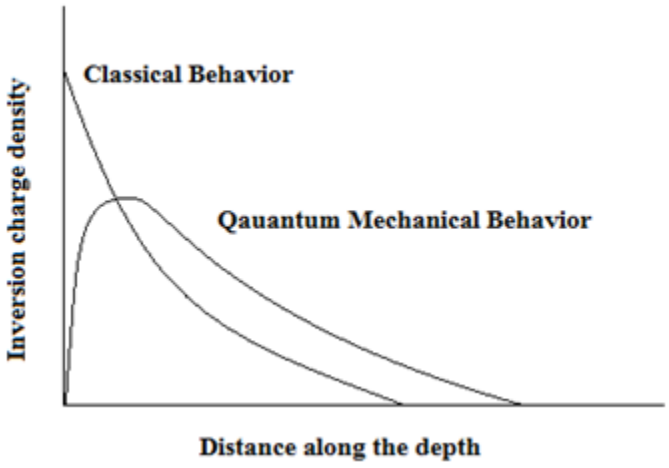

Figure 3.4 Electron concentration distribution in the semiconductor in classical and quantum mechanical cases.

3.4 Approaches to account for Quantum Mechanical Effects

Quantum mechanical effects modify the channel charge through two mechanisms:

i) The channel carriers get distributed among discrete energy levels instead of in a single energy band.

ii) The peak of the carrier concentration is located some distance away from the surface in the substrate, which is a result of superimposition of wave functions at the different energy levels.

Different techniques and models have been proposed over the years to incorporate these effects. Such as band-gap widening model which indirectly includes quantum mechanical (QM) correction. In this model, the proposed QM correction requires transformation of the semi-classical model. The existing physically based QM corrections are either derived from triangular well approximation or variational technique [20]. The physics of both approaches are dependable but none of the techniques are quantitatively correct. A physically based explicit analytical model for the QM correction the surface potential of nanoscale MOS devices was proposed in [25]. Recent study showed this model provides a more accurate QM correction method than the previous ones over a large range of device parameters.

The Karim and Haque QM correction model [25] to the semi-classical surface potential (ψ_S), is valid for both n-channel MOS (nMOS) and p-channel (pMOS) devices. This model directly adds the QM correction term to the semi-classical ψ_S.

According to the semi-classical model, the surface band bending ψ_S will be almost fixed after inversion takes place since a slight increase in the surface potential results in a large buildup of electron density at the surface. For devices with gate oxides in the nanometer range, the surface band bending from QM model is considerably larger than that from the classical model, for high electric field. This is because the 2-D carrier distribution of the sub bands and discrete energy levels lead to reduced charge density compared to semi-classical calculation. Therefore, an extra band bending is required for an increased charge density resulting elevated surface potential. Karim model directly adds this surface potential to the semi-classical model. That is,

$$\psi_{S(QM)} = \psi_{S(SC)} + \delta\psi_S \tag{3.6}$$

Using Pao-Sah equation [41], $\psi_{S\,(SC)}$, which is the semi-classical surface potential, can be estimated in variety of ways. The correction to the surface potential due to the QM effect using the physics of the QM charge sheet model has been shown as

$$\delta\psi_S = -\frac{Q_{inv} Z_{av}}{\in_0 \in_{Si}} \tag{3.7}$$

Here Z_{av} is the average penetration of the inversion carriers into the semiconductor from the oxide-semiconductor interface and Q_{inv} is the inversion charge density. Q_{inv} can be expressed as

$$Q_{inv} = -C_{ox}(V_g - V_{FB} - \psi_{S(QM)}) - Q_b \tag{3.8}$$

Where $C_{ox} = (\in_0 \in_{Si} / T_{ox})$ is the oxide capacitance per unit area, V_{FB} is the flat-band voltage, $Q_b = \mp\gamma C_{ox}\sqrt{\psi_{S(QM)}}$ is the depletion charge density, and $\gamma = \sqrt{2q \in_0 \in_{Si} N_{sub}} / C_{ox}$ is the body factor. Here, the (-) sign is for n-MOS devices, and the (+) sign for p-MOS devices.

Numerically an explicit expression of $\delta\psi_S$ has been derived [25], which is shown:

$$\delta\psi_S = \frac{C_{ox}\left[V_g - V_{FB} - \left(\psi_{S(SC)} + \delta\psi_S^1 \pm \gamma\sqrt{\left|\psi_{S(SC)} + \delta\psi_S^1\right|}\right)\right]E_1^1}{q \in_0 \in_{ox} F_{ox}^1} \tag{3.9}$$

And $\delta\psi_S^1$, the first order solution is

$$\delta\psi_S^1 = \frac{C_{ox}\left[V_g - V_{FB} - \left(\psi_{S(SC)} \pm \gamma\sqrt{\left|\psi_{S(SC)}\right|}\right)\right]E_1^0}{q \in_0 \in_{ox} F_{ox}^0} \tag{3.10}$$

Here, the (+) signs are for n-MOS devices, and the (-) signs are for p-MOS devices. E_1^0 and F_{ox}^0 are the zeroth-order terms, and E_1^1 and F_{ox}^1 are the first-order terms respectively. These are given by:

$$E_0^1 = \zeta_1 \left(\frac{\left| F_{ox}^0 \right| cm}{MV} \right)^{\lambda} \tag{3.11}$$

$$E_1^1 = \zeta_1 \left(\frac{\left| F_{ox}^1 \right| cm}{MV} \right)^{\lambda} \tag{3.12}$$

$$F_{ox}^0 = \frac{C_{ox} \left[V_g - V_{FB} - \psi_{S(SC)} \right]}{\in_0 \in_{ox}} \tag{3.13}$$

$$F_{ox}^1 = \frac{C_{ox} \left[V_g - V_{FB} - \left(\psi_{S(SC)} + \delta\psi_S^1 \right) \right]}{\in_0 \in_{ox}} \tag{3.14}$$

Here, for Si, ζ_1 = 77 meV and λ = 0.61 for electrons and for holes, ζ_1=88 meV and λ = 0.64 [25]. And when we use $In_{0.53}Ga_{0.47}As$, ζ_1 = 117 meV and λ = 0.52 for electrons and for holes, ζ_1 =130 meV and λ = 0.61 [61].

$\delta\psi_S$ is the surface potential which is coming into account due of QM effects. So by adding this to the semi-classical surface potential we have QM corrected result. However due to the nature of equations (3.9) and (3.10), $\psi_{S(QM)}$ leads to diverging derivative with respect to the gate voltage at flat-band (V_{FB}). Through numerical verification it has been found that $\delta\psi_S$ is negligible around the flat-band [25]. The problem of diverging derivative has been overcome exploiting this observation. It has done as follows:

$$\delta\psi_{S(SC)} = \psi_{S(SC)}; \text{ when } V_{tr1} \leq V_g - V_{fb} \leq V_{tr2}$$

$$= \psi_{S(SC)} + \delta\psi_S; \text{Otherwise} \tag{3.15}$$

Here, V_{tr1} and V_{tr2} are two transition voltages such that $V_{tr1} < 0$ and $V_{tr2} > 0$. Choices for $V_{tr\ 1}$= 0.001 V and V_{tr2} = 0.2 V for n-MOS and for p-MOS devices, V_{tr1}= -0.15 V and V_{tr2} = 0.001 V that work well for all cases. A notable feature of this proposed QM correction is that $\delta\psi_S$ is independent of V_{CB}, V_{CB} is the channel voltage that appears due to non-zero drain voltage. V_{CB} effects only $\psi_{S(SC)}$.

Chapter 4

Effects of QM correction and Interface States

4.1 Change in surface potential

An interface trapped charge is an interface semiconductor atom with an unsaturated (unpaired) valence electron at the InGaAs/Al_2O_3 interface. These traps behave as acceptor-like for energy E, when $E > E_{o,}$ and donor-like when $E < E_o$. When a gate voltage is applied across the semiconductor, a charge is paired with each unpaired electrons at the InGaAs/Al_2O_3 interface below E_F. These charges interrupt the electric field which comes from gate to semiconductor for positive applied gate voltage. For n-channel MOSFET when the applied gate voltage is zero Fermi energy lies below the E_{CNL} of the semiconductor, causing a positive accumulation of charge at the interface. These charges will attract electrons from the substrate causing gain in electron concentration despite no applied gate voltage. When the gate voltage is increased separation between Fermi energy and E_{CNL} will start to decrease. This will in turn reduce the interface trap charges at the surface. But as the nature of charge at the gate and at the interface is same, it will sum up to give a greater electron concentration than without considering any interface trap charge. At the point when Fermi energy is equal to E_{CNL}, there is no interface trap charge. Further increasing the gate voltage even, negative charge will take place along the interface as the Fermi energy will lay above the E_{CNL} of the semiconductor. This time it will cancel out the incoming electric field coming from the gate as the nature of charge at both ends are different. This will cause a reduced electron concentration as part of the electric field is cancelled out. Figure (3.1) shows the phenomenon. Figure (4.1) shows the variation of number of interface trap charge density with surface potential considering uniform D_{it}. Equation (3.2) has been used to find the interface trap charge density.

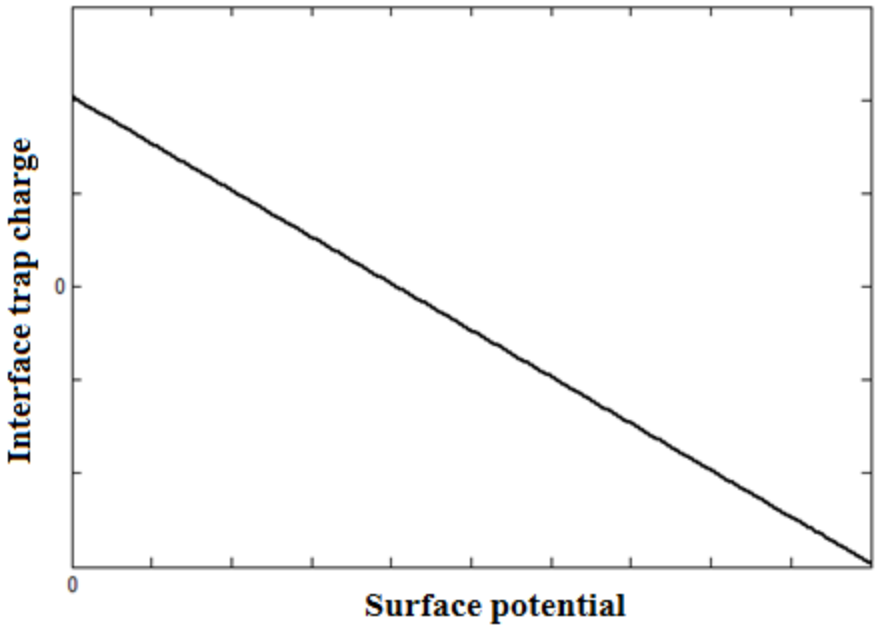

Figure 4.1: Variation of interface trap charges with surface potential.

QM effects also play a significant role on surface potential. As discussed earlier QM correction adds a separate surface potential to the semi-classical ψ_S due to the shift of inversion charge. This results increase in surface potential. Figure (4.2) compares the change in surface potential with gate voltage under different conditions.

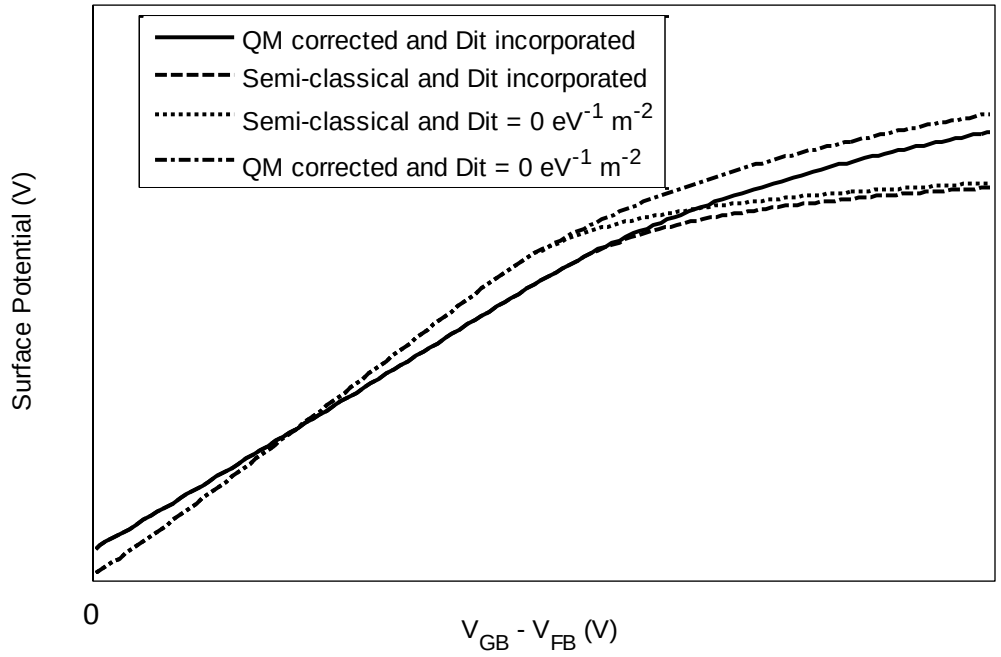

Figure 4.2: Surface potential vs Gate voltage.

As can be seen from the figure (4.2), at depletion region presence of interface states changes the slope of graph significantly, making it gradual than the ideal condition. But at inversion and strong inversion region QM effects plays vital role and increases the surface potential.

4.2 Mobility degradation

Due to the presence of interface trap charges, inversion charges flowing from the source to the drain will scatter more than before, resulting in degradation in mobility. As shown in figure (4.3), increasing the number of trap charges reduces mobility of the carriers. The following Equation (4.1) gives the relation between interface states and mobility.

$$\mu = \frac{\mu_0}{1+\alpha\frac{|Q_{it}|}{q}} \tag{4.1}$$

Where μ_0 is electron mobility in the absence of interface trap scattering and α is a proportionality constant. $\alpha \sim 1\times10^{-12}$ cm^2.

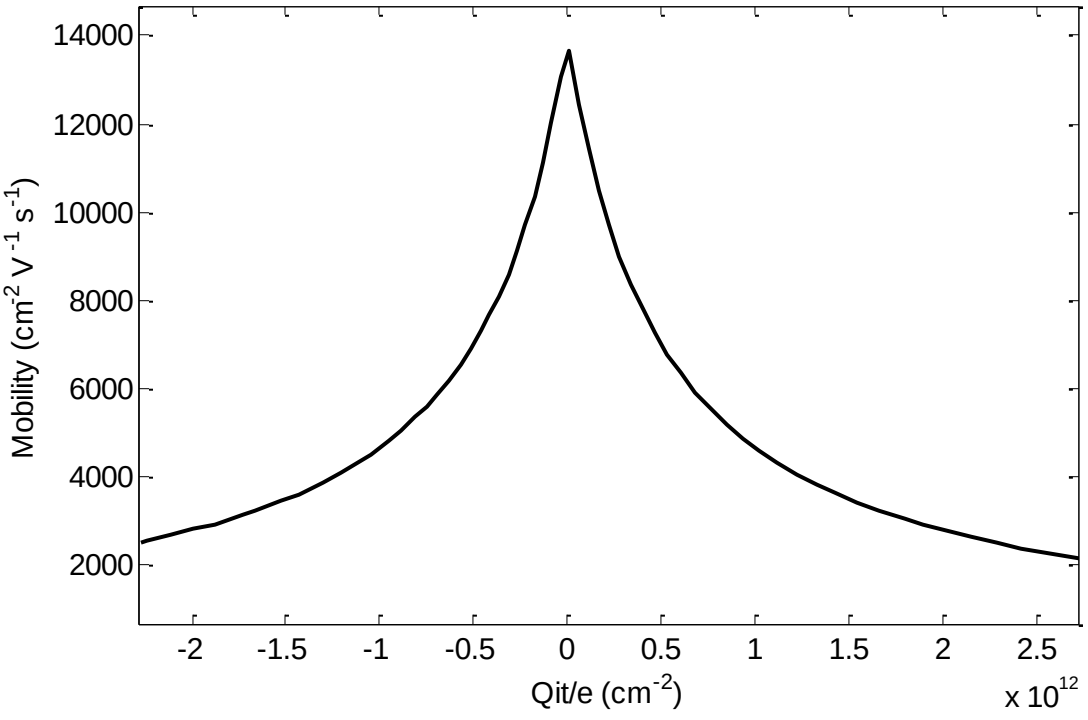

Figure 4.3 Variation of mobility with interface trap charge.

Here for simplicity mobility variation due to effective field along the vertical direction and applied voltage between the source and the drain have been neglected.

Chapter 5

Simulation and Results

In our work we have analyzed the impact of interface trap charges D_{it} and quantum mechanical (QM) correction to the surface potential based compact models for the drain current of $In_{0.53}Ga_{0.47}As$ MOSFETs. As already discussed in the previous chapters, due to the scaling down of MOSFETs, both interface trap charges and QM effects start to play vital role in change in surface potential with gate voltage, resulting a discernible change in I–V characteristics of the MOSFET.

We observe the effect of QM and D_{it} on the surface potential as a function of gate voltage. In order to implement the simulation we have considered some physical parameters of the MOSFET which are kept constant throughout the simulation at the temperature of 300K. Such parameters are as follows: doping density 10^{17} cm^{-3}, Al_2O_3 as gate dielectric material with a dielectric constant of 9 and thickness of 5 nm, $\frac{W}{L}$ of 5 and nickel was used as gate metal with a work function of 5.1V. The electron mobility without degradation due to interface charge was considered equal to the Hall mobility and is 14000 cm^2/V-s.

5.1 Effects of Quantum Mechanical Correction and Interface trap states on surface potential of the MOSFET

As shown in figure (5.1) the variation of interface charge density with respect to gate voltage was used from the D_{it} distribution shown in figure (3.2) for $In_{0.53}Ga_{0.47}As/Al_2O_3$ MOSFET.

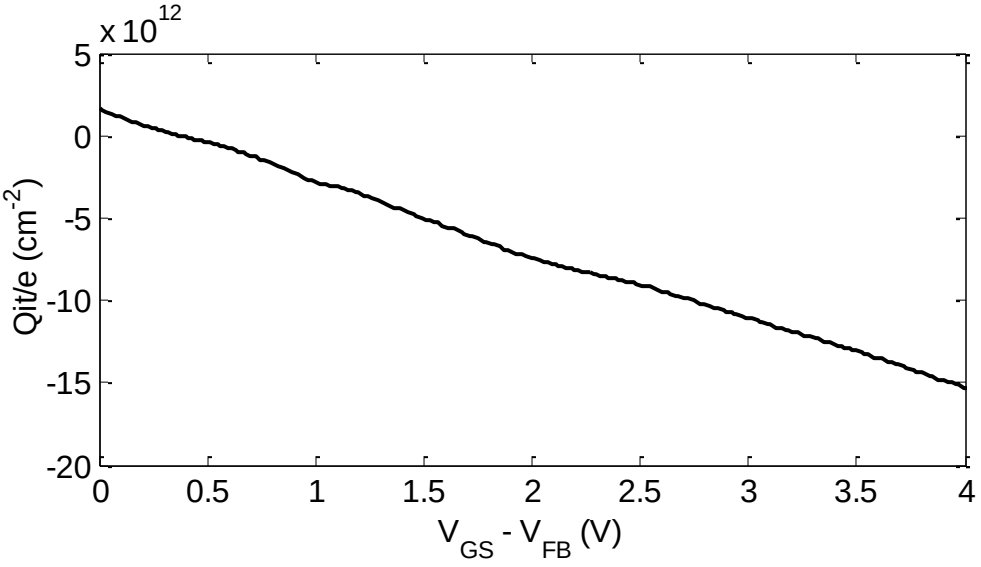

Figure 5.1: Variation of interface trap charges with gate voltage.

As we can see from figure (5.1) that the interface trap charges come into account significantly even after increasing the gate voltage by a very little value. So it is quite apparent that these interface trap states would greatly alter the surface potential.

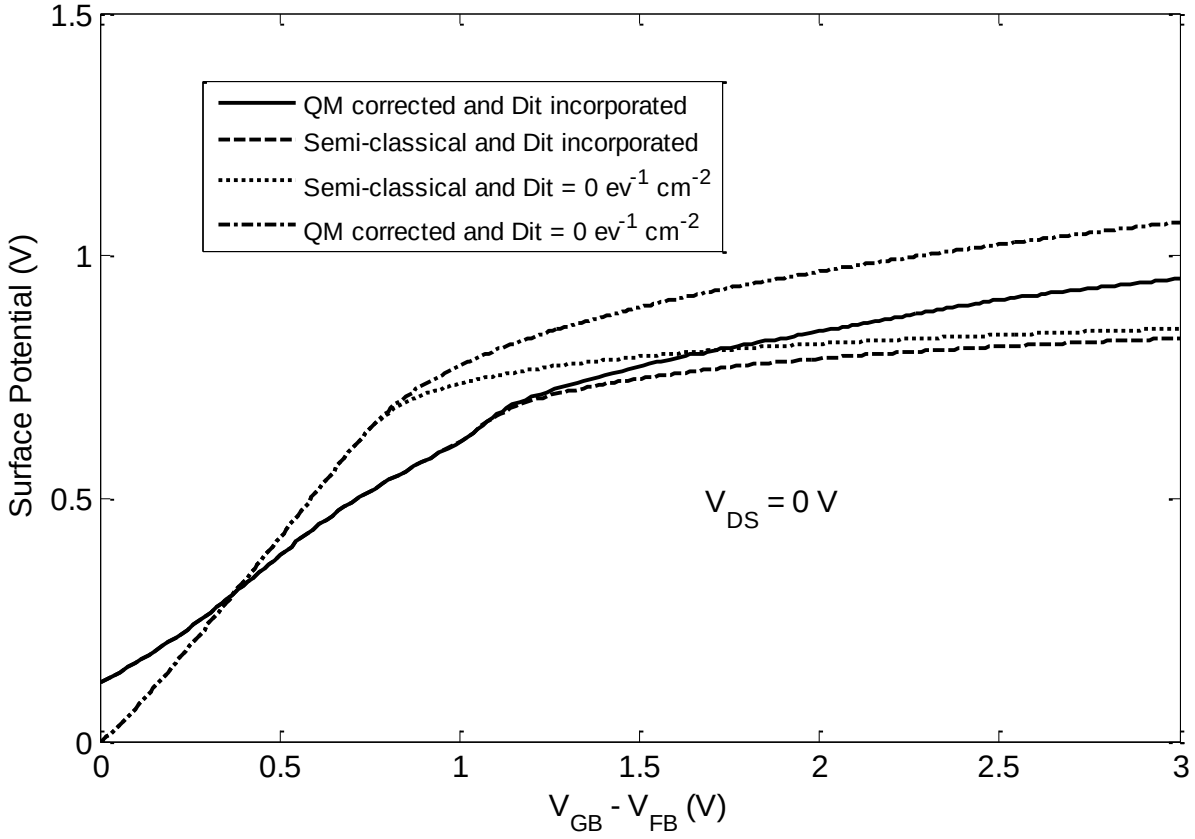

Figure 5.2: ψ_S - V_{GS} characteristics.

Incorporation of interface trap states plays a significant role in surface potential of the MOSFET as shown in figure (5.2). When QM correction was added the surface potential has changed potentially in the strong inversion only compared to semi-classical situation.

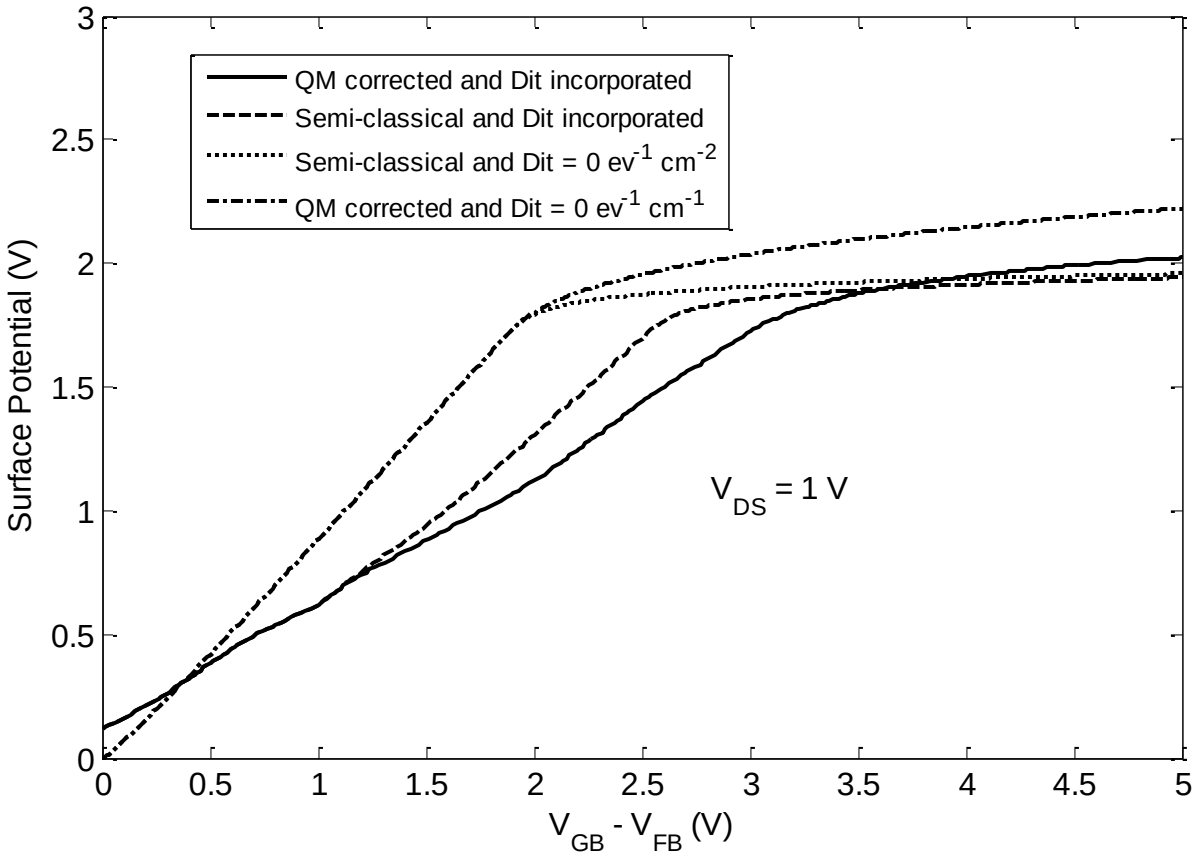

Figure 5.3: ψ_S - V_{GS} characteristics.

Figure (5.3) shows the surface potential of the MOSFET with respect to the gate voltage for drain to source voltage of 1 V. From the figure it is seen that there is less effect of interface trap states on the semi-classical value in the region of strong inversion because both with and without D_{it} saturates at the same potential level. On the other hand QM corrected surface potential with and without D_{it} continues to increase even in the region of strong inversion.

5.2 Effects of Quantum Mechanical Correction and Interface trap states on I-V characteristics

The effects of QM and D_{it} on the drain current are presented in this section. Here the I-V characteristics of MOSFET are simulated by taking extracted data of interface trap states as shown in figure (3.2).

We observe the effect of QM on I-V curves using Karim Model [25] and surface potential based compact model referred to chapter 2. The semi-classical I-V characteristic has been computed from the drift-diffusion equations (2.11), (2.19) and (2.20) derived in chapter 2. We already know that the quantum mechanical effect leads to an increase in the magnitude of ψ_S for a given gate voltage. This is because QM correction adds an additional component to the semi-classical surface potential due to the shift of charge. We have only considered inversion condition. With reference to figure (5.2), it is observed that the magnitude of the surface potential has increased from the inversion and continued to increase in the strong inversion. This results in a decreased inversion charge density at a given gate voltage compared to the semi-classical theory. QME also increases the threshold voltage as well. Therefore, we can see that the QME has decreased the saturation drain current by 21.1% than the ideal semi-classical current as shown in figure (5.4).

Similarly, due to the effect of D_{it} the semi-classical drain current decreased by 55.15%. This is because due to the presence of D_{it} in the oxide-semiconductor interface a smaller surface charge is induced at a given gate voltage. Due to the presence of interface trap charges, surface potential changes. Since the fraction of interface traps between CNL and the Fermi level in strong inversion are occupied donors, leading to negatively charged interface traps. Hence interface traps in n-channel devices in inversion are negatively charged, leading to positive threshold voltage shift [48]. As a result the drain current decreases. Furthermore, when the D_{it} is incorporated in QM correction the drain current decreases further by 83.4% with respect to the ideal semi-classical current. Finally, the incorporation of mobility degradation due to the interface trap states the drain current decreased further by 98.6% with respect to the ideal semi-classical value. All these quantitative comparisons were made for the saturated value of the drain current.

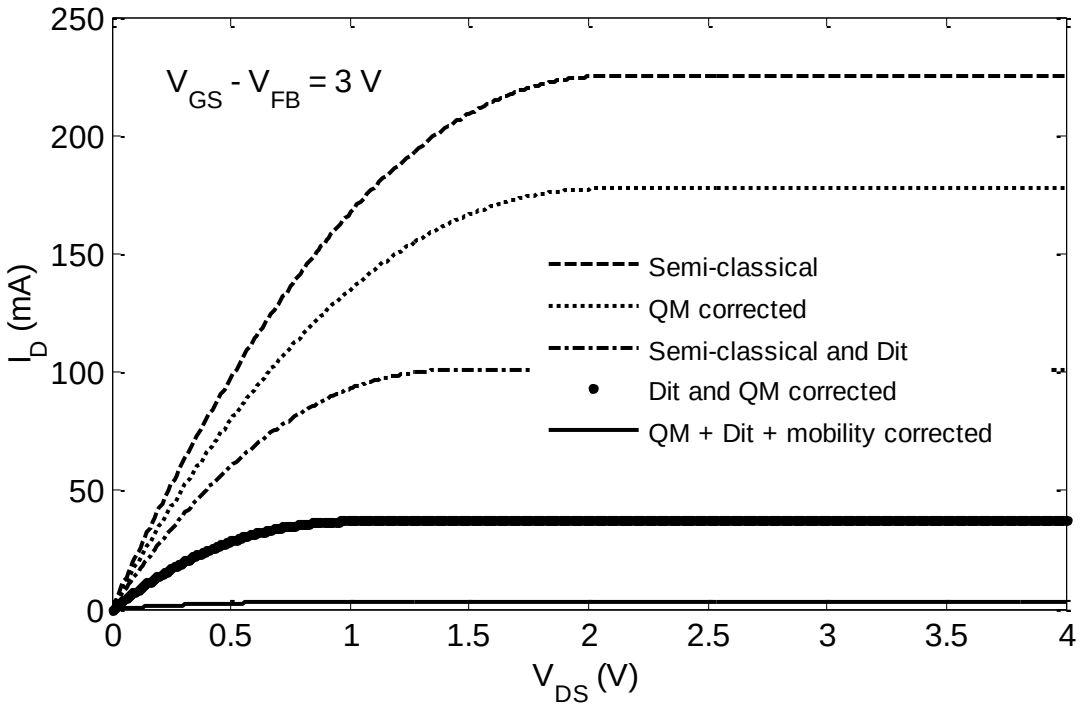

Figure 5.4: *I – V* characteristics.

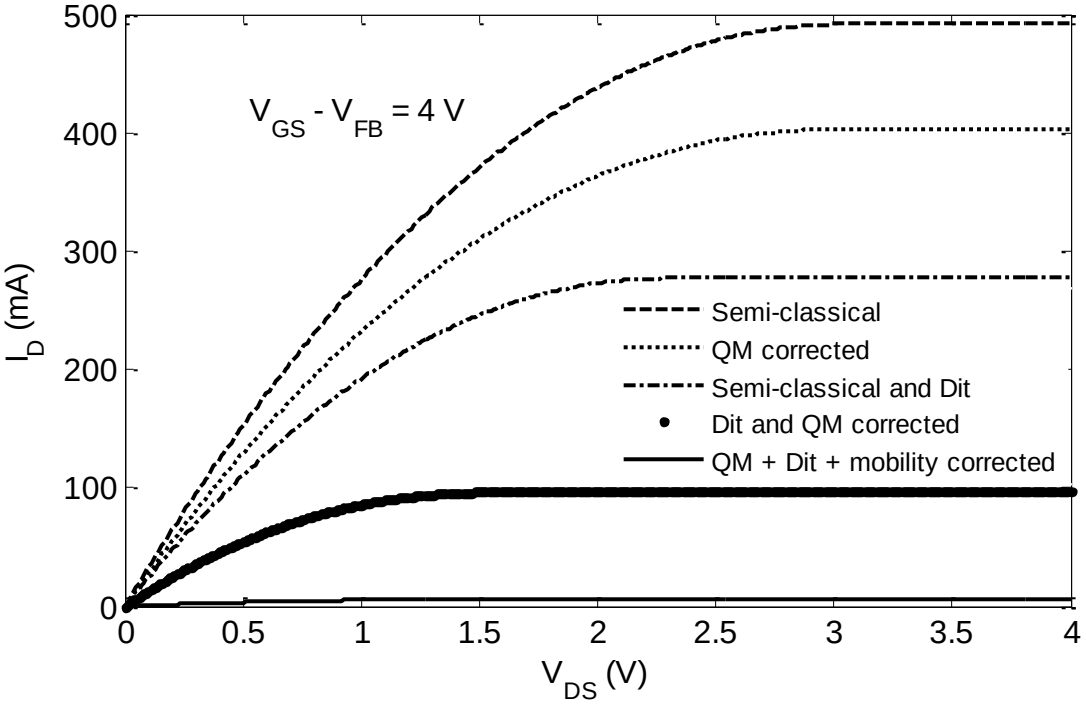

Figure 5.5: *I – V* characteristics.

The figure (5.5) shows the drain current with respect to drain voltage for $V_{GS} - V_{FB} = 4V$.

The transfer characteristics curve is shown in figure (5.6) for $V_{DS} = 50mV$. It is one of the important observations to analyze the subthreshold behavior of the MOSFET. The subthreshold behavior was observed through incorporating various types of secondary effects like quantum mechanical effect, interface trap states and mobility degradation.

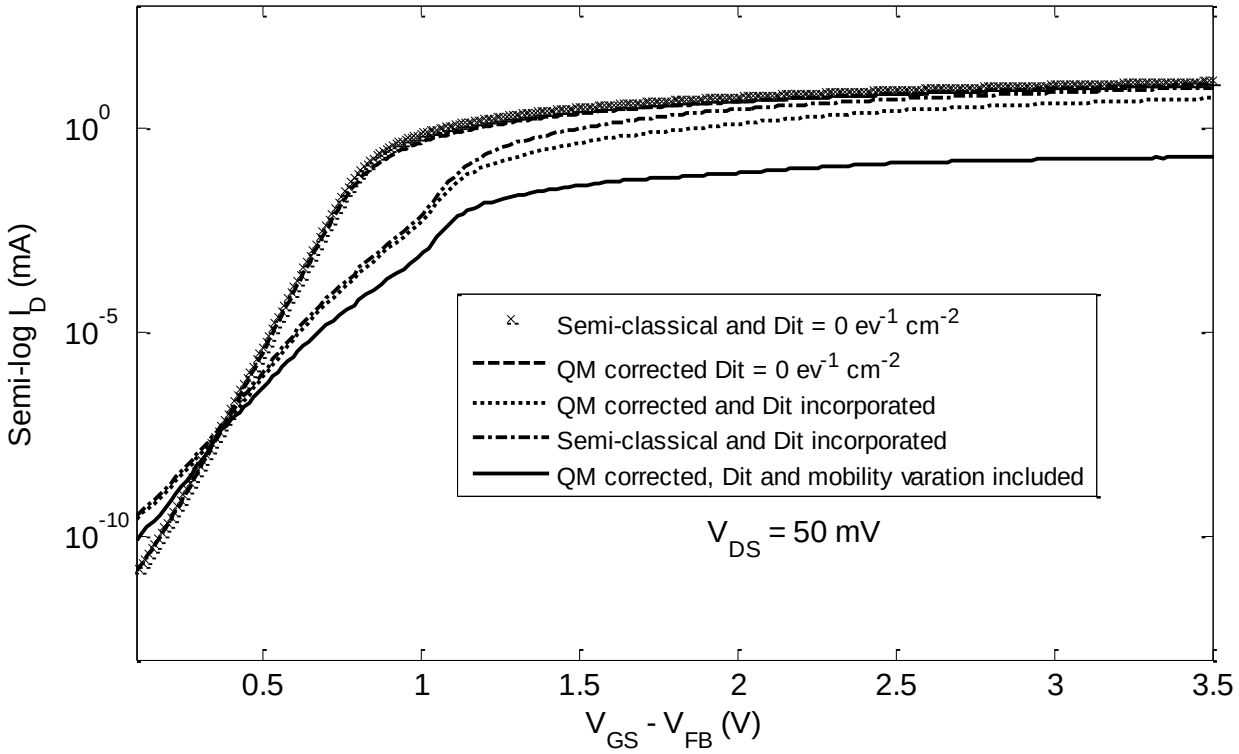

Figure 5.6: The transfer characteristics with respect to gate voltage.

Table 5.1: Subthreshold Swing.

Drain current model	Subthreshold Swing
semi classical	67.5 mV/dec
QM corrected	67.5 mV/dec
semi classical + D_{it}	107.3 mV/dec
QM corrected + D_{it}	110.92 mV/dec
QM corrected + D_{it} + mobility degradation	124.07 mV/dec

Table (5.1) gives the calculations of subthreshold swing for different drain current model. As it can be seen that the subthreshold swing is 67.5mV/dec for both semi-classical and QM corrected current. This shows that there is no effect due to Quantum Mecahnics on subthreshold swing. But there is a large increment in subthreshold swing, which is about 107.3mV/dec and 110.92mV/dec due to the incorporation of interface trap states in both semi-classical and QM

corrected current This is because of the gate voltage stretching occurred by the interface trap states. Figure (5.2) clearly explains the effect of interface trap states on gate voltage bias and it shows that there is a decrease in slope or stretching of gate voltage in the depletion region. Similarly, the mobility degradation due to interface trap states also increased the subthreshold swing to 124.07mV/dec. This has occurred because of the increase in electron scattering against the interface trap states in the channel. From the comparison it could be concluded that the change in subthreshold swing is more rigorous due to the effect of interface trap states than mobility degradation.

5.3 Discussions

From figure (5.2) and (5.3) we have found that the effect of quantum mechanical correction has been more prominent in the region of strong inversion. QM effect increases the surface potential in strong inversion. Hence affects the saturation drain current. Similarly interface trap states affects the slope of the surface potential in subthreshold region, the slope decreases significantly as shown in figure (5.2) and (5.3). It also increases the gate voltage required to induce a given carrier concentration. So the D_{it} affects both the saturation drain current and the subthreshold swing. Besides interface trap charges another parameter that played critical part is mobility. Mobility degradation due to D_{it} affects the subthreshold swing. It also greatly reduces the saturation drain current. Considering all these secondary effects into $In_{0.53}Ga_{0.47}As$ based MOSFET drastically reduces drain current from the surface potential based model of finding drain current, which has been denoted as 'Semi-classical' drain current in the previous section.

Chapter 6

Conclusion

6.1 Summary

The main objective of our work was to present the effects of interface trap states (D_{it}) in an explicit surface-potential based compact model on nanoscale MOSFET. We have also taken quantum mechanical effects (QME) into account as another secondary effect. The inclusion of QME was achieved by using Karim model [25] which is a physics-based and fully analytical and more accurate explicit model for the quantum mechanical correction to the surface potential of nanoscale MOSFETS.

We have used the extracted data of interface trap states of $In_{0.53}Ga_{0.47}As$. Due to the incorporation of interface trap states (D_{it}) only mobility degradation was taken into account.

The semi-classical I-V characteristic has been computed from the drift-diffusion equations (2.11), (2.19) and (2.20) derived in chapter 2. As we already know that the quantum mechanical effect leads to an increase in the magnitude of ψ_S for a given gate voltage due to the quantization of energies of the inversion electrons because of the strong vertical electric field. This results in a decreased inversion charge density at a given gate voltage compared to the semi-classical theory. The QME is more prominent in the inversion bias. This increase in surface potential affects the saturation drain current and we have observed that the saturation drain current has reduced to about 21.1% than the ideal semi-classical current as shown in figure (5.4).

Similarly, due to the effect of D_{it} the semi-classical saturation drain current decreased by 55.15%. Furthermore, when the D_{it} is incorporated in QM correction the saturation drain current decreases further by 83.4% with respect to the ideal semi-classical current. Finally, the incorporation of mobility degradation due to the interface trap states the drain current decreased further by 98.6% with respect to the ideal semi-classical value.

Finally, to follow the behavior of subthreshold swing was one of our prime concerns. From table (5.1) it can be observed that the subthreshold swing is 67.5mV/dec for both semi-classical and QM corrected current. This shows that there is no effect of QM on subthreshold swing. But there is a large increment in subthreshold swing, which is about 107.3mV/dec and 110.92mV/dec due to the incorporation of interface trap states in both semi-classical and QM corrected current The reason for this large transition is the stretching of gate voltage which occurred by the interface

trap states. Figure (5.2) representing the surface potential behavior with respect to gate voltage clearly explains the effect of interface trap states on gate voltage bias and it shows that there is a decrease in slope or stretching of gate voltage in the depletion region. Similarly, the mobility degradation due to interface trap states also increased the subthreshold swing to 124.07 mV/dec. This has occurred because of the increase in electron scattering against the interface trap states in the channel. In conclusion it could be noticed that the change in subthreshold swing is more severe due to the effect of interface trap states than mobility degradation.

6.2 Future Works

Further extension of our work can be done more accurately and comprehensively. Two dimensional analysis of devices under large V_{DS} can be done. Degradation of mobility due to vertical effective field and for different values of V_{DS} can be included in the model to attain the changes occur to the fundamental characteristics of the MOSFET. The short channel effects and gate tunneling current can also be included in the model. Furthermore, inclusion of the effects of parasitic resistances and capacitances in the model can be done. Finally, the results can be verified by comparing with measured experimental data.

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