An Optimal Design of Reversible Fault Tolerant n Bit Comparator

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Abstract

This thesis presents synthesis of the reversible comparator. The proposed circuits are designed using only parity preserving Fredkin and Feynman double gates. Thus, these circuits inherently turn into fault tolerant circuits. In addition, a lower bound on the number of constant inputs and garbage outputs for the reversible fault tolerant comparator has been proposed. It has been evidenced that the proposed circuit is constructed with these optimal garbage outputs and constant inputs. Moreover, a design algorithm for the generalized fault tolerant comparator has been presented. The comparative results show that the proposed design performs much better and has significantly better scalability than the existing approaches.

Letter for Acceptance

This Project entitled "**An Optimal Design of Reversible Fault Tolerant n-Bit Comparator**" submitted by Istiaq Ahmed (ID: 2010-3-60-020) and Nusrat Jahan Trisha (ID: 2011-1-60-016) to the Department of Computer Science and Engineering, East West University, Dhaka, Bangladesh is accepted by the department in partial fulfillment of requirements for the Award of the Degree of Bachelor of Science in Computer Science and Engineering on September, 2015.

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Chapter 1

Introduction

Reversible logic is very important to recover bit loss through unique mapping between input and output vectors [1]. There is no bit loss property of reversible circuitry results less power dissipation than the conventional one [2]. Moreover, as quantum evolution must be reversible, it is viewed as a special case of quantum circuit [3]. Reversible circuitry increase its interests in the field of DNA-technology [4], Nano-technology [5], optical computing [6], program debugging and testing [7], quantum dot cellular automata [8], and discrete event simulation [9] and in the development of highly efficient algorithms over the last two decades [10].On the other hand, for detecting single level fault parity checking is a very popular mechanisms. If the parity of the input data is maintained throughout the computation, then intermediate checking wouldn't be required and an entire circuit can preserve parity if its individual gate is parity preserving [11].Through parity checking, reversible fault tolerant circuit based on reversible fault tolerant gates allows to detect faulty signal in the primary outputs of the circuit [11].Generally, a Comparator is a hardware that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number. Digital comparators are common combinational logic circuits used in CPUs and microcontrollers (MCU). Therefore, this thesis investigates the generalized design methodologies of reversible fault tolerant 1-bit Comparator [10].

1.1 Motivation

In logic computation, kTln2 joules of heat are generated by every bit of information loss, where k is the Boltzmann constant and T is the absolute temperature of the environment [12]. Bennett showed that zero energy dissipation is possible if the circuit consists of only reversible gates [13]. Through unique mapping between inputs and outputs The Reversible circuit consists of only reversible gates that recover from bit loss. Moreover, it is viewed as a special case of quantum circuit as quantum evolution must be reversible [14]. Reversible computation gained remarkable interests in the development of highly efficient algorithms [13], [15], optimal architecture [16], [15], simulation and testing [17], [18], DNA and Nano-computing [19], [20], quantum dot cellular automata [22], [29], over the last twenty years. In addition, fault tolerant circuit based on reversible fault tolerant gates detect faulty signal in low level through parity checking [13], [16], [17],[23]. Parity checking is the easiest mechanisms for detecting single level fault. If every individual gate is parity preserving then the entire circuit can preserve parity. It is used mostly to detect errors in the storage or transmission of information. If the parity of the input data is maintained throughout the computation, then the intermediate checking would not be required and the entire circuit can preserve parity if its individual gate is parity preserving. In other words a reversible fault tolerant circuit can capture any erroneous result that tends to propagate through the downstream of modules without a danger of corrupting additional information.

In this report, we have proposed the reversible fault tolerant implementation of n-bit comparator. We have proposed different bit of comparator with improvement in terms of cost comparing with the existing designs.

1.2 Aims and Objectives

The objectives of this study are summarized below:

• To realize the reversible logic and reversible fault tolerant of n-nit comparator circuit in detail by examples and theories.

• To design an optimal comparator circuit which has minimal constant inputs and garbage outputs.

1.3 Overview

This document presents the implementation of the internal architecture of reversible fault tolerant n-bit comparator. We have proposed different bits of comparator with improvement in terms of cost comparing with the existing designs.

1.4 Methodologies of Research

While working on this research, the following important steps are followed:

• First, understanding of reversibility, its importance in low power circuitry, the basics of fault tolerance, its synthesis, the basics of quantum computation, its synthesis, various existing reversible and fault tolerant logic gates along with the quantum and transistor equivalent realizations etc.

• Designing various reversible and fault tolerant combinational circuits for n-bit comparator, studying existing comparator design approaches, then analyzing the designs, working procedures, advantages and shortcomings.

• Inventing and contriving the ideas for the fault tolerant reversible logic and basic I/O of comparator circuitry under a general and scalable structure. Establishing the novelty of the proposed methods through theoretical explanations. Finally, showing a comparative study among the proposed and the existing works through table.

1.5 Outline

The next chapter (Chap.2) briefly discusses about the Existing Reversible fault tolerant n- bit Comparator designs with their performance and evaluation.

Chap.3 discusses the Background study ie basic definition and literature overview relating to reversible and fault tolerant computing. The study includes understanding of the reversible and fault tolerant logic gates along with their quantum equivalent realizations and applications.

Chap.4 introduces several components of proposed reversible Fault tolerant 1, 2, n-bit design approaches. It describes elaborate design methodologies of the working procedure of the proposed comparator.

Chap.5 illustrates the performance evaluation of the proposed method.

Chap. 6 finally discussed about Conclusions and Future work.

1.6 Summary

This chapter demonstrates motivations and objective of this thesis. Then the methodologies of the research that is being followed are discussed here. A brief elementary instructional text of remaining chapters of this thesis has also been described.

Chapter 2

Background Study

This chapter introduces the basic definition and properties which are related with reversible logic and Comparator. Definition of reversible gate, garbage output, delay, hardware complexity and presents popular reversible fault tolerant gates along with their input-output specifications, transistor and quantum equivalent representations are formally defined in this section.

2.1 A Reversible and Fault Tolerant Gates

An n×n reversible gate is a data stripe block that uniquely maps between input vector Iv = (I_0, I_1, …., I_{n-1}) and output vector Ov = (O_0,O_1, . . . , O_{n-1}) denoted as Iv ↔ Ov.

Two prime requirements for the reversible logic circuit are as follows [14]:

- There should be equal number of inputs and outputs.
- There should be one-to-one correspondence between inputs and outputs for all possible input-output sequences.

A Fault tolerant gate is a reversible gate that constantly preserves same parity between input and output vectors. More specifically, an n × n fault tolerant gate clarifies the following property between the input and output vectors [12]:

$$I_0 \oplus I_1 \oplus \ldots \oplus I_{n-1} = O_0 \oplus O_1 \oplus \ldots \oplus O_{n-1} \qquad (1)$$

Parity preserving property of Equation.1 allows detecting a faulty signal from the circuit's primary output. Researchers [11], [12], [15] have showed that the circuit consist of only reversible fault tolerant gates preserves parity and thus able to detect the faulty signal at its primary output.

2.2 Constant Inputs

Number of constant inputs is one of the other main factors in designing a reversible logic circuit. The input that is added to an n*k function to make it reversible is called constant input [24]. The proposed parity preserving reversible full adder circuit requires only two constant inputs that are equal to the design in [25] and this is the minimum theoretically, but the design in [26] requires 5 constant inputs. So, it can be stated that the proposed design approach is better than all the existing designs in terms of number of constant inputs. From the above discussion we can conclude that the proposed fault tolerant reversible full adder circuit is better than all the existing counterparts.

2.3 Garbage Output

Garbage Outputs: Garbage output refers to the output of the reversible gate that is not used as a primary output or as input to other gates [24]. One of the other major constraints in designing a reversible logic circuit is to lessen number of garbage outputs. Our proposed parity preserving reversible full adder circuit produces only three garbage outputs which are equal to the design in [25] and this is the minimum as proved earlier in this thesis, but the design in [26] produces six garbage outputs. So, it can be stated that the proposed design approach is better than all the existing counterparts in terms of number of garbage outputs.

2.4 Qubit and Quantum Cost

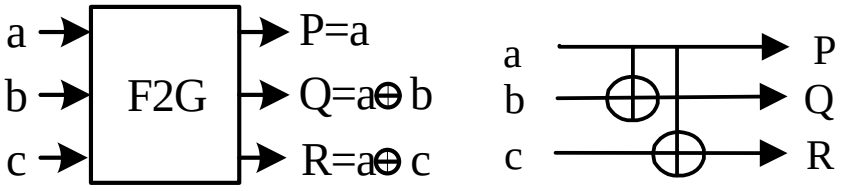
The main difference between the qubits and conventional bits is that, qubits can form linear combination of states |0> or|1> called superposition, while the basic states |0> or |1> are an orthogonal basis of two-dimensional complex vector [3]. A superposition can be denoted as, $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$, which means the probability of particle being measured in states 0 is $|\alpha|2$, or results 1 with probability $|\beta|2$, and of course $|\alpha|2 + |\beta|2 = 1$ [16]. Thus, information stored by a qubit are different when given different α and β. Because of such properties, qubits can perform certain calculations exponentially faster than conventional bits. This is one of the main motivations behind the quantum computing. Quantum computer demands its underneath circuitry be reversible [1] ~ [6].

The quantum cost for all 1×1 and 2×2 reversible gates are considered as 0 and 1, respectively [6]~[14]. Hence, quantum cost of a reversible gate or circuit is the total number of 2×2 quantum gate used in that reversible gate or circuit.

2.5 Popular Reversible Fault Tolerant Gates

2.5.1 Feynman Double Gate

Input vector (Iv) and output vector (Ov) for 3 × 3 reversible Feynman double gate(F2G) is defined as follows [11]: Iv = (a, b, c) and Ov = (a, a⊕b, a⊕c). Block diagram of F2G is shown in Fig. 1(a). Fig. 1(b) represents the quantum equivalent realization of F2G. From Fig. 1(b) we find that it is realized with two 2×2 Ex-OR gate, thus its quantum cost is two.

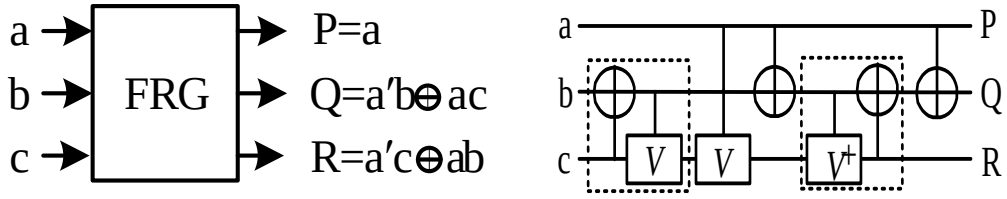


(a) (b)

Fig. 1: Reversible Feynman double gate (a) Block diagram (b) Quantum equivalent realization

2.5.2 Fredkin Gate

The input and output vectors for 3 × 3 Fredkin gate (FRG) are defined as follows [11]: Iv = (a, b, c) and Ov = (a, ab⊕ac, ac⊕ab). Block diagram of FRG is shown in Fig. 2(a). Fig. 2(b) represents the quantum realization of FRG. In Fig. 2(b), each rectangle is equivalent to 2 × 2 quantum primitives, therefore its quantum cost is considered as one [11]. Thus total quantum cost of FRG is five.



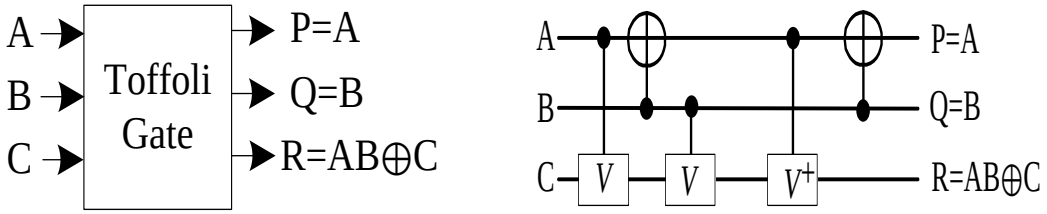
(a) (b)

Fig. 2: Reversible Fredkin gate (a) Block diagram (b) Quantum equivalent realization

2.5.3 Toffoli Gate

The Toffoli gate is one of the most popular reversible gates and has quantum cost of 5.Toffoli gate is a 3*3 gate in which three inputs vector is I (A, B, C) and the three

output vector is O (P,Q, R) and output is P=A, Q=B, R=AB⊕C. The circuit representation and gate representation of Toffoli gate is shown in fig.

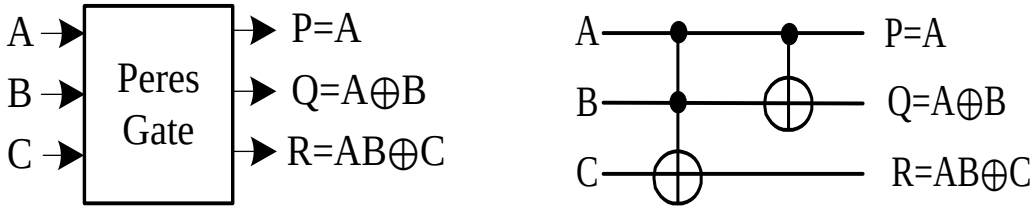


(a) (b)

Fig. 3: Reversible Toffoli gate (a) Block diagram (b) Quantum equivalent realization

2.5.4 Peres Gate

In the existing literature, among the 3*3 reversible gate, Peres gate has the minimum quantum cost and its quantum cost is 4.The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A⊕B and R=AB⊕ C. The circuit representation and gate representation of Peres gate is shown in fig.



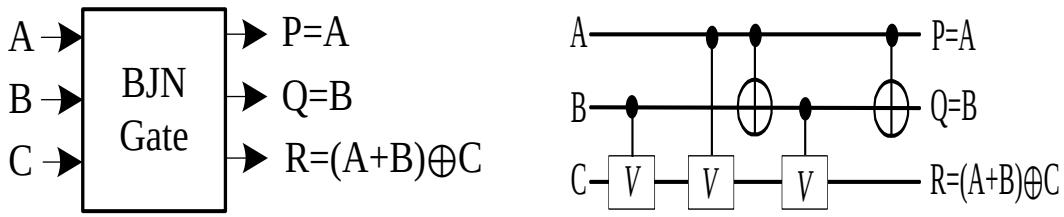
(a) (b)

Fig. 4: Reversible Peres gate (a) Block diagram (b) Quantum equivalent realization

2.5.5 BJN Gate

BJN gate is a 3*3 gate with inputs (A, B, C) and outputs P=A, Q=B, R = (A+B) ⊕C. Its quantum realization is shown in figure. It has quantum cost of 5.

The circuit representation and gate representation of BJN gate is shown in fig.



(a) (b)

Fig. 5: Reversible BJN gate (a) Block diagram (b) Quantum equivalent realization

2.6 Comparator

A comparator circuit compares two inputs A and B that gives three outputs as A>B (where, A is greater than B), A<B (where, A is less than B) and A=B (where, A is equal to B). Comparators are often used, for example, to check whether an input has reached some predetermined value.

2.7 Summary

A brief literature overview and the related terminologies regarding reversible and Fault tolerant logic synthesis are presented in this chapter. Definitions of two most popular reversible and fault tolerant logic gates devoted here as well. Also a basic note about Comparator has been given in this chapter.

Chapter 3

Existing 1-bit Comparator

Essential technical background of Control Unit is presented in this chapter which is required to understand the proposed work. Section 3.1, 3.2, 3.3, 3.4 present the design and working procedure of one-bit reversible comparator design using different gates.

3.1 One- bit comparator using Peres and BVF gate

Reversible one bit comparator is implemented with DFG gate and Peres gate and BVF gate as shown in fig. The numbers of garbage outputs are two and represented as G1 and G2, it uses two constant inputs, one logic ‘0’ and two logic ‘1’and its quantum cost is 8.

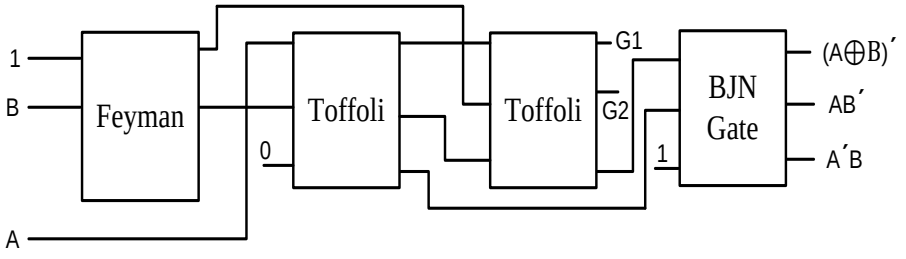


Fig.6: proposed one bit comparator using Peres gate [27]

3.2 One bit comparator using Toffoli and BVF gate

Reversible one bit comparator is implemented with DFG gate and Toffoli gate and BVF gate as shown in fig. The number of garbage outputs are two and represented as G1 and G2, it uses two constant inputs, one logic ‘0’ and two logic ‘1’ and its quantum cost is 9.

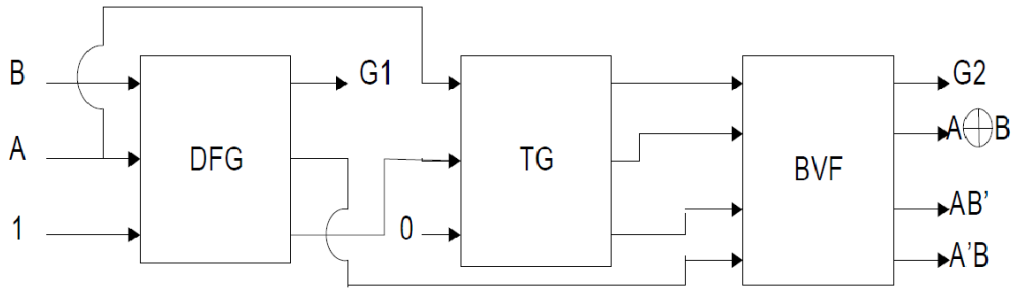


Fig .7: proposed one bit comparator using Toffoli gate [27]

3.3 One bit comparator using Fredkin and BVF gate

Reversible one bit comparator is implemented with BVF gate and Fredkin gate and BVF gate is as shown in fig. The number of garbage outputs is three and represented with G1to G3, it uses two constant inputs, logic ‘0’ and logic ‘1’ and its quantum cost is 9.

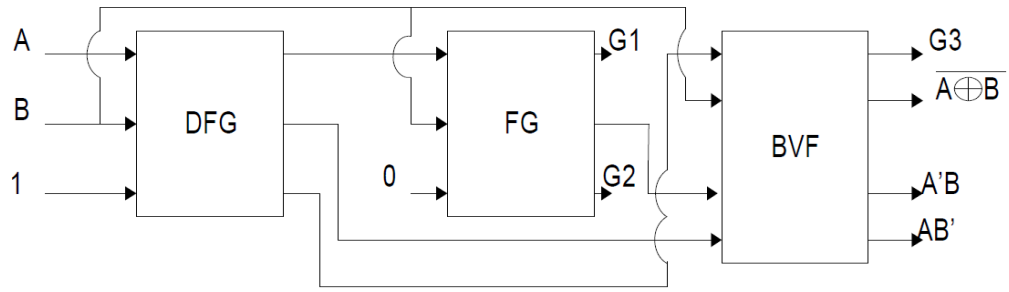


Fig. 8: proposed one bit comparator using Fredkin gate [27]

3.4 One bit comparator using TR and BVF gate

Reversible one bit comparator is implemented with Feynman gate and TR gate and BVF gate as shown in fig. The number of garbage outputs is one and represented as G1, it uses two constant inputs, logic ‘0’ and logic ‘1’ and its quantum cost is 7.

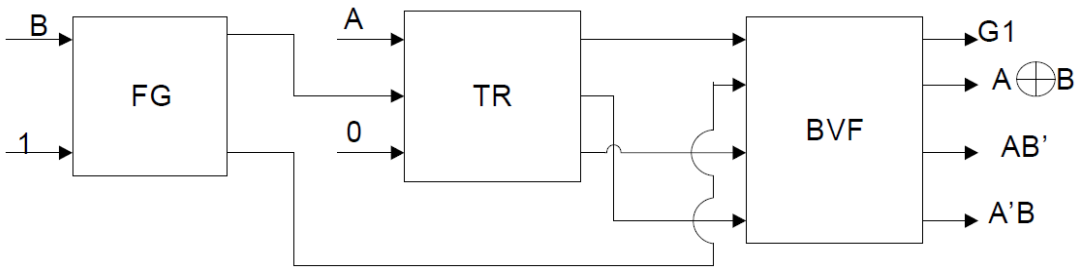


Fig. 9: proposed one bit comparator using TR gate [27]

3.5 Summary

This chapter demonstrates the conventional works on reversible fault tolerant one-bit comparator with the help of different gates and structures.

Chapter 4

Proposed Reversible Fault Tolerant n-bit Comparator

4.1 Reversible Fault Tolerant Single-bit Comparator

A reversible fault tolerant one-bit comparator can be designed with at-least 3 Feynman Double Gate (F2G) and 1 Fredkin Gate (FRG).

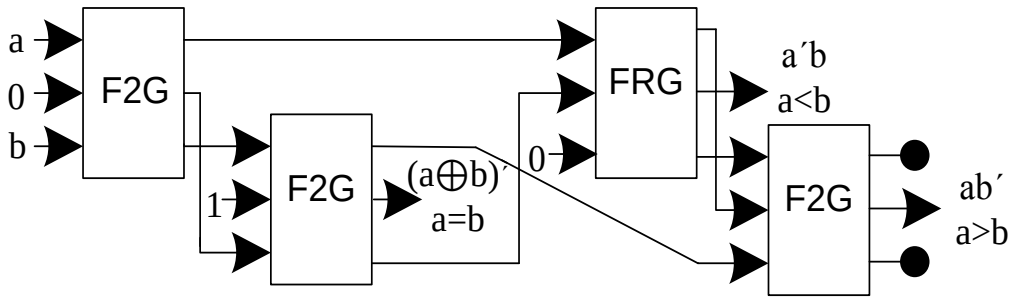


Fig. 10: Proposed reversible fault tolerant 1-bit comparator

Considering the trivial case i.e., n=1 we have 1-bit comparator. Fig. 10 shows the block diagram of the proposed reversible fault tolerant 1-bit comparator. From this we find that the 1-bit reversible fault tolerant comparator is realized with 3 constant inputs and 2 garbage outputs. These are the minimal parameter for a single bit reversible fault tolerant comparator which is proved in the following theorem.

4.2 Theorem

A reversible fault tolerance one-bit comparator can be realized with at-least 3 constant inputs and 2-garbage outputs.

Proof

Fig. 10 is the proof for the existence of a One bit reversible fault tolerant with 2 garbage output and three constant inputs. Next, we want to prove that it is not possible to realize a reversible fault tolerant 1-bit comparator fewer than 2 garbage outputs and 3 constant inputs.

The 1-bit comparator has two 1-bit inputs. Let these inputs be ***a*** and ***b***. Then, its outputs are ***a<b***, ***a=b***, and ***a>b***. Let named these o; i.e., total of three outputs. Since, any reversible circuit should have equal number of input-output; hence reversible comparator requires at least one constant input. The value of this constant input (C_0) can be either 0 or 1. Table I(A) and (B) shows the approximate truth table of the reversible comparator with constant input set to 0 and 1, respectively.

Table I : Truth table of reversible fault tolerant 1-bit comparator with 1-constant set to (A) 0 (B) 1.

(A)

Input			Output		
C_0	*a*	*b*	*P = a>b*	*Q = a<b*	*R = a=b*
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	0	0	1

(B)

Input			Output		
C_0	*a*	*b*	*P = a>b*	*Q = a<b*	*R = a=b*
1	0	0	0	0	1
1	0	1	0	1	0
1	1	0	1	0	0
1	1	1	0	0	1

Table I shows that the different input combinations (shaded rows) maps to identical outputs. In other words it violates one-to-one mapping property of reversible logic. Thus, at least one more constant input is needed (total of two constant inputs) which produce at least one garbage outputs. The value of these constant inputs (C0 and C1) can be 00, 01, 10 or 11. Table II shows different input combinations (shaded rows) can map to different outputs with the help of the garbage output G0. In Table II (A) and (D), the input parity of both the shaded rows is even but output-parity without the value of the garbage output is odd which implies that if it tries to maintain one-to-one mapping it can't maintain the parity. In other words, here both garbage outputs should be 1 if it tries to maintain the parity which violates one-to-one mapping.

Table II : Truth table of reversible fault tolerant 1-bit comparator with 2-constant set to (A) 00 (B) 01 (C) 10 (D) 11.

(A)

Input				Output			
C_0	C_1	a	b	P	Q	R	G_0
0	0	0	0	0	0	1	
0	0	0	1	0	1	0	
0	0	1	0	1	0	0	
0	0	1	1	0	0	1	

(B)

Input				Output			
C_0	C_1	a	b	P	Q	R	G_0
0	1	0	0	0	0	1	
0	1	0	1	0	1	0	
0	1	1	0	1	0	0	
0	1	1	1	0	0	1	

(C)

Input				Output			
C_0	C_1	a	b	P	Q	R	G_0
1	0	0	0	0	0	1	
1	0	0	1	0	1	0	
1	0	1	0	1	0	0	
1	0	1	1	0	0	1	

(D)

Input				Output			
C_0	C_1	a	b	P	Q	R	G_0
1	1	0	0	0	0	1	
1	1	0	1	0	1	0	
1	1	1	0	1	0	0	
1	1	1	1	0	0	1	

In addition, Table II (B) and (C) show that the input parity of both the shaded rows is odd and the output-parity without the value of garbage output is odd as well. Thus, both garbage outputs should be 0 if it tries to maintain the parity which also violates one-to-one mapping. Therefore, reversible fault tolerant comparator requires at least one more constant input (three constant inputs in total) which produce at least one more garbage output (two garbage outputs in total).

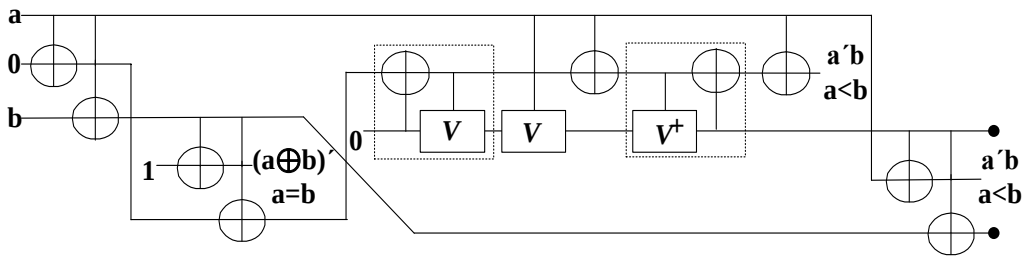


Fig. 11: Quantum realization of proposed 1-bit comparator.

Fig. 11 shows the quantum realization, transistor circuit and corresponding simulation result of the proposed 1-bit comparator. Based on this single bit design (as schema) an algorithm for the proposed reversible fault tolerant n-bit comparator is shown in Algorithm 1.

4.3 Algorithm for proposed1-bit Reversible Fault Tolerant Comparator

Algorithm 1: Algorithm for proposed One-Bit fault tolerant reversible circuit.

Input : Data a (a_0, a_1, a_2, …, a_n) and b (b_0, b_1, b_2, …, b_n)
Feynman double gate (F2G) and Fredkin gate (FRG).

Output : n-bit reversible fault tolerant comparator circuit.

Begin
Begin Procedure SBRFC (a, b, F2G, FRG)
i = input, o = output
for j→0 **to** n-1 **do**
  a → first.i.F2G$_j$, 0→ second.i.F2G$_j$
  b → third.i.F2G$_j$, first.o.F2G$_j$ → first.i.FRG
  for k ← 0 **to** n-1 **do**
    third.o.F2G$_j$ → first.i.F2G$_k$,1→second.i.F2G$_j$
    second.o.F2G$_j$ → third.i.F2G$_k$, third.o.F2G$_k$ →
    second.i.FRG, first.o.F2G$_k$ → third.i.F2G
  end for
  0→ third.i.FRG, third.o.FRG → first.i.F2G
  first.o.FRG → second.i.F2G
end for
return F2G$_2$.second.o, FRG.second.o and F2G$_3$.second.o as desire outputs and remaining outputs as garbage.
End Procedure
for m →1 **to** n **do**
 call SBRFC (a_{n-1}, b_{n-1}, F2G, FRG)
  for p →1 **to** n/2 **do**
    SBRFC$_p$.o → first.i.FRG$_p$, SBRFC$_{p-1}$.o →
    second.i.FRG$_p$, 0→ third.i.FRG$_p$
  end for
for q →1 **to** n **do**
  if (q<n)
    FRG.third.o → first.i.F2G$_q$, SBRFC$_{q+1}$.o →
    second.i.F2G$_p$, 0→ third.i.F2G$_p$
  else
    F2G$_{q-1}$.o → first.i.F2G$_q$, 1 →second.i.F2G$_q$,
    second.i.F2G$_{q-1}$ → third.i.F2G$_q$
 end if
  return first.o.F2G$_{n-1}$, second.o.F2G$_n$, third.o.F2G$_n$ as desire outputs and remaining outputs as garbage.
end for
End

Initially Algorithm 1 builds the circuitry for the proposed reversible fault tolerant single bit comparator which is shown insider the procedure SBRFC (lines 2 to 14). Then the algorithm makes the larger circuitry making a linear call to the SBRFC procedures. From this we find that, it requires n number FRG gates and 2n number of F2G gates in addition with n number of n-1 bit reversible fault tolerant circuit for an n bit reversible fault tolerant comparator. Finally line 26 returns the outputs. According to this algorithm the block diagram of the two-bit comparator is shown in Fig. 12.

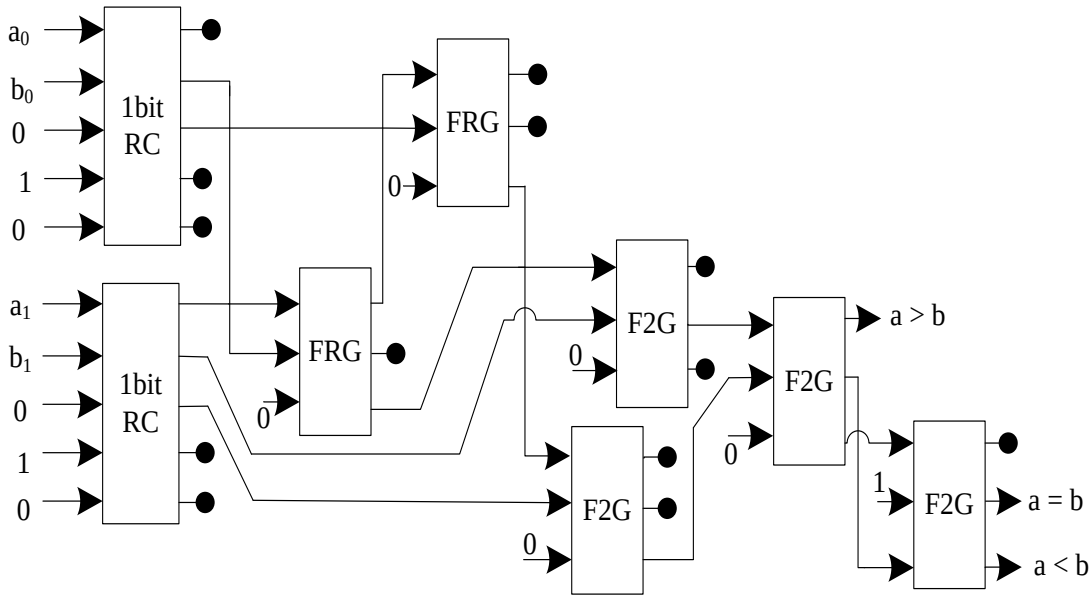


Fig. 12: Proposed 2-bit comparator's block diagram

4.4 Lemma

Let GT, GO, QC, HC, CPD be the number of gates, garbage outputs, quantum cost, hardware complexity and critical path delay for the proposed reversible fault tolerance *n*-bit comparator, respectively ($n \geq 1$). Also let α, β and γ be hardware complexity for the two input EX-OR, AND and NOT calculation, respectively. Then,

$$GT = 3n+4$$
$$GO = 3(n+2)+1$$
$$QC = 5(4n+5)$$
$$HC = (6n+8)\,\alpha + 4(n+1)\,\beta + 2(n+1)\,\gamma$$
$$CPD = n+4$$

4.5 Summary

This chapter detailed the design and working procedures of the proposed reversible fault tolerant 1 to n-bit comparator circuit. Here, several lower bounds on the number of garbage outputs, constant inputs and quantum cost of fault tolerant logic circuits are proposed for reversible fault tolerant comparator circuit. Finally construction procedure and algorithm are proposed for the implementation of proposed reversible fault tolerant comparator circuit. It has also been evidenced that the proposed components are optimized greatly from the existing components.

Chapter 5

Performance Evaluation of the Proposed Method

In the previous chapter, the performance of the components of reversible fault tolerant comparator circuit and the existing components of reversible comparator circuits been shown. This chapter provides the overall performances of the proposed reversible fault tolerant scheme with the existing reversible methods. The performance of the proposed method is evaluated by the required number of gates, garbage outputs, constant inputs and quantum cost.

5.1 Comparison

Here, in this section we have compared four important components between our proposed 1-bit design and conventional n-bit comparator designs. We have compared the number of reversible gates used in each designs, number of constant inputs, number of garbage outputs and quantum costs. Compare to all other conventional designs out proposed 1-bit comparator circuit is much better in quantum cost and it has the minimal number of constant inputs and garbage outputs. The comparison is shown in the following table:

Table III: Comparison between proposed reversible fault tolerant comparator circuit and conventional reversible fault tolerant comparator circuits.

One bit comparator design using	Reversible gates	Garbage outputs	Constant inputs	Quantum cost
Proposed Design	**4**	**2**	**3**	**11**
Existing Design [11] (*Toffoli and BJN Gates*)	4	2	3	16
Existing Design [21] (*Fredkin and BJN Gate*)	5	6	7	23
Existing Design [28] (*TR and BJN Gates*)	3	2	3	12

5.2 Summary

A comparator circuit compares two inputs A and B that gives three outputs as A>B (where, A is greater than B), A<B (where, A is less than B) and A=B (where, A is equal to B). Comparators are often used, for example, to check whether an input has reached some predetermined value. As we shown, the better performance of proposed methods of the circuit sequence counter and others so, we can say that the comparator will give the better performance than other existing methods.

Chapter 6

Conclusion

6.1 Conclusion

In this thesis an one-bit reversible fault tolerant comparator circuit is presented. For low power digital circuits and quantum computers this design is very efficient. Here we have used only Feynman Double Gate and Fredkin Gate to design these circuits. By the theorem we also proof that the circuit has been created with minimal number of constant input and garbage outputs. Here one circuit has been designed to perform less than, equal and garbage than calculation with only 3 Feynman Double Gates and 1 Fredkin Gate, where as other previously proposed circuits for these three calculations. Moreover, with this given design 2-bit, 4-bit to n-bit reversible fault tolerant comparator circuit can also be designed.

The proposed circuit will be useful for implementing the quantum computers, reconfigurable computer etc.

6.2 Future Work

The Reversible gates are used to implement Fault tolerant synthesis of comparator. The Reversible fault tolerant compactor is built using efficient design with minimum quantum cost, minimum garbage and minimum area and power overheads. The proposed design implementation of Reversible fault tolerant compactor has better performance as compared to existing designs in terms of number of gates used, Garbage outputs and Quantum Cost. Hence, it can be used for low power applications. In future, the design can be extended to any number of bits as Comparator and also for low power Reversible ALUs and Multipliers. ALU is most important part of a Processor. So we can design an efficient reversible ALU using this proposed Reversible fault tolerant compactor.

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