SIGNAL DEGRADATION IN HIGH SPEED SYSTEMS DUE TO CHIP BREAKOUT ROUTING CONSTRAINTS IN PACKAGE SHADOW REGION.

By

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Submitted to the

Department of Electrical and Electronic Engineering
Faculty of Sciences and Engineering
East West University

in partial fulfillment of the requirements for the degree of
Bachelor of Science in Electrical and Electronic Engineering
(B.Sc. in EEE)

Fall, 2008

Approved By

Dec 24th 2008

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24.12.08

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Abstract

The High Speed Systems involves electrical performance of the wires and other packaging structures used to move signals about within an electronic product. In these early days of modern VLSI era, digital chip circuit design and layout were manual processes. The application of automatic synthesis techniques allowed designers to express their designs using high-level languages and apply an automated design process to create very complex designs. Such performance is a matter of basic physics and as such has remained relatively unchanged since the inception of digital computing devices. As circuit shrinks in accordance with Moore's law, several signal integrity issues are becoming critical. Several of these issues are ringing, crosstalk, ground bounce and power supply noise that can cause systems to fail particularly at high frequencies.

The socket breakout region requires important design consideration when signals are routed through it. In this region the trace width and trace spacing between them have to be decreased to maintain keep out region which are critical for manufacturing boards. However, decreasing trace space and width means increasing impedance. The high speed designer should maintain this thing very carefully as a matter of cost effective.

In our High Speed System analysis we use H-Spice and ADS (Advanced Design System) as a simulator. In this simulator we draw a schematic diagram of a high speed system and run the system in high frequency and observed the eye opening to validate data integrity. As per visual observation the system runs smoothly at GHz range for specific design consideration in the socket shadow region of a CPU based system.

A signal integrity analysis methodology that performs high speed circuit simulation analysis is done in this paper. The use of the distributed circuit simulation technique drastically reduces the simulation time for lumped circuit components. This program can promptly simulate practical package, power ground planes and signal traces. While considering Signal Integrity problems such as signal delay, distortion, reflection coupling and power/ground noise.

To meet our project requirement it would be necessary to systematically identify and quantify each aspect of the design process. This had to be done in terms of the effects on the system and the performance at 5 Gbps as well as higher speeds. In addition to the theoretical study there was also going to have to be a practical method developed that would show the required performance was not only met but exceeded. This was necessary to validate to what extend the theory converged with practice and also to ensure that the final constructed High Speed System was free from any possible system errors when running under maximum design conditions. The eye diagram was used to observe signal transmission at different frequencies, especially in the 1 to 5 GHz range.

Acknowledgements

It is a pleasure to thank the many people who made this thesis possible.

It is difficult to overstate my gratitude to my undergraduate thesis supervisor, Dr.Ishfaqur Raza. With his enthusiasm, his inspiration and his great efforts to explain things clearly and simply, he helped to make mathematics fun for me. Throughout my thesis writing period, he provided encouragement, sound advice, good teaching, good company and lots of good ideas. I have been lost without him.

I would like to thank many people who have taught me mathematics: my high school math teachers (specially Mr. Abdul Khaleq, Mr. Moazzem Hussain (Motijheel Model High School)), Mrs.Sharmeen Kabir, Late.Mrs.Shahida Khanom, Mrs. Afroza Banu (Dhaka City College)), my undergraduate math teachers especially Prof.Ajit K. Mojumder, Dr.Gaurango Dev Roy and Mrs.Anindita Paul. For their kind assistance with writing letters, giving wise advice, helping with various applications and so on. I specially remember Dr.Ruhul Amin, Dr.Ghulam Rahman and Dr.Anisul Haque who inspired me lot and giving wise advice. I wish to thank in addition Dr. Khairul Alam, Sarwar Jahan, Kazi Zamir Uddin Ahmed, Mustafa M. Hussain, Tahseen Kamal and Rumana Rois.

I am indebted to my many student colleagues for providing a stimulating and fun environment in which to learn and grow. I am especially grateful to Jubayer, Shushanto, Asaduzzaman, Arnab, Ophelia, Laila, Rezowana, Galib, Mehrab, Atique and Shajib at EWU and to Fuad Hussain, Sarwar Alam, Salman Zaman, A.B.M. Zakir Hussain and Glory at BU and my undergraduate best friend (specially Hasan, Rakesh) for helping me get through the difficult times, and for all the emotional support, entertainment and caring they provided, also Tareq for his helping hand about this thesis.

I am grateful to the secretaries and librarians in the Engineering departments of EWU for helping the department to run smoothly and for assisting me in many different ways.

I wish to thank my entire extended family for providing a loving environment for me. My brothers, my sister, my cousin and some uncles were particularly supportive.

Lastly and most importantly, I wish to thank my parents, they bore me, raised me, supported me, taught me and loved me. To them dedicate this thesis.

Authorization page

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1. Introduction

Signal Integrity, known as SI, refers to electronic circuit tools and techniques that ensure electrical signals are of sufficient quality for proper operation. In fact, signal integrity tools attempt to identify and remove effects that cause a design to malfunction due to distortion of the signal waveforms. In Integrated Circuits(IC) signal integrity problems is noise induced by neighboring connections or crosstalk. In case of CMOS technology it is primarily due to coupling capacitance, mutual inductance, non-ideal gate operation and other sources. Induced noise can have many drastic consequences for digital designs likewise design work become incorrect, make the design slower etc. In the realm of high speed design, signal integrity has become a critical issue and is posing increasing challenges to the design engineers. Many signal integrity problems Phenomena in nature and hence related to the Electro Magnetic Interference (EMI).The term Signal Integrity (SI) addresses two concerns in the electrical design aspects – the timing and the quality of the signal. Does the signal reach its destination when it is supposed to? And also, when it gets there, is it in good condition?

The cost of such a failure is very high and includes so many costs. Therefore proper automation tools have been developed to analyze, prevent and correct these problems. The application of automatic synthesis techniques allowed designers to express their designs using high-level languages and apply an automated design process to create very complex designs.

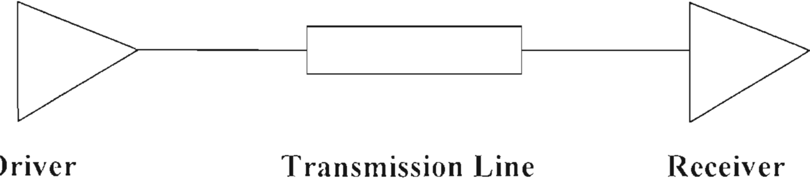
Signal Integrity affects all levels of electronics packaging including but not limited to the IC. For High Speed digital products at the level of an IC package or printed circuit board (PCB) main issues of concern are ringing, crosstalk and power supply noise. Without considering these typical issues High Speed Digital products can fail to operate at the design stage. However, such performance is a matter of basic physics and has remained relatively unchanged since the inception of digital computing devices.

Signal Integrity primarily involves the electrical performance of the wires and other packaging structures used to move signals about within an electronic product. In the modern VLSI era, digital chip circuit design and layout were manual process. The use of abstraction and the application of automatic synthesizer allow the designer to express their designs using high-level language and apply an automated design process to create very complex design.

In high Speed systems, the components are shrinking day by day in this era of nanotechnology. In line with this the CPU capacity is increasing as Moore's law predicted. This has resulted in the increase of number of input and output signals while the size of CPUs remains pretty much constant. Thus Pin density is large decreasing the pin pitch. Therefore, in a small area of the socket, larger number of signal has to be routed out in this shadow region. To enable this, the trace width and differential pair space has to be decreased to support pin keep out region. As we have to decrease trace spacing and trace width, the line impedance increases. This causes reflection, ringing and changes the quality of the signal. As a result of narrowing the trace width, signal integrity quality decreases. We use the eye concept of a signal data stream to analyze the signal quality in the CPU transmission line system.

2. TRANSMISSION LINE THEORY

Signal Integrity is a kind of configuration where information i.e. signals is transferred across a link from a driver to receiver. In fact, a binary signal which alternates between two voltages, one representing a 1 and another representing a 0.The signal that passes from the transmission line should maintain quality and fidelity. The transmission line should be able to carry successful information from driver to receiver end.



Driver **Transmission Line** **Receiver**

Figure 1: Signal Integrity

As per efficient point to point transmission of power and information the source energy must be directed or guided. In our project we use parallel- plate transmission line; this type of transmission line consists of two parallel conducting plates separated by a dielectric slab of uniform thickness. At microwave frequencies parallel plate transmission lines can be fabricated inexpensively on a dielectric substrate using printed circuit technology, known as stripline.

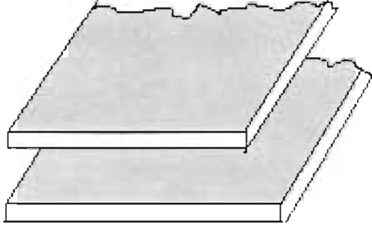


Figure 2: parallel-plate transmission line.

As a signal propagates through the conductors each new section acts electrically as a small lumped circuit element. According to transmission line which is known as lossless transmission model. The equivalent circuit of a transmission line has just inductance and capacitance. These elements are uniformly distributed down the length of the line as shown in the figure-

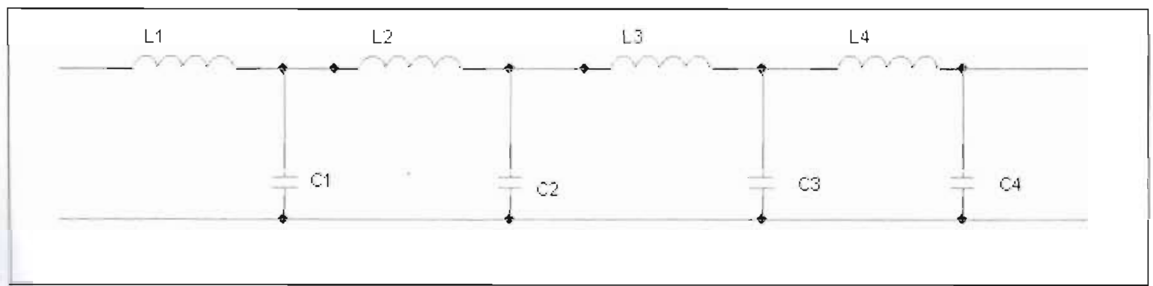


Figure 3: Equivalent circuit model of a lossless transmission line.

From this circuit model, the two important terms that characterize
A transmission line can be derived: the velocity of a signal (v) and the characteristic impedance (Zo).

$$V = 1/\sqrt{L} \qquad \text{and} \qquad Z_0 = \sqrt{L/C}$$

Where,
L=Inductance per length
C=Capacitance per length.

But, when loss is significant, the effects of the series resistance (R) and the dielectric conductance (G) should be included fig: 6 shows the equivalent circuit model of lossy transmission line, with distributed "lumps" of R, L, C elements.

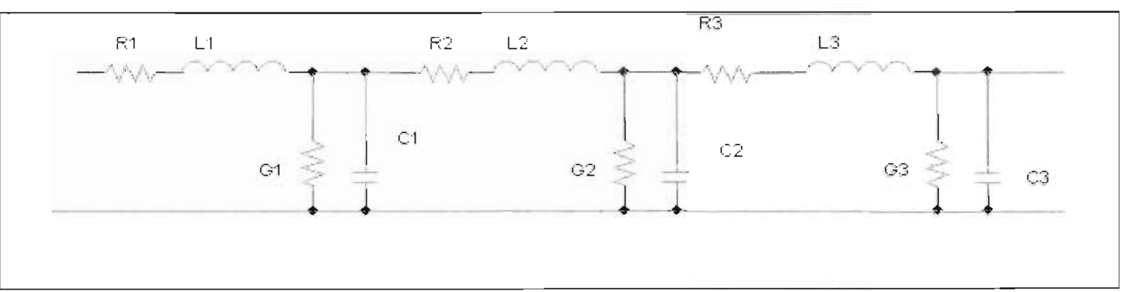


Figure 4: Equivalent circuit model of a lossy transmission line.

These elements are the equivalent circuit model for the lossy transmission line. In a transient simulation, these elements automatically accounts for frequency-dependent characteristic impedance, dispersion (frequency dependence in the velocity) and attenuation. The most common transmission line are microstrip, stripline, coax, wire over ground and twisted pair, we consider microstrip, stripline in our model.

The differential transmission line it depends on the following four parameter:

R, resistance per unit length, in Ω /m.
L, inductance per unit length in H/m.
G, conductance per unit length in S/m.
C, capacitance per unit length in F/m.

Here, both R and L are series components and G and C are shunt elements. In table 1, the R, L, G, and C of a ideal transmission line is given. In the table width=w, separation=d, magnetic permeability=μ, frequency=f, permittivity of a medium= ε, electrical conductivity= σ.

Table 1: Distributed parameters of parallel-plate transmission line.

Parameter	Formula	Unit
R	$2/w\sqrt{\Pi . f . \mu / \sigma}$	Ω / m
L	$\mu . d / w$	H / m
G	$\sigma . w / d$	S / m
C	$\varepsilon . w / d$	F / m

Microstrip line is one example of a class of configurations involving planar conductors of finite widths on or within dielectric substrates; they are usually employed as device interconnects for microelectronic circuitry. The microstrip configuration consists of a thickness d and of permittivity έ =εr*εo, where εo permittivity of free space and εr is the permittivity of that material, sandwiched between a conducting ground plane and a narrow conducting strip of width w.The region above the strip is air or lower dielectric permittivity.
The development of solid-state microwave devices and systems has led to the wide spread use of a form of parallel plate transmission lines called microstrip lines or simply known as striplines.Todays high performance PCB traces are manufactured as microstrips or striplines.A microstrip transmission line consists of a conductive trace of controlled width on a low –loss dielectric mounted on a conducting ground plane.The dielectric usually made of glass reinforced epoxy such as FR-4 or polyimide glass for very high frequencies. There are several configuration of PCB microstrip:

(1) Surface microstrip.
(2) Embedded microstrip.
(3) Coated microstrip.

2.1. Single ended microstrip transmission line:

Single-ended transmission lines are the basic way to connect two high speed devices. In the single-ended transmission line a single conductor connects the source of one device to the load of another device. The reference (ground) plane provides the signal return path. The impedance value is determined by the width (w) of the trace, the value of the board dielectric constant (**εr**), the height of the dielectric constant (h) and the thickness (T) of the dielectric.Figure1 shows the parameter.

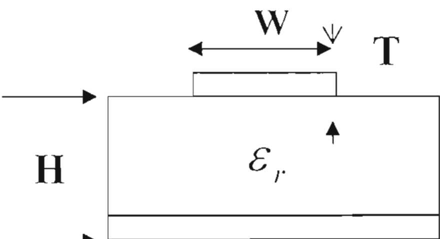


Figure 5: **Single ended microstrip transmission lines.**

2.2. Differential micro strip transmission line:

According to the figure 2, w1is the width of the trace one and w2 is the width of the trace two, S is the space between the two traces, h is the height of the dielectric constant and **εr** is the value of the board dielectric constant. In case of differential transmission line differential impedance should be Zdiff should be 90 ohms and single line trace impedance should be Zo 50 ohms.

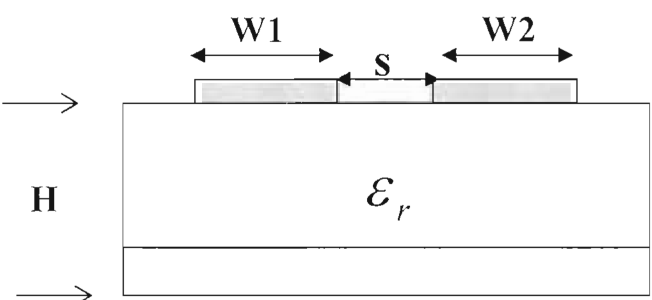


Figure 6: **Differential microstrip transmission lines.**

Signal Integrity issues came whenever unwanted noise becomes detectable or interferes with the signal we are concerned with. Suppose if our home audio system provides 60 Hz hum (very low frequency) then definitely it's a signal integrity problem. Signal integrity solutes this problem.

1. The key to efficient high-speed product design is to take advantage of analysis tools that enable accurate performance prediction. Use measurements as a way of validating the design process, reducing risk and increasing confidence in the design tools.

2. Each interconnects in a transmission line with a signal and a return path, regardless of its length, shape or signal rise time. A signal instantaneous impedance at each step along its way down an interconnect. Signal quality is improved of the instantaneous impedance is constant as in a transmission line with a uniform cross section.

The goal of signal integrity analysis is to ensure reliable high-speed data transmission. In a digital system, a signal is transmitted from one component to another in the form of logic 1 or 0. A good SI tool should contain the following key components: 2D field solvers for extracting RLGC matrices of single/couple transmission lines; single/couple lossy transmission line simulator; 3D field solvers for wirebonds, vias, metal planes; behavior modeling of drivers and receivers. They should also take physical layout files as input data and post process simulation results in time domain and frequency domain.

Table 2: Major Signal Integrity tools.

Company	Tool	Function
Agilant Technology	ADS	Signal integrity, Patch antenna simulation.
Ansoft	SI 2D,SI 3D,PCB Signal Integrity	2D, 3D static DC EM simulation extracts inductance and capacitor, PCB pre and post route SI analysis.
Mentor Graphics	IS_Analyzer	Delay, crosstalk simulation.
Sigrity	SPEED 97/SPEED 2000	Power/Ground noise simulation with couple lossy transmission line analysis.
Cadence	SPECCTRA QUEST	SI simulation: transmission line simulation, power plane builder.

The basic components in the design of a High-Speed computing system are Driver (silicon die), Break out, package transmission line, plated through hole (PTH), solder ball, CPU socket, Printed Circuit board (PCB), Receiver. In the simulation setup of a system, these components are modeled.

3. OBJECTIVES.

In this thesis we study the effect of socket breakout region on signal integrity in a High speed transmission system, when signal propagates at Giga hertz frequency. Main objective of Signal Integrity is how a signal passes from Driver to Receiver end accurately i.e. how successful the information passes through Driver to Receiver end. We have to ensure the reliable operation of a digital design by predicting, measuring and modifying the behaviors of electrical signals on interconnects between electronic components. In our Printed Circuit Board (PCB)/Integrated Circuit packaging electrical impedance is an important issue. In a high – speed IC package or Printed Circuit Board (PCB) environment digital signal pathways have low impedance, meaning that the circuit impedance lies below the 377 ohm impedance in this typical dielectric material. Contrast that with the typically high impedance (> 377 ohms) possessed by digital IC circuits on silicon die. As a consequence of low impedance in the Printed Circuit Board/Integrated Circuit packaging printed Circuit Board signal traces (single line, Differential line microstrip/ stripline) carry much more current compare to the VLSI (Very Large Scale Integration) chips. This larger current induces crosstalk, primarily in a magnetic or inductive mode as opposed to a capacitive mode. To overcome this crosstalk Signal Integrity (SI) engineers /digital Printed Circuit Board (PCB) designers must remain acutely aware of not only the intended signal path for every signal. The signal itself and its returning signal current path are equally capable of generating inductive crosstalk. A second difference between communication within an IC and communication in a high– speed IC package or PCB environment involves the signal conductor resistance (typically 100 um or more in width, have a small series resistance typically 0.1 ohms/cm.) but on die conductors have much more resistance. Since this negligible resistance PCB conductor is characterized primarily by its capacitance and inductance per unit length. Together, these considerations determine the traces characteristic impedance. It is important to mention in a PCB single lines characteristic impedance is 50 ohms and differential lines 90 ohms. In the package shadow region differential lines impedances (> 100 ohms) because of trace space and trace width decreases. Thus one important thing to mention if we decrease trace space impedance increases.

4. Model And Simulation.

This is model in a High-Speed design system, where the system components are Driver, Package Transmission Inept, and Solder ball, CPU socket, Mother Board. The Figure shows a block diagram.

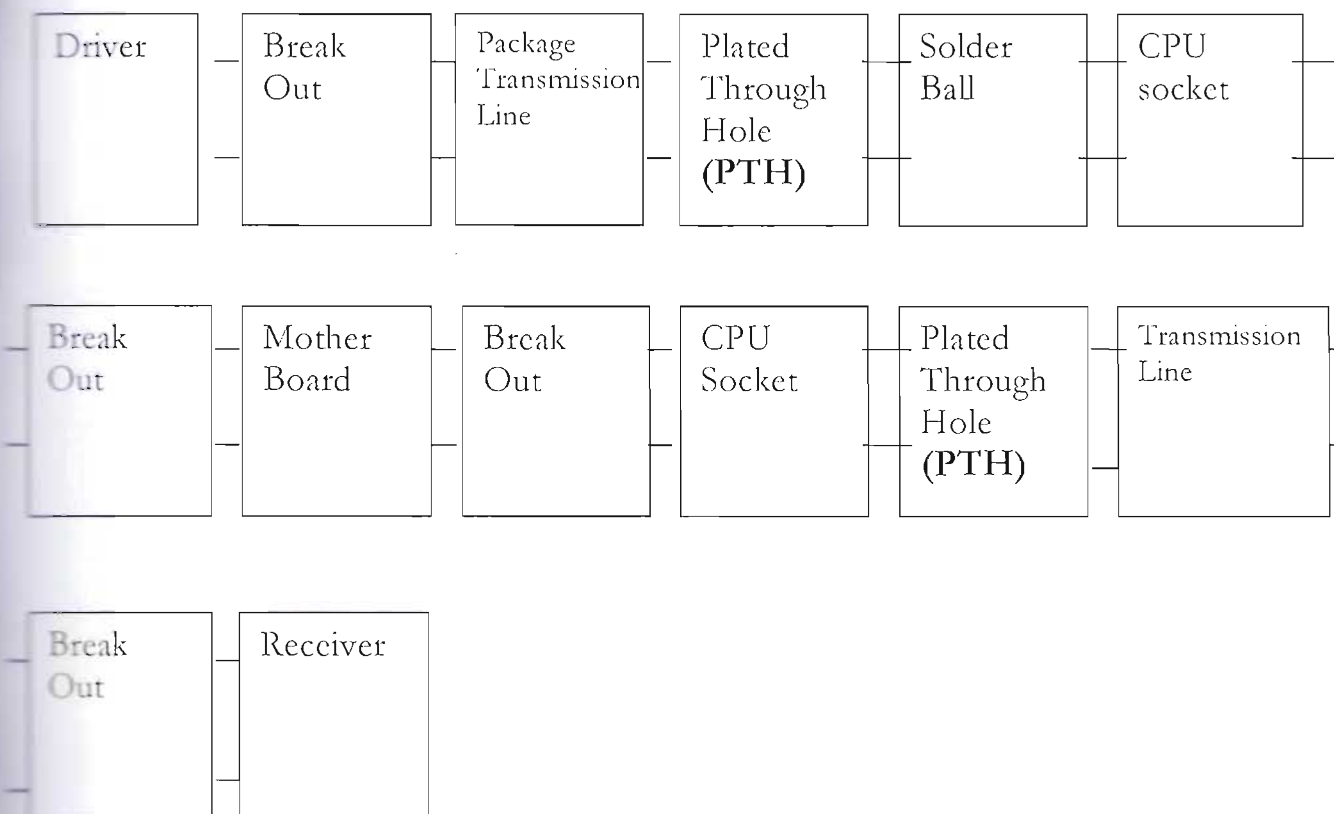


Figure 7:W element passing through Driver to Receiver end. (Block Diagram).

According to this H-spice analysis we construct a three signal conductors and a reference conductor. These parameters extracted from the field solver, laboratory experiments or packaging specifications supplied by vendors. According to these parameters –

1. Capacitance/length.Each conductor has a capacitance to all other conductors.

2. Conductors/length.Each conductor has a conductance to all other conductors due to dielectric leakage.
3. Inductance/length.Each conductor has a self inductance and mutual inductances to all other conductors in the transmission line.
4. Resistance/length.Each conductor has two resistances, high frequency resistance due to skin effect and bent wires and DC core resistance.

4.1. RLGC Model Extraction

These RLGC components can be derived in a matrix form which is known as RLGC matrix.

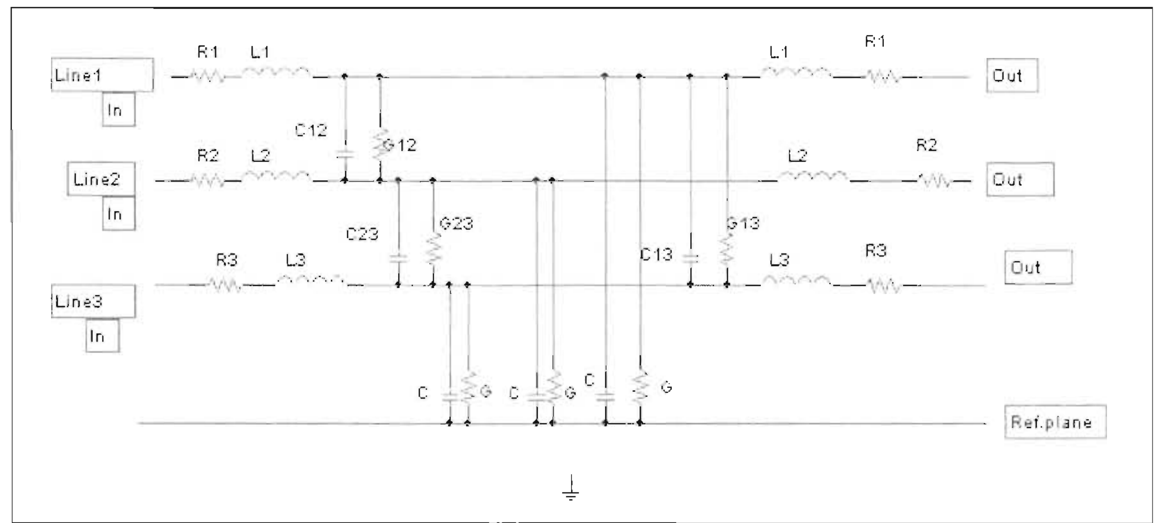


Figure 8: **Transmission line RLGC components of 3 conductors and a reference plane.**

In a two line Transmission line (N=2), there are RLGC component. Where R=Resistance, L=inductance, G=Conductance and C=Capacitance. For our simulation procedure we use H-spice. For W modeltype RLGC component the RLGC matrix is given here-

$$L_0 = \begin{bmatrix} L_{11} & \\ L_{21} & L_{22} \end{bmatrix}$$

Here,L11 is the first component(Row=1,Column=1) of the matrix,L11=2.569762e-007.Similarly,L21 is row 2 column 1 component and L22 is the row 2 column 2 component of the matrix.

$$C_0 = \begin{bmatrix} C_{11} & \\ C_{21} & C_{22} \end{bmatrix}$$

Similarly, C11, C21 and C22 is row 1 column 1 and row 2 column 1 and row 2 column 2 of the matrix.

$$R_0 = \begin{bmatrix} R_{11} & \\ R_{21} & R_{22} \end{bmatrix}$$

Similarly, R11, R21 and R22 is row 1 column 1 and row 2 column 1 and row 2 column 2 of the matrix.

$$G_0 = \begin{bmatrix} G_{11} & \\ G_{21} & G_{22} \end{bmatrix}$$

Similarly, C11, C21 and C22 is row 1 column 1 and row 2 column 1 and row 2 column 2 of the matrix. Where the values of the RLGC matrix component are given here.

```
.MODEL mb_minz W MODELTYPE=RLGC, N=2
+ Lo = 2.569762e-007
+     3.510568e-008 2.550276e-007
+ Co = 1.443481e-010
+     -1.577618e-011 1.471304e-010
+ Ro = 3.437408e+000
+     0.000000e+000 3.437408e+000
+ Go = 0.000000e+000
+     0.000000e+000 0.000000e+000
+ Rs = 1.564327e-003
+     3.093692e-004 1.555904e-003
+ Gd = 1.511610e-011
+     -1.652078e-012 1.540746e-011
```

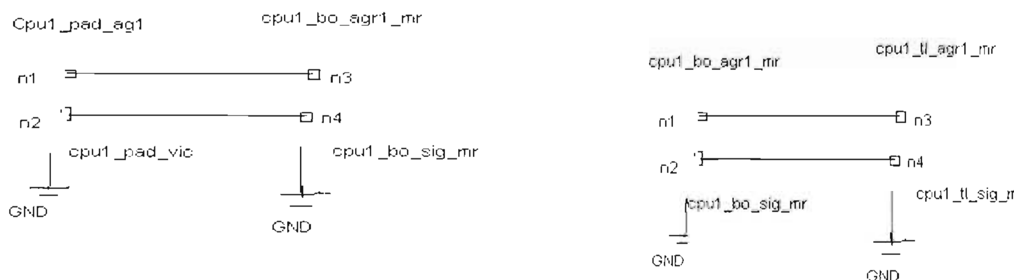
To explain the net list following thing should be clear .To put '*' sign means this line will not execute, ".param" means to define parameter as an example in our High speed design we define the Vdd value =1.5v, (My net list is given below.)Where, "$" symbol is used to put comments, so that beginner user can easily understood.".tran" means transient analysis which computes the circuit solution, as a function of time.Again to run the simulation there are few link file which need to be link through the main file i.e. ".include" command is being used for that purpose. To define nodes likewise node1, node2, node3 we use the following command circuit name and specify node name. The "+" symbol is used for continuity of the line. We use the "x" command for using sub circuit likewise "x_cpu1_socket". Again we use probe statement ".probe" to output variables.

5. Results and Analysis.

After running the simulation here is the program output. When analyzing the signal we use a pulse train of bits 010100110101011010101010101, which has a random mix of different bit combinations. The signal degrades away and the signal become round off in the receiver end. In fact the receiver can't detect information successfully. The signal that passes from driver to receiver comes across different system components. These components are modeled in the simulator using the following models. In H-spice simulation the models used are explained by the following diagram

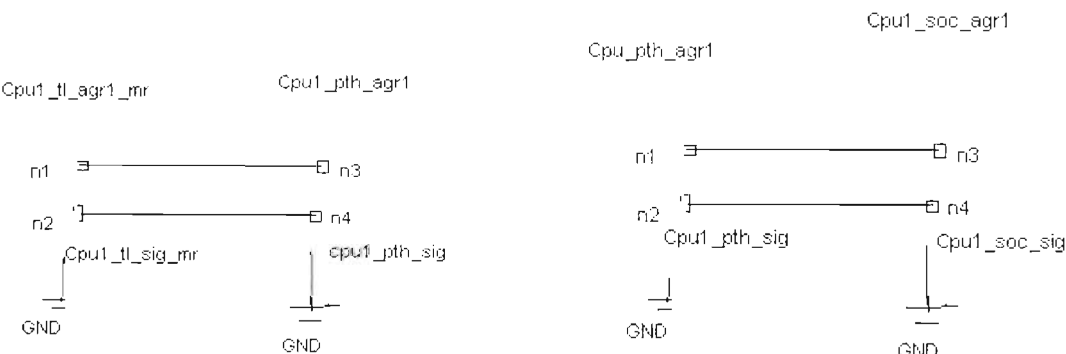
Where N=2 transmission line n1, n2, n3 and n4 are nodes and their common node ground is defined.

Driver (Silicon die.) **CPU package transmission line**

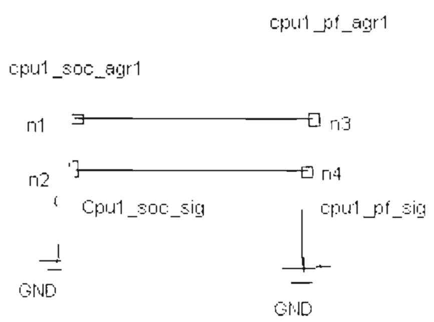


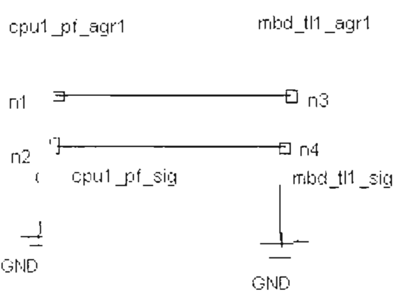
Here, n1= Cpu1_pad_ag1, n2=cpu1_pad_vic, n3=cpu1_bo_agr1_mr and n4=cpu1_bo_sig_mr.This pinfield portion where interconnection of different circuit components are shown. In the CPU package, nodes are defined n1= Cpu1_bo_agr1_mr, n2=cpu1_bo_sig_mr. n3=cpu1_tl_agr1_mr and n4=cpu1_tl_sig_mr.

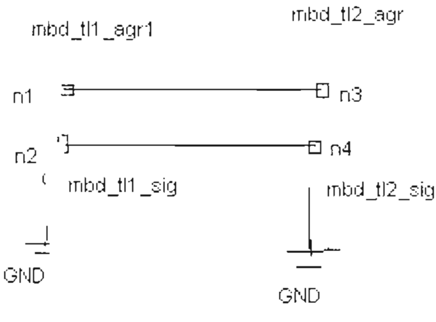
CPU plated through Hold **CPU socket**

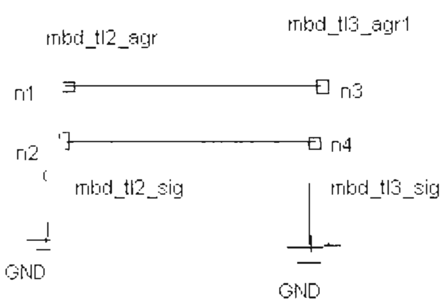


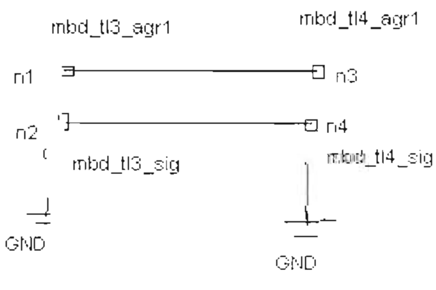
Motherboard (Cpu1 pinfield)

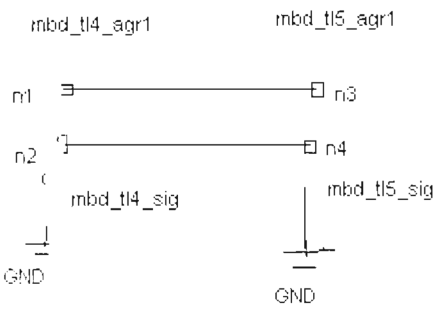


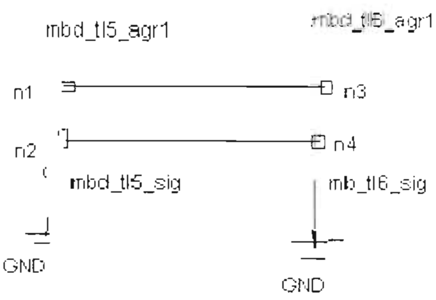


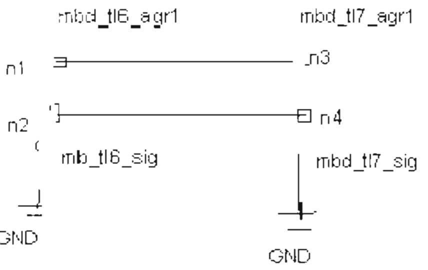






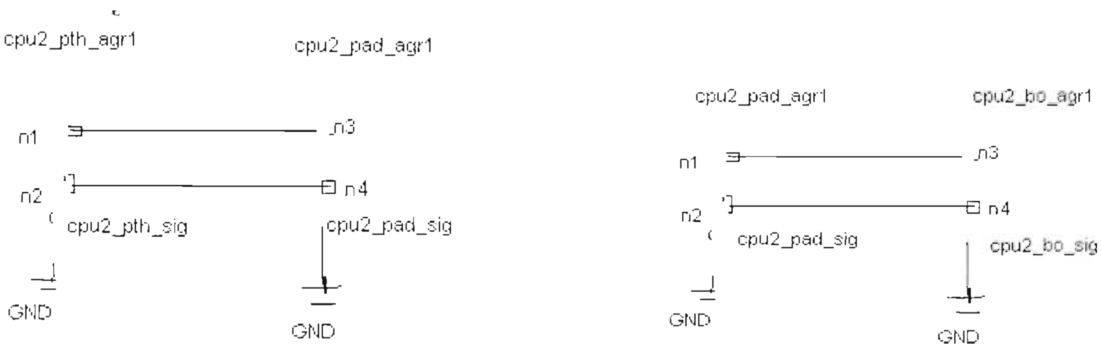






In this Pinfield portion, we call a func named " mb_minz "(H-Spice Netlist) where RLGC matrix is defined.Here, I analyze the pinfield portion, we can see there are mbd_tl1 to mbd_tl7 is defined in the H-Spice netlist and also call a subcircuit named "Zif_socket_couple".In the PKG (Package) folder there is a file named socket where it is defined "3 pin CPU socket model" for three pin there should be seven node where it defined in1, in2, in3, out1, out2, out3 and gnd.Thats why in the netlist portion there are seven trace Trace 1 to Trace 7.

CPU2 transmission line: **Receiver**



Here, nodes are defined n1= Cpu2_pad_agr1, n2=cpu2_pad_sig, n3=cpu2_bo_agr1 and n4=cpu2_bo_sig and common node ground. Thus the figure shows how the signal passes from driver to receiver end.

After running the simulation here is the program output. Where analyzing the signal we see the setup pulse train of bits 0101001101010110101010101 is given. The signal degrades away and the signal become round off in the receiver end. In fact the receiver can't detect information successfully. Here is the output of the when we call driver, there the node is defined cpu_test_pad1.

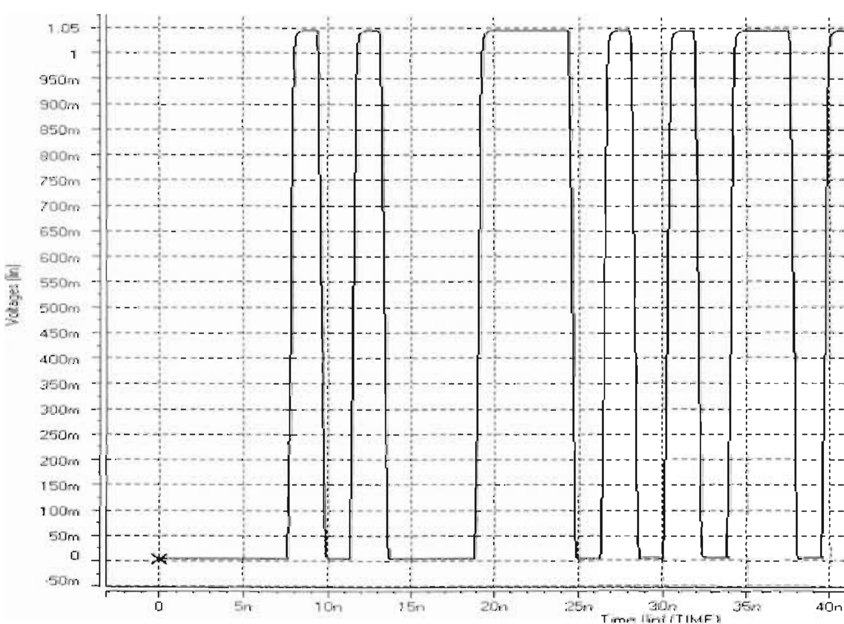


Figure 9: **V (cpu_test_pad1)**

In cpu1, we named a subcircuit x_cpu1_breakout_mr, where node4 is defined cpu1_bo_sig_mr.we can see how the signal degrades and became round off. When the signal passes from one node to another noise adds over signal thus it degrades.

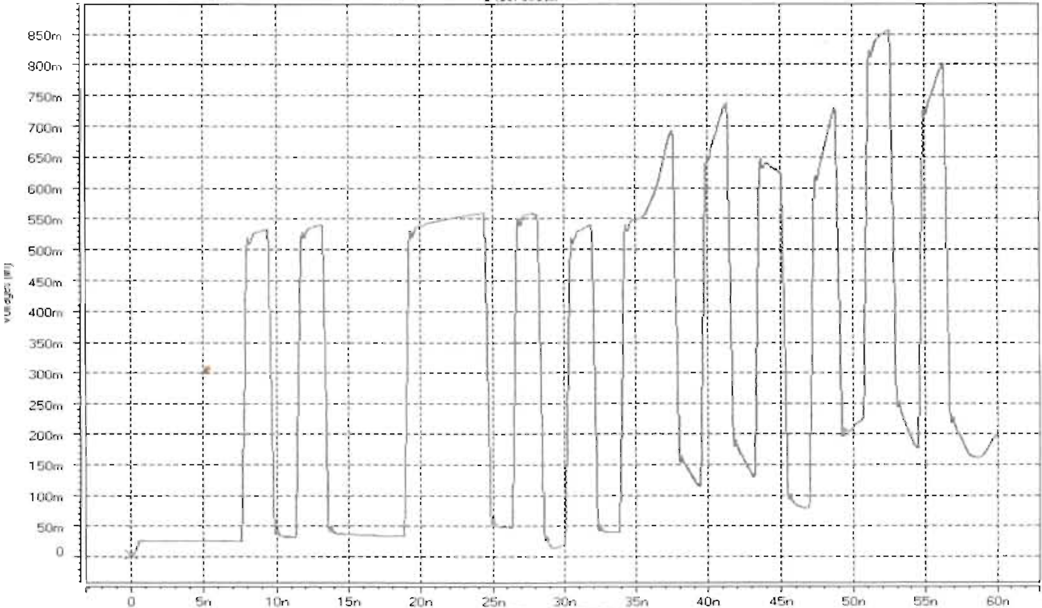


Figure 10: V (cpu1_bo_sig_mr.)

This out put is in the MB Trace1 portion, where the node4 is defined mbd_tl1_sig.The signal became more degraded and round off.

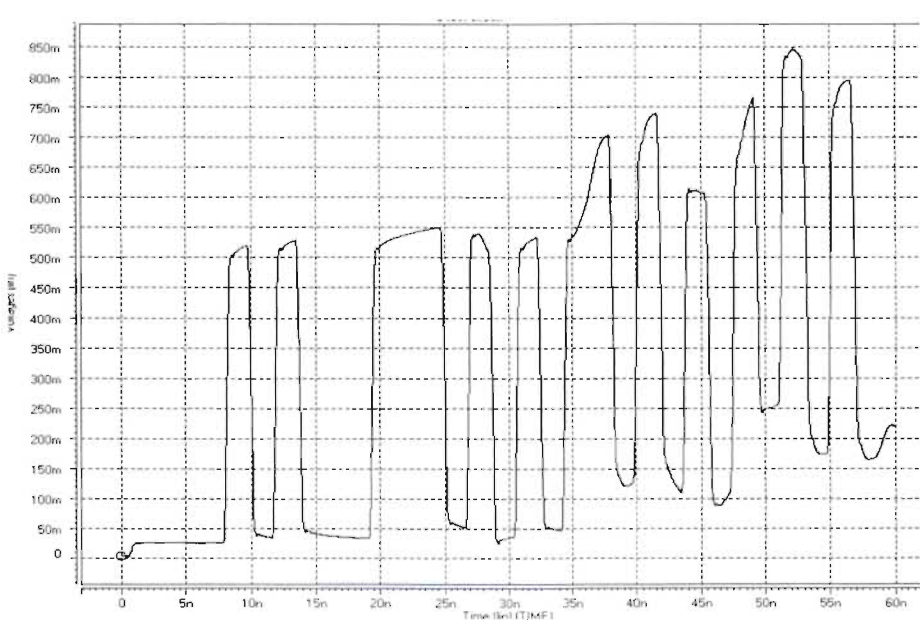


Figure 11:V (mbd_tl1_sig.)

this output is in the CPU2 Plated Through Hole (PTH) portion, where node 4 is defined cpu2_pth_sig. Here also the signal became more degraded and round off.

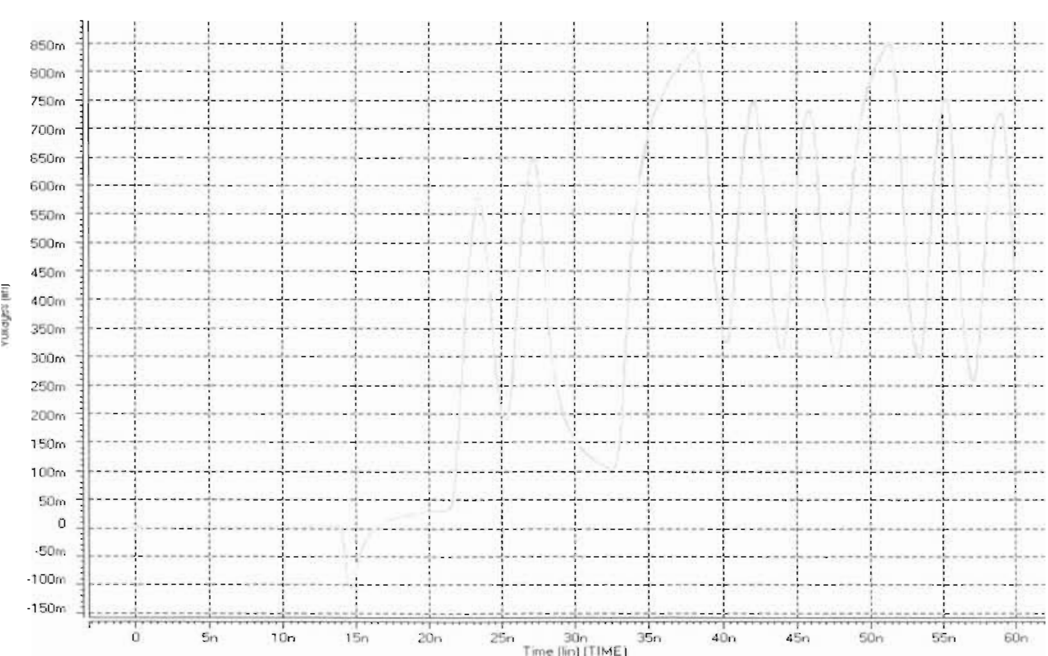


Figure 12: V(cpu2_pth_sig.)

This output is in the CPU2 package transmission line portion, where node4 is defined cpu2_pad_sig .Here we can see the quality of the signal is more degraded and more rounds off and also give a negative pulse. That means the receiver can't detect the whole information successfully.

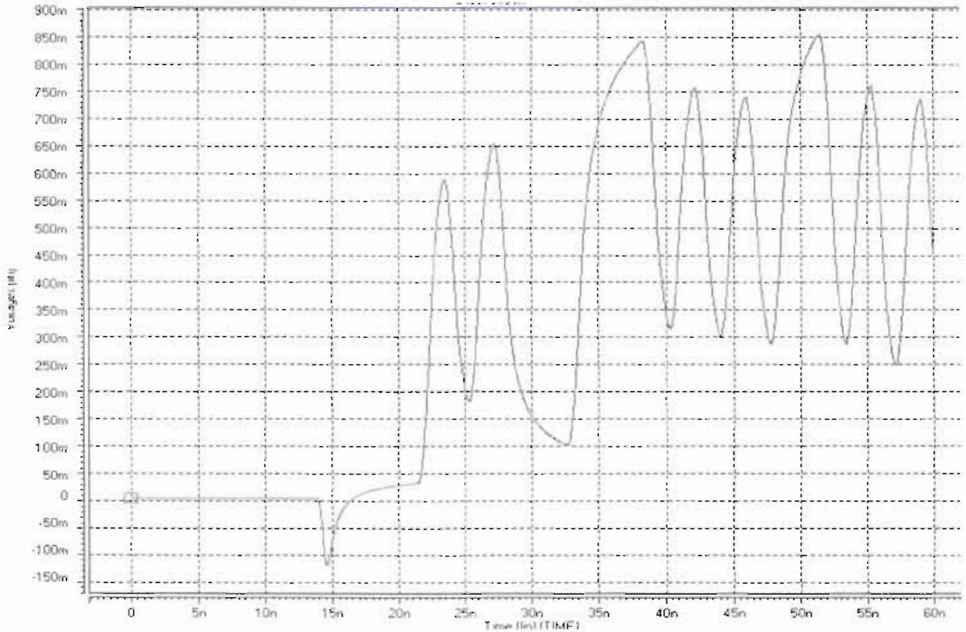


Figure 13: V (cpu2_pad_sig)

5.1. ADS analysis:

After analyzing the H-Spice we construct our design, fig- shows the block diagram of the design. We put the design in ADS where we choose transient time domain analysis where maximum time step is 1.0 nano sec and stop time is 100.0 nano sec.In our design we choose polyimide glass as typical dielectric materials whose relative dielectric constant Er= 4.2.Substrate thickness, H= 6 mil, Relative permeability=1, Conductor conductivity=1.0E+50, Cover Height, Hu=3.9E+034 mil,Conductor thickness, T=1.4 mils,Dielectric loss tangent, TanD=.005,Conductor surface roughness ,Rough=0 mil.

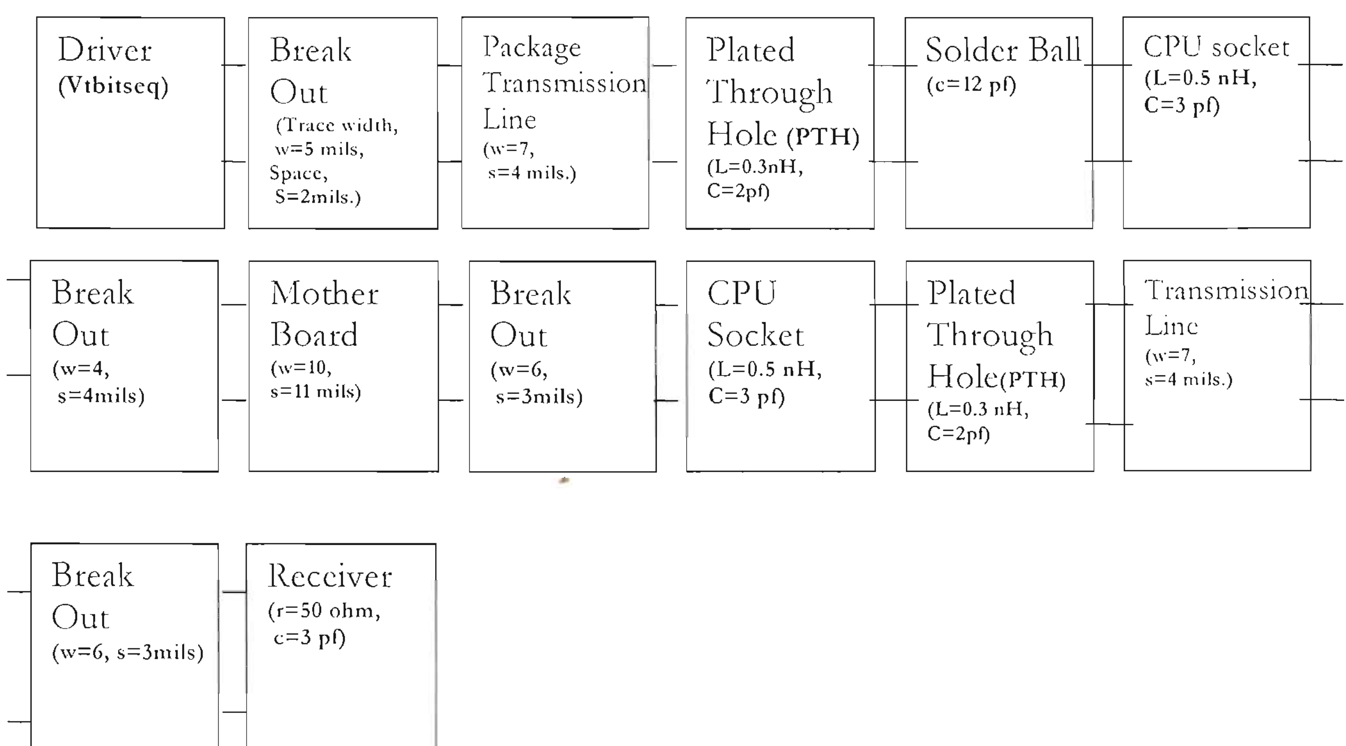


Figure 14: **High Speed Design. (Block Diagram)**

In our experimental setup we choose Vtbitseq (Voltage source, pseudo random pulse train bit defined at Continuous Time by Bit sequence) where rise time=1 nano sec, fall time is1 nano sec, experimental Bit seq "01011100110100001011" for source1 and "10100011001011110100" for source 2 as this is a differential line. Now constructing Break out reign we choose polyimide glass as typical dielectric material for microstrip, where trace width, w=5 mils and space s=2 mils. Similarly, Package transmission line w=7 mils, s=4 mils, Plated through hole (PTH) L=0.3 nH,C=2pf, Solder ball C=12 pf, CPU socket L=0.5 nH, C=3pf, Break out w=6 & S=3 mils, Mother Board w=10, s=11 mils, Break Out w =6 mils,s=3 mils,CPU socket L=0.5 nH,C=3 pf,PTH L=3 nH, Mother Board transmission line w=7, s=4 mils,Break out w=6,s =3 mils and Receiver r =50 ohm,C=3 pf . We choose the values such that the impedance should be in our required level (Table-3 shows the impedance differences.)

Table 3: Impedance differences in the Printed Circuit Board (PCB.)

Break Out	Package Transmission Line	Break Out	Mother Board	Break Out	Package Transmission Line	Break Out
Trace width, w=5 Mils	Trace width, w=7 mils	Trace width, w=6 mils	Trace width, w= 10 mils	Trace width, w= 6 mils	Trace width, w= 7 mils	Trace width, w= 6 mils
Space, s= 2 mils	Space, s= 4 mils	Space, s= 3 mils	Space, s= 11 mils	Space, s= 3 mils	Space, s= 4 mils	Space, s= 3 mils
Impedance 70 ohm	Impedance 60 ohm	Impedanc 65 ohm	Impedance 50 ohm	Impedance 65 ohm	Impedance 60 ohm	Impedance 65 ohm

In our system designing we consider single line and differential line in the Printed Circuit Board (PCB).When these lines routes through the PCB we have to maintain impedance constraint (Table below shows the impedance differences.)For better routing single lines impedance should be 50 ohm and difflines impedance should be 90 ohm (All the calculations done by the Microstrip, Stripline impedance calculator.)According to the graph we see that when the trace spacing, S decreases single lines impedance increases again in case of differential line opposite things happened if we decrease the trace space differential line impedance decrease.

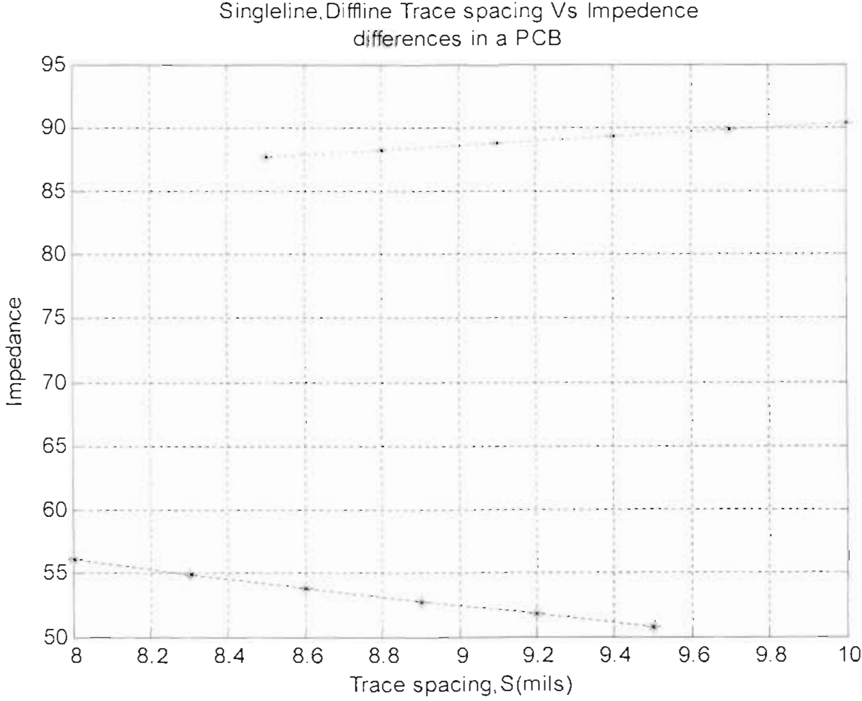


Figure 15: **Impedance differences in a PCB (Single line, Differential line.)**

Table 4: Impedance differences in a Printed Circuit Board.

Single line	Trace spacing 9.5 Mils	Trace spacing 9.2 mils	Trace spacing 8.9 mils	Trace spacing 8.6 mils	Trace spacing 8.3 mils	Trace spacing 8.0 Mils
	Impedance 50.80 Ohm	Impedance 51.79 ohm	Impedance 52.81 ohm	Impedance 53.86 ohm	Impedance 54.94 ohm	Impedance 56.05 Ohm
Differential line	Trace spacing 10 mils	Trace spacing 9.7 mils	Trace spacing 9.4 mils	Trace spacing 9.1 mils	Trace spacing 8.8 mils	Trace spacing 8.5 mils
	Impedance 90.31 ohm	Impedance 89.83 ohm	Impedance 89.33 ohm	Impedance 88.81 ohm	Impedance 88.26 ohm	Impedance 87.68 ohm

As I focus on the pinfield (shadow) region thus I consider surface mount, Land Grid Array LGA775 socket. Assume this socket has a two dimensional array. The socket also provides I/O, power, and ground contacts. The socket contains 775 contacts arrayed about a cavity in the center of the socket with eutectic solder balls for surface mounting with the motherboard. Though, many sockets uses lead-free solder balls while the LGA775 socket contains eutectic solder balls. For our simplicity we assume the socket contacts as 1mm X 1mm pitch or 40 mils X 40 mils (X by Y) pitch in a 30 X 30 grid array.(Figure below). A matching Land Grid Array package will be mated with the socket.

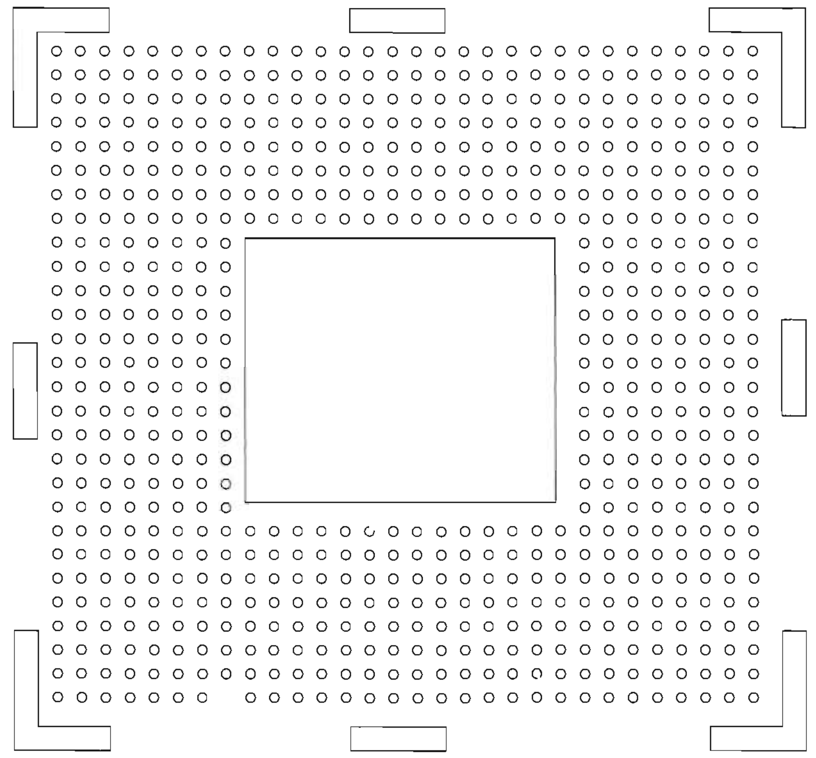


Figure 16:LGA775 Socket.

After efficient routing when the signal enters into the shadow reign it follows a pattern or geometry. According to this figure we consider two traces, where the trace width is defined W1, W2.Trace spacing S and keep out reign shows in the figure, all the units are considered as mils (Followed by the Printed Circuit Board design rules.).According to the PCB design rules we consider pitch as 1mm (Ball pitch) (approx 40 mil.) considered w1=w2=4 mils; s=4 mils and the keep out is 14 mils (All the calculations are done by the Microstrip, Stripline impedance Calculator.)As the signal routed and enters into the pinfield (shadow reign) trace space s decreases to maintain the keep out reign, so that the pin does not short circuited.

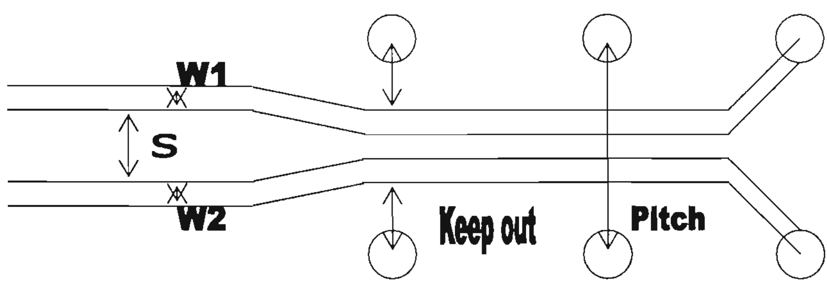


Figure 17: Printed circuit board Pinfield geometry.

When the signal enters into the shadow reign then the trace routes through this shadow reign maintaining the geometry. For efficient routing we can see in the table the impedance increases as 90 ohm to 112.71 ohm. In an electronic industry the cost of the PCB is higher when the trace width and spaces are smaller. According to the table we can see for 4 mil trace spacing we get 112.71 ohm. similarly as the line spacing decreases the impedance also decreases linearly.(Table-1).Putting these values into the graph we get a straight line, where trace spacing,S in X -axis and Impedance differences.Zdiff in the Y-axis.

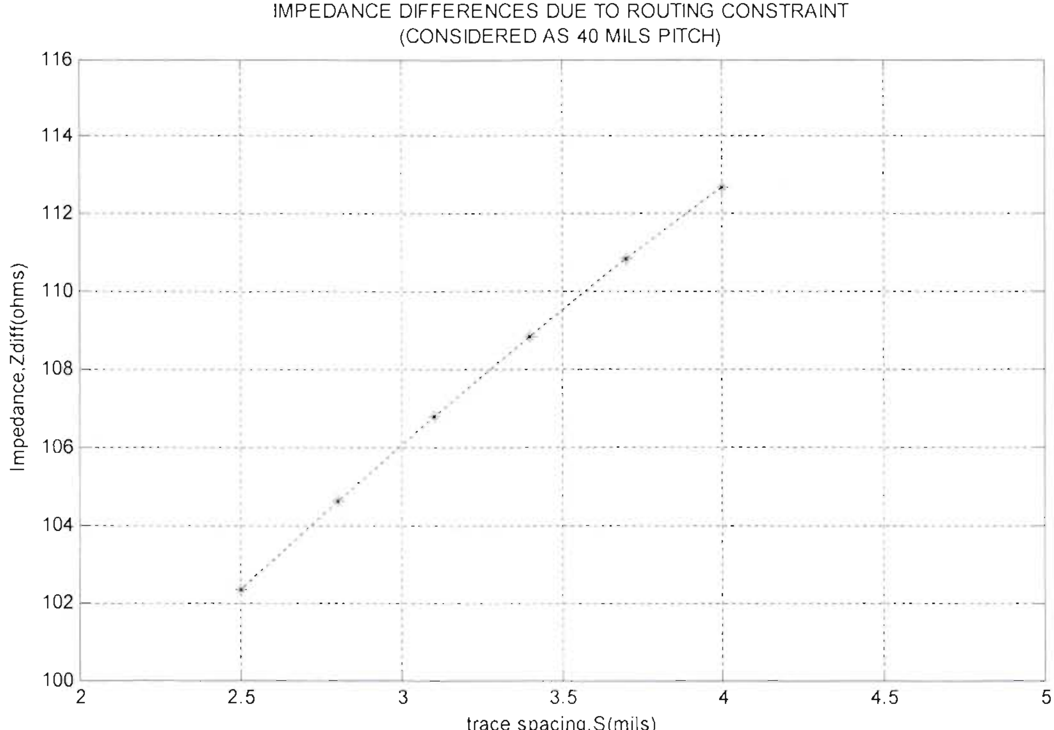


Figure 18: **Impedance differences showing when signal routes through the pin field.**

Table 5: Impedance differences showing when signal routes through the pin field.

Impedance, Zdiff 112.71 Ohm	Impedance, Zdiff 110.83 ohm	Impedance, Zdiff 108.86 ohm	Impedance, Zdiff 106.79 Ohm	Impedance, Zdiff 104.62 ohm	Impedance, Zdiff 102.35 ohm
Trace spacing, S=4 Mil	Trace spacing, S=3.7 mil	Trace spacing, S=3.4 mil	Trace spacing, S=3.1 Mil	Trace spacing, S=2.8 mil	Trace spacing, S=2.5 mil

As per Signal Integrity concerned the maximum accuracy i.e. the signal passes through driver to receiver end how accurately the message captured into the receiving end. The table below compares the signal accuracy both the receiving end and the braeak out reign. For 1 GHz experimental frequency, the edge rate I consider .01 nsec for which eye diagram shows 1.27 V (Eye height) and 8.88e-010 sec (Eye width.)Receiving end and break out reign0.81V (Eye height) and 8.29e-010 sec (Eye width).Similarly, 1.33 GHz we see both the receiving end and the break out reign the signal degrades i.e. Eye height and Eye width shrinks. As high frequency for example 5 GHz the Eye totally collapse (Eye height=0 V) i.e. the receiver can't detect the signal quite accurately.

Table 6: Eye opening consideration at different frequency.

Frequency	Edge rate (Rise & Fall)	Eye opening (HXW)
1 GHz	Receiving end 0.01 nsec	1.27 V X 8.88e-010sec
	Shadow reign 0.01 nsec	0.81V X 8.29e-010sec
1.33 GHz	Receiving end 0.075 nsec	1.01 V X 6.83e-010 sec
	Shadow reign 0.075 nsec	0.57 V X 6.98e-010 sec
2GHz	Receiving end 0.05 nsec	0.849V X 4.06e-010 sec
	Shadow reign 0.05 nsec	0.694 V X 4.56e-010 sec
2.5GHz	Receiving end 0.04 nsec	0.663V X 2.68e-010 sec
	Shadow reign .04 nsec	0.293 X 2.18e-010 sec
3GHz	Receiving end .03 nsec	0.041V X 1.66e-010 sec
	Shadow reign .03 nsec	0.493 X 2.97e-010 sec
5 GHz	Receiving end .02 nsec	0 V X 7.2e-011 sec.
	Shadow reign .02 nsec	0 V X 3.53e-011 sec

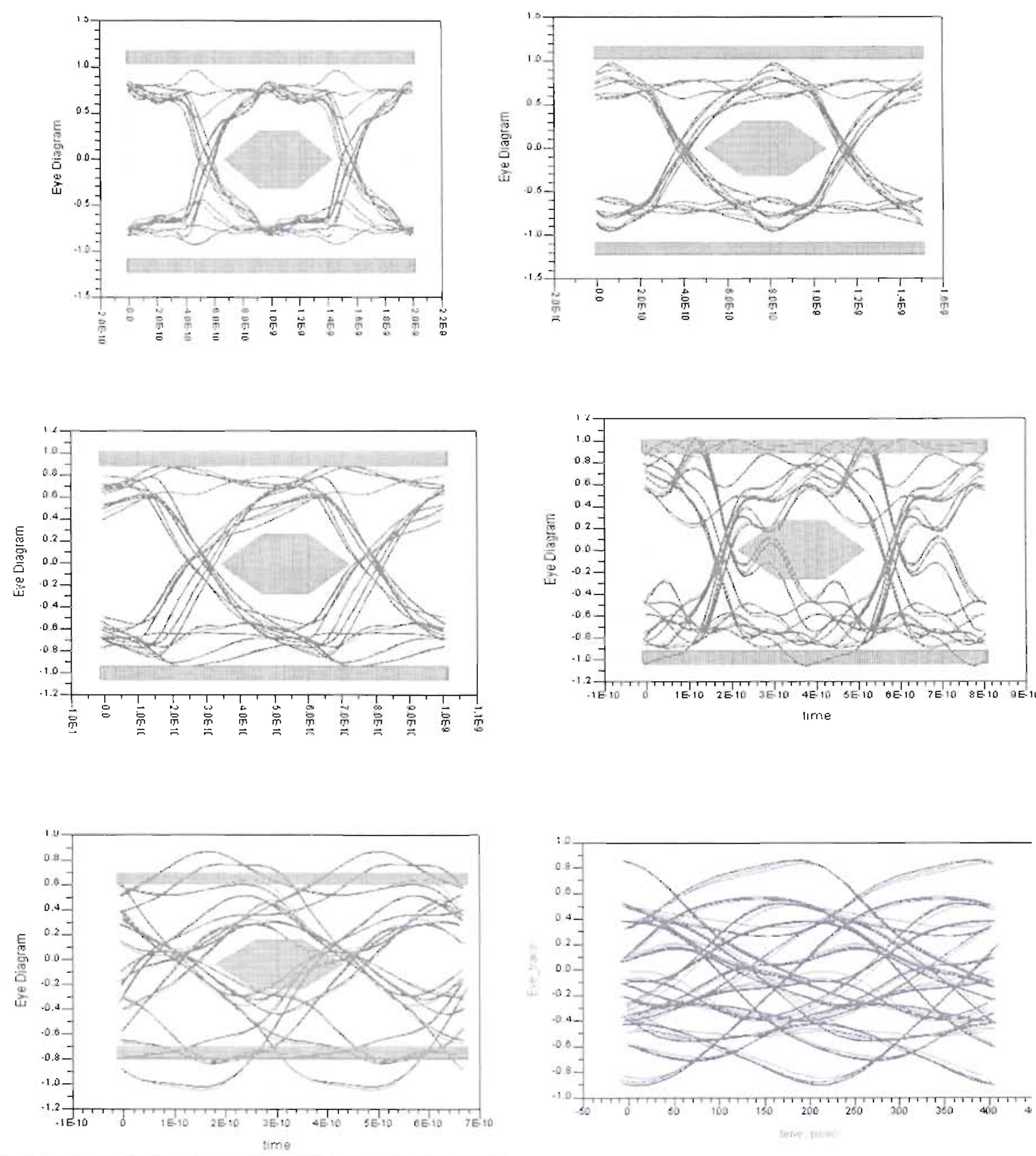


Figure 19: Comparison of Eye diagrams at different frequencies.

The figure shows comparison between Eye diagrams in different frequencies. According to our visual observation it can be seen that at higher frequencies it becomes worst i.e. collapse.

6. Discussions and Future Works

In this paper, I analyzed the differential lines mismatch which is simulated by H-Spice simulator. In my simulated program I studied how a signal passes from Driver to Receiver end through break out, package transmission line, Plated Through Hole (PTH), Solder ball, CPU socket, Mother board, Break through, Mother board transmission line, CPU socket, Plated Through Hole(PTH), Transmission line to Receiver end. I also observe CPU pin field where a signal passes from Driver (Silicon Die) to Receiver end and how the signals are interconnect I show the diagram on top. As for Interconnection I consider 2 mm HM ZD interconnection system as this is the best solution for high speed interconnection system. When the signal routes through the Printed Circuit Board (PCB) I analyzed the impedance mismatch through the single line and differential line (Transmission line), table and graph shows the scientific analysis. Finally, I focus on the pinfield (Shadow reign) where I analyzed how a signal routes through the pinfield region maintaining geometry (Pinfield geometry) and the impedance differences and analyzed the Eye both the receiving end and the shadow reign. Also I analyzed my system a 5 GHz hypothetical socket and observed the wave shape and Eye diagram.

As the world is moving faster and faster day by day. In future I shall upgrade my system 5 to 10 GHz range. In future I shall have to construct the single lines, differential lines in such a way that the trace width and trace spacing between the differential lines will be more accurate for routing and eye opening.

The original design needs to be modified accordingly so that in case if any Electronic Design Automation (EDA) companies choose the systems adopt the tester for quality control purposes.

6. References.

[1] " HSPICE User's manual" Ver. True-Hspice Device Models, Version 2001.4 Avant! Software Inc.

[2]A Subgridding Method for the Time-Domain Finite-Difference Method to Solve Maxwell's Equations.Svetlana S. Zivanovic, Kane S. Yee, Member, IEEE, and Kenneth K. Mei, Fellow, IEEE.

[3] E. Bogatin "Signal Integrity –Simplified" Prentice Hall Publications.

[4] Howard Johnson, Martin Graham "High Speed Signal Propagation. Advanced Black Magic" Prentice Hall Publications.

[5]. Douglas Brooks "Signal Integrity Issues and Printed Circuit Board Design" Prentice Hall Modern Semiconductor Design Series.

[6] Clayton R. Paul "Introduction to Electromagnetic Compatibility" Second Edition. John Wiley and Sons, Inc.Publication.

[7] David. M. poser "Microwave Engineering" TATA McGraw Hill Inc.

[8] Application Note, AP-579 "Pentium Processor Flexible Motherboard, Design Guidelines" Intel Corporation.

[9] Hayt Jr. " Electromagnetic Engineering" TATA McGraw Hill Inc.

[10] David. K. Cheng "Field and Wave Electromagnetics" Pearson Education. 2nd Edition.

[11]Neil H.E.Weste. David Harris. Ayan Banerjee "CMOS VLSI DESIGN" Pearson Education. 3rd edition.

[12] Douglas V. Hall "Microprocessors and Interfacing" Second Edition TATA McGraw Hill publications.pp 547-549.

[13] Amos Gilat "MATLAB (An introduction with Application)" Wiley Publications.

[14] Strategic Alliance to Deliver"2 MM HM ZD Connector Introduction" Tyco Electronics, Corp.

[15] Interconnect Application Note"Z-PACK HM-ZD, PWB Footprint Optimization for Routing" Report #20GC015-1. Rev.B. july10, 2003, Tyco Elctronics, Corp.

[16] NESA Technical White Paper "Signal Integrity and Validation of National's Bus LVDS (BLVDS) Technology in Heavily Loaded Backplanes" Interface Products Group, National Semiconductor Corporation.

[17] Design Con 2007 "Pre-Emphasis and Equalization Parameter Optimization with Fast, Worst-Case/Multibillion-Bit Verification" Altera Corporation, Mentor Graphics.

[18] Design Con 2007 "Digitally Assisted Adaptive Equalizer in 90 nm With Wide Range Support From 2.5 Gbps to 6.5 Gbps" Altera Corporation.

[19] " Z-Pack Hard Metric (HM)-Zd, 2-, 3- and 4-pair Connector Systems" Application Specification 114-13059. Tyco Electronics.

[20] "Virtex-4RocketIO Multi-Gigabit Transceiver, User Guide" UG076 (v4.0) August17, 2007, XILINX Corporation.

[21] "Device Package User Guide"UG112 (v3.0) May18, 2007, XILINX Corporation.

[22] "Ball/Land Grid Array Sockets, Twist Lock Types" E-Tec, Interconnect.

[23] "Thermal Design Guide for Socket F (1207) Processors" Publication# 32800 Rev: 3.00, Issue Date: August 2006.Advanced Micro Devices (AMD)

[24] "BGA Socket Adapter System, 0.50 and 0.65 mm Pitch" Advanced Interconnections.

[25] "1 mm-pitch Low Profile Connector System for Wire to PCB Applications suitable for use with Discrete Wire, FPC or Fine Coaxial Cable" HIROSE ELECTRIC CO.Tokyo.Japan.

[26] "Power Connectors and Interconnection System, Multi-Beam XL Power Distribution Connector System" Tyco Electronics.

[27] "LGA775 Socket. Mechanical Design Guide" Document Number: 302666-003, February, 2006. Intel Corporation.

[28] "Socket Mounting Recommendations and Reflow Profile" Emulation Technology, Inc.

[29] "Socket-adapter systems: A practical Test Alternative" August/September 2006 edition Advanced Packaging Corporation.

[30]"FASTON Terminals Insulated and Uninsulated" Tyco, Electronics.

[31] "ML300 User Guide. Virtex-II Pro Development System.UG038 (v1.3.2) January 3, 2008" XILINX Corporation.

7. Appendix A - Keywords

Some of the critical components and devices used in this analysis is described below.

[1] Packaging- Assembly of integrated circuits is known as Packaging. Actually, the chip package provides a mechanical and electrical connection between the chip and the circuit board.

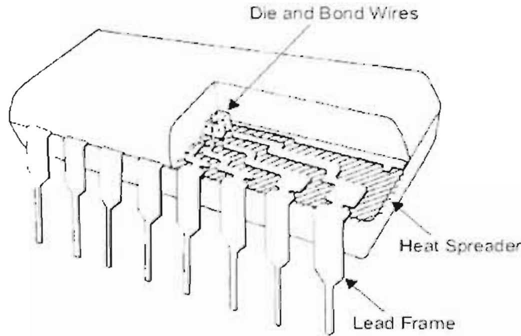
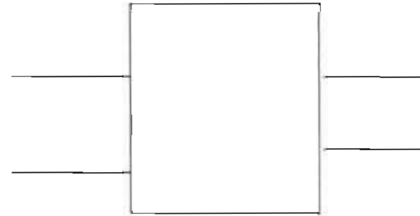


Figure 20: **Dual-in-line package (Cutaway view.)**

[2] Transmission Line- In printed Circuit Board (PCB) there are many microstrip single lines and differential lines ,which are known as Transmission line.



N=2 Transmission Line.

Figure 21: **Transmission line.**

[3] Routing- Routing is the method of interconnection of different circuit components with an aim to minimize the chip area and also reduction of total wire length.

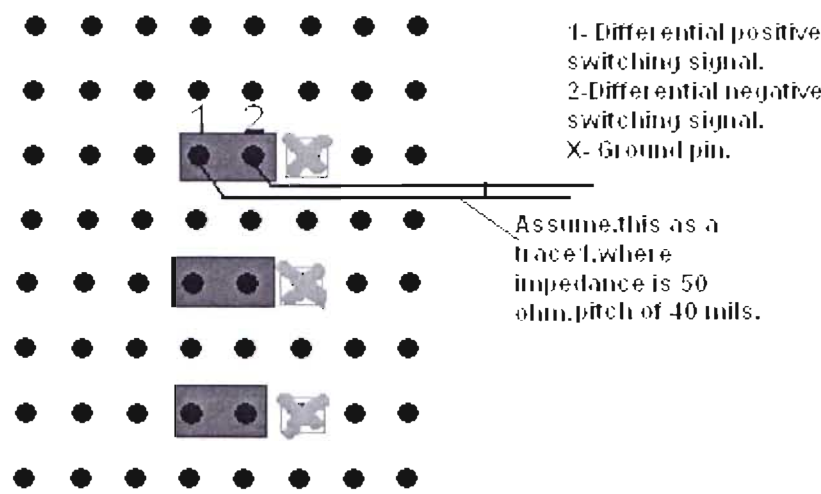


Figure 22: **Routing of 8X8 pins socket.**

[4] Noise- In SI there are lot of noise likewise ringing, ground bounce, reflections, crosstalk Switching noise. Etc.

[5] Rise time- The time is taken for a signal to rise from 10% to 90%.

[6] Fall time- The time is taken for a signal to 90% to 10%.

[7] Eye diagram- The vertical thickness of the line bunches in an eye diagram indicate the magnitude of AC voltage noise, whereas the horizontal thickness of the bunches where they cross over is an indication of the AC timing noise or Jitter. Fixed DC voltage and timing offsets are indicated by the position of the eye on the screen.

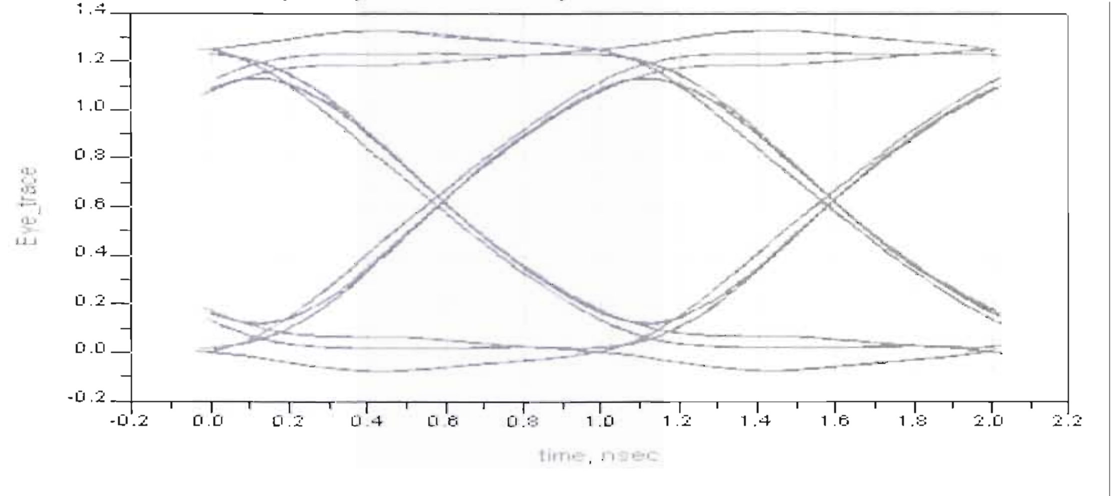


Figure 23: **Eye diagram.**

[8] Overshoot- where a signal rises to a level greater than its steady-state voltage before settling to its steady state voltage.

[9] Peak to peak- measurement of total amplitude.

[10] Crosstalk- Undesirable signal coupling from noisy aggressor nets to victim nets. This phenomena can be eliminated by spacing between the nets.

[11] PTH (Plated Through Hole): In PCB design it refers to a pad with a plated hole that connects copper tracks from one layer of the board to other layer. In the figure below the vertical column is known as Via. In IC circuit via is a small opening in an insulating layer to form a connection.

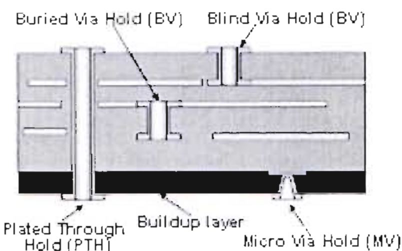


Figure 24: **Plated Through Hole.**

[12] Socket: Socket is a connector on a computers motherboard that accepts a CPU and forms an electrical interface with it. Most CPU sockets are based on the Pin Grid Array (PGA) architecture in which short pins on the underside of the processor package mate with holes in the socket.

[13] Transient analysis- Transient analysis computes the circuit solution, as a function of time, over a time range specified in the .TRAN statement.

[14] Pitch- Center to center distance of an IC (Integrated Circuit) pin.

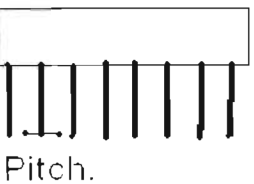
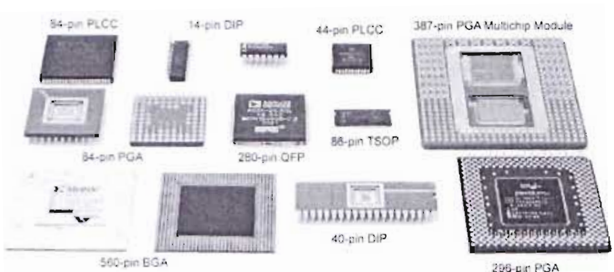


Figure 25: **Pitch.**

[15] BGA(Ball Grid Array) – Array of SMT(Surface Mount Technology) solder balls underside of package on 15.7 – 50 mil centres.Extremely high densities of I/Os with low

parasitics.In that particular case, requires specialized assembly and inspection equipment to blindly attach to array of pads on PCB.

[16] PGA (Pin Grid Array) – Array of through hole-pins on 100 mil centres.Low cost long wires between chip and corner pins.



8. Appendix B – Hspice Code

```
A Test Circuit
**************SI_Research****************

*   Md.Nahidul Ghani
*   Electronic and Electrical Engineering
*   East West University
*   Dhaka, Bangladesh
*****************************************
**
**  Project: Study of differential lines mismatch
**
**  Date: July 2007
**
*****************************************


*Linear Driver

*-- Voltage parameters
.param vdd    = 1.05          $ in volts


*-- Driver Parmaters
.param cpu_ccomp      = 1.5p  $ driver ccomp in pF
.param rise_time      = 375p    $750p        $in ps

*-- Driver parameters
.param data_rate = 1067                               $ in MT/s
.param clock_speed = 'data_rate/2'
.param freq    = '(clock_speed/2)*
.param period_ctl = '1/freq'
.param period = '1/freq'
.param pw      = 'period/2'
.param pw_ctl         = 'period/2'
.param half_pw        = 'pw_ctl/2'
.param delay_start_ctl        = 0n
.param delay_start_data      ='delay_start_ctl+period_ctl+period_ctl-half_pw'  $this is if
simulating a clock to delay for settling time.
.param data_delay     = 'delay_start_data'
.param write_strobe_delay = 'delay_start_ctl'
.param delay_start_strobe = 'delay_start_ctl+period_ctl+period_ctl'
.param idrvm  = 1.0
.param dtr    = rise_time
.param dtf    = rise_time+40p
.param dpwr   = '(period/2)-dtr'
.param dpwf   = '(period/2)-dtf'
.param ron_pmos = 50          $ driver impedance settings pmos
.param ron_nmos = 25          $ driver impedance settings nmos
.param sim_time = 'delay_start_ctl+(32*pw_ctl)'

.param rc = 50


.param m_in =               0.0254          $ meter/inch

* CPU parameter

.param cpu1_tl_mr = '0.469*m_in'     $ in.


* MB
.param mb_tl1 =             '(0.5*m_in)'   $ in.
.param mb_tl2 =             '(3*m_in)'     $ in. $CPU2 TRL length
```

```
.param mb_tl3 =             '(12*m_in)'   $ in. $CPU2 TRL length
.param mb_tl4 =             '(15*m_in)'
.param mb_tl5 =             '(17*m_in)'
.param mb_tl6 =             '(19*m_in)'
.param mb_tl7 =             '(20*m_in)'
.param cpu1_pf_len =        '0.8*m_in'      $ in.
.param cpu2_pf_len =        '0.8*m_in'      $ in.

.param top_board2buf_len =  '0.5*m_in'      $ in.


*-- HSPICE simulator parameters
.option probe post=1 measdgt=6
.width co = 132
.tran  20e-12 sim_time

*----------------------------------------------------------------------------
*       Include Files
*----------------------------------------------------------------------------
.include '..\Nahidinclude\linear_driver.inc'
.include '..\Nahidinclude\bit_patterns_ctl_aug05.inc'
.include '..\Nahidinclude\fpgaload.inc'
.include '..\Nahidinclude\probeload.inc'

****************** included files  *********************
* CPU Package
.inc '..\Nahidinclude\PKG\breakout_w_rect.sp'
.inc '..\Nahidinclude\PKG\ddd_667_MaxZ.sp'
.inc '..\Nahidinclude\PKG\ddd_667_MinZ.sp'
.inc '..\Nahidinclude\PKG\ddd_667_NomZ.sp'
.inc '..\Nahidinclude\PKG\pth_3io.sp'
.inc '..\Nahidinclude\PKG\socket.sp'

* Motherboard

.inc '..\Nahidinclude\MB1066\mb_maxz.rlc'
.inc '..\Nahidinclude\MB1066\mb_minz.rlc'
.inc '..\Nahidinclude\MB1066\mb_typz.rlc'

*----------------------------------------------------------------------------
*       Memory Controller Driver
* this is set up for a 2 line model
*----------------------------------------------------------------------------
*-- Voltage Rails
V_vsm vddq gnd vdd
V_vtt vtt gnd 1.2

*-- Bit Pattern Drivers
Xdrive_CSC2 ctl_data CTL_pulse_DRIVER           $ vic bit pattern
Xdrive_CSC1 sdata1 CTL_high_DRIVER       $ ag1 bit pattern
Xdrive_CSC3 sdata2 CTL_high_DRIVER       $ ag2 bit pattern

*-- VCVS with bessel filter input on PWL stimulus

Rfltd1   ctl_data ctl_in  3                      $ vic source
xfltd1   ctl_in ctl_out gnd  Bessel2 f3db=3G  $ vic 3dB filter

Rflts1   sdata1  iws1  3                         $ ag1 source
xflts1   iws1 cws1 gnd  Bessel2 f3db=3G        $ ag1 3B filter

Rflts2   sdata2  iws2  3                         $ ag2 source
xflts2   iws2 cws2 gnd  Bessel2 f3db=3G        $ ag2 3dB filter

*-- Driver call

xdrvc1   vddq gnd cpu1_pad_vic ctl_out  VCR_driver    $ vic behavioral driver
Cmch_1   cpu1_pad_vic gnd cpu_ccomp

xdrvds1   vddq gnd cpu1_pad_ag1 cws1  VCR_driver      $ agg1 behavioral driver
Ccpu_s1   cpu1_pad_ag1 gnd cpu_ccomp
```

```
xdrvds2  vddq gnd cpu1_pad_ag2 cws2  VCR_driver      $ agg2 behavioral driver
Ccpu_s2  cpu1_pad_ag2 gnd cpu_ccomp


* CPU1
x_cpu1_breakout_mr  cpu1_pad_ag1      cpu1_pad_vic   0
 +               cpu1_bo_agr1_mr   cpu1_bo_sig_mr   0
 +               gnd breakout_w_rect

* CPU Package Transmission Line
w_cpu1_tl_mr N=2
 + cpu1_bo_agr1_mr cpu1_bo_sig_mr  gnd
 + cpu1_tl_agr1_mr cpu1_tl_sig_mr  gnd
 + rlgcmodel=ddd_667_minz
 + l=cpu1_tl_mr

*****************************************************

* CPU Plated Through Hole (PTH)
x_cpu1_pth  cpu1_tl_agr1_mr cpu1_tl_sig_mr   0
 +          cpu1_pth_agr1 cpu1_pth_sig 0 gnd pth_3io

* CPU Socket
x_cpu1_socket   cpu1_pth_agr1  cpu1_pth_sig  0
 +               cpu1_soc_agr1  cpu1_soc_sig  0  zif_socket_couple  $gnd zif_socket_couple


   *************probe attach ***********
   ************************************************************

*X_probe cpu1_soc_agr1  cpu1_soc_sig  0
* + cpu1_socprb_agr1  cpu1_socprb_sig  0 gnd probeload interposerprobeloadpcudebug

*****************************************************
* MB TraceX: CPU1 Pin Field
w_mb1_pf n=2
 + cpu1_soc_agr1  cpu1_soc_sig   gnd
 + cpu1_pf_agr1  cpu1_pf_sig   gnd
 + l = cpu1_pf_len
 + rlgcmodel=mb_minz
 + fgd = 0 includersimag=yes

*********************************************
* MB Trace1:
w_mb1 n=2
 + cpu1_pf_agr1 cpu1_pf_sig  gnd
 + mbd_tl1_agr1 mbd_tl1_sig  gnd
 + l = mb_tl1
 + rlgcmodel=mb_minz       *Assumption is routed in top layer
 + fgd=0 includersimag=yes

*********************************************
* MB Trace2:
w_mb2 n=2
 + mbd_tl1_agr1 mbd_tl1_sig  gnd
 + mbd_tl2_agr1 mbd_tl2_sig  gnd
 + l = mb_tl2
 + rlgcmodel=mb_minz * Assumption is routed in top layer
 + fgd=0 includersimag=yes

*********************************************
* MB Trace3:
w_mb3 n=2
 + mbd_tl2_agr1 mbd_tl2_sig  gnd
 + mbd_tl3_agr1 mbd_tl3_sig   gnd
 + l = mb_tl3
 + rlgcmodel=mb_minz * Assumption is routed in top layer
 + fgd=0 includersimag=yes
*********************************************
* MB Trace4:
w_mb4 n=2
```

```
 + mbd_tl3_agrl mbd_tl3_sig  gnd
 + mbd_tl4_agrl mbd_tl4_sig   gnd
 + l = mb_tl4
 + rlgcmodel=mb_minz       *Assumption is routed in top layer
 + fgd=0 includersimag=yes
*******************************************
* MB Trace5:
w_mb5 n=2
 + mbd_tl4_agrl mbd_tl4_sig  gnd
 + mbd_tl5_agrl mbd_tl5_sig   gnd
 + l = mb_tl5
 + rlgcmodel=mb_minz       * Assumption is routed in top layer
 + fgd=0 includersimag=yes
*******************************************
* MB Trace6:
w_mb6 n=2
 + mbd_tl5_agrl mbd_tl5_sig  gnd
 + mbd_tl6_agrl mbd_tl6_sig   gnd
 + l = mb_tl6
 + rlgcmodel=mb_minz       * Assumption is routed in top layer
 + fgd=0 includersimag=yes
*******************************************
* MB Trace7:
w_mb7 n=2
 + mbd_tl6_agrl mbd_tl6_sig  gnd
 + mbd_tl7_agrl mbd_tl7_sig   gnd
 + l = mb_tl7
 + rlgcmodel=mb_minz * Assumption is routed in top layer
 + fgd=0 includersimag=yes

****************************************************
* MB TraceY: CPU2 Pin Field
w_mb2_pf n=2
 + mbd_tl7_agrl mbd_tl7_sig  gnd
 + cpu2_pf_agrl  cpu2_pf_sig    gnd
 + l = cpu2_pf_len
 + rlgcmodel=mb_minz
 + fgd = 0 includersimag=yes

*****************************************************
****************************************************
* CPU2 Socket
x_cpu2_socket
 + cpu2_pf_agrl  cpu2_pf_sig    gnd
 + cpu2_soc_agrl  cpu2_soc_sig  gnd zif_socket_couple

****************************************************
* CPU2 Plated Through Hole (PTH)
x_cpu2_pth
 + cpu2_soc_agrl cpu2_soc_sig 0
 + cpu2_pth_agrl cpu2_pth_sig 0 gnd pth_3io

****************************************************
* CPU2 Package Transmission Line
w_cpu2_tl_mr N=2
 + cpu2_pth_agrl cpu2_pth_sig gnd
 + cpu2_pad_agrl cpu2_pad_sig gnd
 + rlgcmodel=ddd_667_minz    $ In dir file is defined.
 + l=cpu1_tl_mr

*************************************************
* CPU2
x_cpu2_breakout_mr
 + cpu2_pad_agrl cpu2_pad_sig gnd
 + cpu2_bo_agrl  cpu2_bo_sig  gnd
 + gnd breakout_w_rect

*********  cpu  load  *****************************
c_cpu2_load1 cpu2_bo_agrl gnd cpu_ccomp
c_cpu2_load2 cpu2_bo_sig gnd cpu_ccomp
```

```
*----------------------------------------------------------------------------
*       .Probe Statements
*------------------------------------------------------------------------
.probe tran v(cpu1_bo_sig_mr)
.probe tran v(mbd_tl1_sig)      $Probe point.
.probe tran v(cpu2_pth_sig)
.probe tran v(cpu2_pad_sig)
.probe tran v(cpu1_tl_sig_mr)

.end


.MODEL MB_1 W MODELTYPE=RLGC, N=3

$L0=DC inductance matrix; C0=DC capacitance Matrix.

$R0=DC resistance matrix; G0=DC shunt Conductance.

$Rs=Skin effect resistance; Gd= Dielectric Loss conductance.

+ Lo = 3.448598e-007
+       6.531542e-008 3.423302e-007
+       2.119154e-008 6.531542e-008 3.448598e-007
+ Co = 1.071690e-010
+       -1.786122e-011 1.110616e-010
+       -9.561500e-013 -1.786122e-011 1.071690e-010
+ Ro = 5.190929e+000
+       0.000000e+000 5.190928e+000
+       0.000000e+000 0.000000e+000 5.190929e+000
+ Go = 0.000000e+000
+       0.000000e+000 0.000000e+000
+       0.000000e+000 0.000000e+000 0.000000e+000
+ Rs = 1.570409e-003
+       3.474044e-004 1.585259e-003
+       1.576151e-004 3.473658e-004 1.569653e-003
+ Gd = 1.122271e-011
+       -1.870422e-012 1.163034e-011
+       -1.001278e-013 -1.870422e-012 1.122271e-011


.MODEL mb_maxz W MODELTYPE=RLGC, N=2
+ Lo = 3.448598e-007
+       6.531542e-008 3.423302e-007
+ Co = 1.071690e-010
+       -1.786122e-011 1.110616e-010
+ Ro = 5.190929e+000
+       0.000000e+000 5.190928e+000
+ Go = 0.000000e+000
+       0.000000e+000 0.000000e+000
+ Rs = 1.570409e-003
+       3.474044e-004 1.585259e-003
+ Gd = 1.122271e-011
+       -1.870422e-012 1.163034e-011


.MODEL mb_minz W MODELTYPE=RLGC, N=2
+ Lo = 2.569762e-007
+       3.510568e-008 2.550276e-007
+ Co = 1.443481e-010
+       -1.577618e-011 1.471304e-010
+ Ro = 3.437408e+000
+       0.000000e+000 3.437408e+000
+ Go = 0.000000e+000
+       0.000000e+000 0.000000e+000
+ Rs = 1.564327e-003
+       3.093692e-004 1.555904e-003
+ Gd = 1.511610e-011
+       -1.652078e-012 1.540746e-011


.MODEL mb_typz W MODELTYPE=RLGC, N=2
```

```
+ Lo = 3.001149e-007
+       4.887577e-008 2.977921e-007
+ Co = 1.229949e-010
+       -1.692670e-011 1.263573e-010
+ Ro = 4.152733e+000
+       0.000000e+000 4.152733e+000
+ Go = 0.000000e+000
+       0.000000e+000 0.000000e+000
+ Rs = 1.558346e-003
+       3.288710e-004 1.560845e-003
+ Gd = 1.288000e-011
+       -1.772560e-012 1.323211e-011


* BEGIN ANSOFT HEADER (Break out)
  * node 1 XXD#_14#_0_vccsrc3
  * node 2 XXD#_15#_0_vccsrc2
  * node 3 XXD#_16#_0_vccsrc1
  * node 4 XXD#_14#_0_Sink
  * node 5 XXD#_15#_0_Sink
  * node 6 XXD#_16#_0_Sink
  * node 7 Ground_Bias
  *   Format: HSPICE
  *    Model: 3D Lumped Model
  *     Type: RLC
  * END ANSOFT HEADER
  .SUBCKT breakout_w_rect 1 2 3 4 5 6 7
  C001 8 7 1.38497E-013
  C002 9 7 1.68392E-013
  C003 10 7 1.27596E-013
  C001_002 8 9 7.09658E-015
  C001_003 8 10 7.50137E-016
  C002_003 9 10 7.38084E-015
  V001 1 11 DC 0
  V002 2 12 DC 0
  V003 3 13 DC 0
  L001 11 14 2.74134E-010
  L002 12 15 3.55278E-010
  K001_002 L001 L002 0.119357
  L003 13 16 2.61042E-010
  K001_003 L001 L003 0.0752826
  K002_003 L002 L003 0.0874047
  R001 14 8 0.0430051
  F001R002 8 14 V002 0.0240054
  F001R003 8 14 V003 0.0240054
  R002 15 9 0.0543152
  F002R001 9 15 V001 0.0190067
  F002R003 9 15 V003 0.0190067
  R003 16 10 0.0399283
  F003R001 10 16 V001 0.0258551
  F003R002 10 16 V002 0.0258551
  V004 8 17 DC 0
  V005 9 18 DC 0
  V006 10 19 DC 0
  L004 17 20 2.74134E-010
  L005 18 21 3.55278E-010
  K004_005 L004 L005 0.119357
  L006 19 22 2.61042E-010
  K004_006 L004 L006 0.0752826
  K005_006 L005 L006 0.0874047
  R004 20 4 0.0430051
  F004R005 4 20 V005 0.0240054
  F004R006 4 20 V006 0.0240054
  R005 21 5 0.0543152
  F005R004 5 21 V004 0.0190067
  F005R006 5 21 V006 0.0190067
  R006 22 6 0.0399283
  F006R004 6 22 V004 0.0258551
  F006R005 6 22 V005 0.0258551
  .ENDS breakout_w_rect
```

```
* BEGIN ANSOFT HEADER
* node 1 Trace1_A
* node 2 Trace2_A
* node 3 Trace3_A
* node 4 Ground_A
* node 5 Trace1_B
* node 6 Trace2_B
* node 7 Trace3_B
* node 8 Ground_B
*   Format: HSPICE W Element
*   Length: 1 meters
*   T_Rise: 1E-009 seconds
*    Model: Distributed Lossy Transmission Line

.model ddd_667_maxz W modeltype=RLGC N=3
+ Lo=
+   3.781982630758784e-007
+   3.036302332357759e-008
+    3.77785469050805e-007
+   8.694378401122924e-009
+   3.035836579264989e-008
+   3.787443474762008e-007
+ Co=
+   1.004675391870003e-010
+  -7.013101153174054e-012
+    1.01080233132815e-010
+  -5.914315758260171e-013
+  -7.019190671098722e-012
+   1.004855989646466e-010
+ Ro=
+        53.77868289323165
+        1.121076233183845
+        53.77868289323194
+        1.121076233183866
+        1.121076233183954
+        53.77868289322854
+ Rs=
+     0.005066823360478899
+    0.0004708697369349221
+     0.00513329882111646l
+    0.0001616560859422387
+    0.0004681214561559896
+     0.004954379830848193

* end of file


* BEGIN ANSOFT HEADER
* node 1 Trace1_A
* node 2 Trace2_A
* node 3 Trace3_A
* node 4 Ground_A
* node 5 Trace1_B
* node 6 Trace2_B
* node 7 Trace3_B
* node 8 Ground_B
*   Format: HSPICE W Element
*   Length: 1 meters
*   T_Rise: 1E-009 seconds
*    Model: Distributed Lossy Transmission Line
*      Cap:

*.SUBCKT us_ddd_667_minz 1 2 3 4 5 6 7 8
.model ddd_667_minz W modeltype=RLGC N=2
+ Lo=
+   2.953370942477167e-007
+    1.73348309173483e-008
+   2.953160340247037e-007
+ Co=
+   1.373877485584915e-010
```

```
+   -6.563917688215942e-012
+    1.377933182491636e-010
+ Ro=
+         40.37964172903712
+         1.121076233183803
+         40.37964172903352
+ Rs=
+       0.005434852729436l3
+     0.0004350653121069269
+       0.005461368749950 92

*W1 1 2 3 4 5 6 7 8 N=3 L=1 RLGCMODEL=us_ddd_667_minz

*.ENDS us_ddd_667_minz

* end of file


* BEGIN ANSOFT HEADER
* node 1 Trace1_A
* node 2 Trace2_A
* node 3 Trace3_A
* node 4 Ground_A
* node 5 Trace1_B
* node 6 Trace2_B
* node 7 Trace3_B
* node 8 Ground_B
*    Format: HSPICE W Element
*    Length: 1 meters
*    T_Rise: 1E-009 seconds
*     Model: Distributed Lossy Transmission Line
*       Cap:

*.SUBCKT nomz 1 2 3 4 5 6 7 8
.model ddd_667_nomz W modeltype=RLGC N=2
+ Lo=
+    3.372812253704848e-007
+    2.417359793838517e-008
+    3.371354901402379e-007
+ Co=
+    1.160814534703761e-010
+   -7.210332592679944e-012
+    1.167085028021935e-010
+ Ro=
+         45.08485008352661
+         1.121076233183857
+         45.08485008353133
+ Rs=
+      0.005183639553197403
+     0.0004624578937901263
+      0.005259088913393801

*W1 1 2 3 4 5 6 7 8 N=3 L=1 RLGCMODEL=nomz

*.ENDS nomz

* end of file


* BEGIN ANSOFT HEADER
*node 1 XXD#_0#_vccsrc1
*node 2 XXD#_2#_vccsrc2
*node 3 XXD#_4#_vccsrc3
*node 4 XXD#_0#_Sink
*node 5 XXD#_2#_Sink
*node 6 XXD#_4#_Sink
*node 7 Ground_Bias
*    Format: HSPICE
*     Model: 3D Lumped Model
*      Type: RLC
*   Project: pth_3io
```

```
.SUBCKT pth_3io 1 2 3 4 5 6 7
C001 8 7 1.09233E-013
C002 9 7 5.11135E-014
C003 10 7 1.1155E-013
C001_002 8 9 5.53446E-014
C001_003 8 10 1.50742E-014
C002_003 9 10 4.75027E-014
V001 1 11 DC 0
V002 2 12 DC 0
V003 3 13 DC 0

L001 11 14 2.16864E-010
L002 12 15 2.62009E-010
K001_002 L001 L002 0.316666

L003 13 16 2.39229E-010
K001_003 L001 L003 0.232361
K002_003 L002 L003 0.287989
R001 14 8 0.00151094
F001R002 8 14 V002 0.326788
F001R003 8 14 V003 0.326788
R002 15 9 0.00197495
F002R001 9 15 V001 0.250011
F002R003 9 15 V003 0.250011
R003 16 10 0.00197504
F003R001 10 16 V001 0.249999
F003R002 10 16 V002 0.249999
V004 8 17 DC 0
V005 9 18 DC 0
V006 10 19 DC 0
L004 17 20 2.16864E-010
L005 18 21 2.62009E-010
K004_005 L004 L005 0.316666
L006 19 22 2.39229E-010
K004_006 L004 L006 0.232361
K005_006 L005 L006 0.287989
R004 20 4 0.00151094
F004R005 4 20 V005 0.326788
F004R006 4 20 V006 0.326788
R005 21 5 0.00197495
F005R004 5 21 V004 0.250011
F005R006 5 21 V006 0.250011
R006 22 6 0.00197504
F006R004 6 22 V004 0.249999
F006R005 6 22 V005 0.249999
.ENDS pth_3io


* Three pin CPU Socket Model
.subckt zif_socket_couple in1 in2 in3 out1 out2 out3
L11 in1 mid1 1.202n
R11 mid1 out1 20m
C11 out1 gnd 0.669p

L22 in2 mid2 1.478n
R22 mid2 out2 20m
C22 out2 gnd 0.8506p

L33 in3 mid3 1.202n
R33 mid3 out3 20m
C33 out3 gnd 1.055p

K12 L11 L22 0.2610
K23 L22 L33 0.2464

C12 out1 out2 0.1724p
C23 out2 out3 0.3461p
.ENDS zif_socket_couple
```

```
******************************************************************************************
********************** Driver.LIB ********************

.subckt ix
+ i ibd g ctl  Mx=100.0 rondr = 100

epad i g cur='Mx*v(ctl)'
rs  i ibd rondr

.ends ix

******************************************************************************************
.subckt VCR_driver   vcc gnd out v_cont

Gpullup  vcc out VCR PWL(1) v_cont gnd
+      0    ,   8000
+      0.1 ,   'ron_pmos      +786'
+      0.15,   'ron_pmos      +286'
+      0.2 ,   'ron_pmos      +186'
+      0.25,   'ron_pmos      +98'
+      0.3 ,   'ron_pmos      +88'
+      0.35,   'ron_pmos      +78'
+      0.4 ,   'ron_pmos      +68'
+      0.45,   'ron_pmos      +58'
+      0.5 ,   'ron_pmos      +48'
+      0.55,   'ron_pmos      +38'
+      0.6 ,   'ron_pmos      +32'
+      0.65,   'ron_pmos      +26'
+      0.7 ,   'ron_pmos      +20'
+      0.75,   'ron_pmos      +14'
+      0.8 ,   'ron_pmos      +8'
+      0.85,   'ron_pmos      +6'
+      0.9 ,   'ron_pmos      +4'
+      0.95,   'ron_pmos      +2'
+      1   ,   'ron_pmos      +0'

Gpull_dwn  out gnd VCR PWL(1) v_cont gnd
+      0    ,   '       ron_nmos      +      0      '
+      0.1 ,   '       ron_nmos      +      2      '
+      0.15,   '       ron_nmos      +      4      '
+      0.2 ,   '       ron_nmos      +      6      '
+      0.25,   '       ron_nmos      +      8      '
+      0.3 ,   '       ron_nmos      +      14     '
+      0.35,   '       ron_nmos      +      20     '
+      0.4 ,   '       ron_nmos      +      26     '
+      0.45,   '       ron_nmos      +      32     '
+      0.5 ,   '       ron_nmos      +      38     '
+      0.55,   '       ron_nmos      +      48     '
+      0.6 ,   '       ron_nmos      +      58     '
+      0.65,   '       ron_nmos      +      68     '
+      0.7 ,   '       ron_nmos      +      78     '
+      0.75,   '       ron_nmos      +      88     '
+      0.8 ,   '       ron_nmos      +      98     '
+      0.85,   '       ron_nmos      +      186    '
+      0.9 ,   '       ron_nmos      +      286    '
+      0.95,   '       ron_nmos      +      786    '
+      1   ,   8000

.ends VCR_driver


******************** Bessel.LIB ********************

.subckt Bessel2
+ i o g
+ f3db=1 zo=1

.param c0='1/(zo*6.28318*f3db)'
.param l0='zo/(6.28318*f3db)'
```

```
l1 i o '2.148*l0'
c2 o g '0.576*c0'
r1 o g10Meg

.ends Bessel2
```

Microstrip, Stripline impedance Calculator-