Semi-classical study of n-MOS inversion layer

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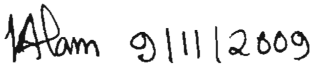

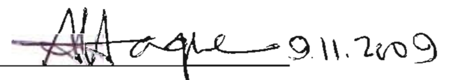

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Abstract

We study the energy band diagram, surface electric field, charge density and static current-voltage (C-V) characteristics of a metal-oxide-semiconductor (MOS) capacitor by self-consistently solving the one dimensional Poisson's equation and semi-classical charge density. Also analytical expressions are derived under depletion approximation and they are compared with the self-consistent simulation results. Analytical expressions of different levels of approximation are used to study the current-voltage (I-V) characteristics, subthreshold current, and quasi-Fermi potential along the channel of an n-channel metal-oxide semiconductor field effect transistor (MOSFET). Analytical and simulation results of MOS capacitor match well at relatively low biases. The current in MOSFETs with different approximation match pretty well at low bias and the parabolic approximation underestimate the current at higher biases.

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Authorization page

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Chapter 1: Introduction

1.1: History of Field Effect Transistors

The first patent for the field-effect transistors (FETs) principle was filed in Canada by Austrian-Hungarian physicist Julius Edgar Lilienfeld on October 22, 1925. Unfortunately he never got it to work because he did not fully appreciate the role of surface defects or surface states, in the process of trying to demonstrate experimentally such a field effect transistor. Lilienfeld did not publish any research articles about his devices. In 1934 German physicist Dr. Oskar Heil patented another field-effect transistor [1].

On 17 November 1947,John Bardeen and Walter Brattain, at AT&T Bell Labs, observed that when electrical contacts were applied to a crystal of germanium, the output power was larger than the input. William Shockley saw the potential in this and worked over the next few months greatly expanding the knowledge of semiconductors [2]. According to physicist/historian Robert Arns, legal papers from the Bell Labs patent show that William Shockley and Gerald Pearson had built operational versions from Lilienfeld's patents, yet they never referenced this work in any of their later research papers or historical articles. The problem of surface states was resolved by growing an oxide insulator on Si, and the first MOSFET was demonstrate in 1960 by Kahng and Atalla [3].

1.2: The two-terminal MOS capacitor

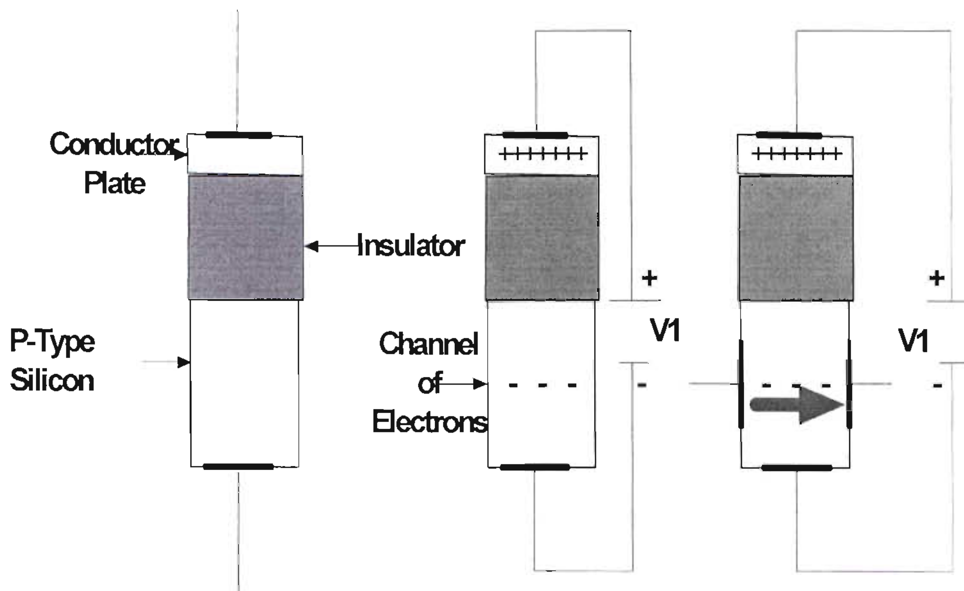


Figure 1: MOS capacitor as like parallel plate capacitor.

The heart of the MOSFET is the metal oxide-semiconductor capacitor shown in Figure 1. The metal may be aluminum or some other type of metal, although in many cases, it is actually a high-conductivity polycrystalline silicon that has been deposited on the oxide; however, the term metal is usually still used.

The physics of the MOS structure can be more easily explained with the aid of the simple parallel plate capacitor. An insulator material separates the two plates. A parallel plate capacitor with the top plate at a negative voltage with respect to the bottom plate, a negative charge exists on the top plate. A positive charge exists on the bottom plate, and an electric field is induced between the two plates as shown in figure 2. The capacitance per unit area for this geometry is

$$C = \frac{\varepsilon}{d} \quad (1)$$

where ε is the permittivity of the insulator and d is the distance between the two plates. The magnitude of the charge per unit area on either plate is

$$Q = CV \quad (2)$$

where the indicates charge or capacitance per unit area and V is the applied voltage. The magnitude of the electric field is

$$E = \frac{V}{d} \quad (3)$$

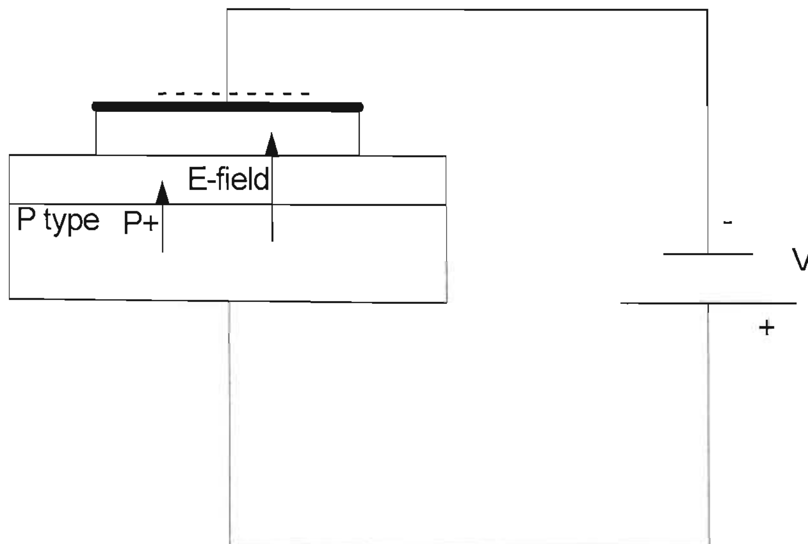


Figure 2: The MOS capacitor with a p-type semiconductor substrate.

The top metal gate is at a negative voltage with respect to the semiconductor substrate. From the example of the parallel-plate capacitor, we can see that a negative charge will exist on the top metal plate and an electric field will be induced with the direction shown in the figure. If the electric field were to penetrate into the semiconductor, the majority carrier holes would experience a force toward the oxide-semiconductor interface.

Now consider the case when a larger positive voltage is applied to the top metal gate of the MOS capacitor. We expect the induced electric field to increase in magnitude and the corresponding positive and negative charges on the semiconductor to increases. A larger negative charge in the MOS capacitor implies a larger induced space charge region and more band bending. Figure 3 shows such a condition. The intrinsic Fermi level at the surface is now below the Fermi level: thus, the conduction band is closer to the Femi level than the valence band is. This result implies that the surface in the semiconductor adjacent to the oxide-semiconductor interface is n type.

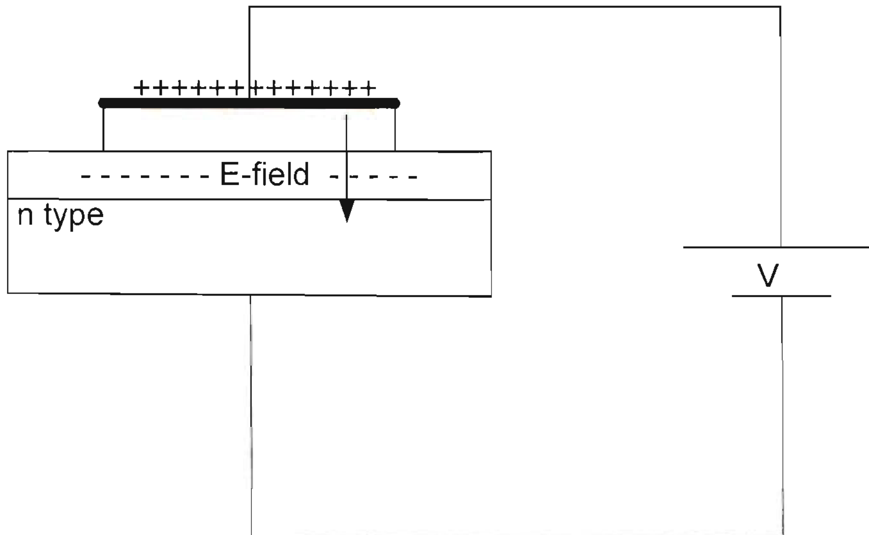


Figure 3: The MOS capacitor with an n-type substrate for a positive gate bias.

By applying a sufficiently large positive gate voltage, we have inverted the surface of the semiconductor from a p-type to an n-type semiconductor. We have created an inversion layer of electrons at the oxide-semiconductor interface.

In the MOS capacitor structure that we have just considered, we assumed a p-type semiconductor substrate. Figure 3 shows the MOS capacitor structure with a positive voltage applied to the top gate terminal. A positive charge exists on the top gate and an electric field is induced with the direction shown in the figure [4].

1.3: The flat band voltage

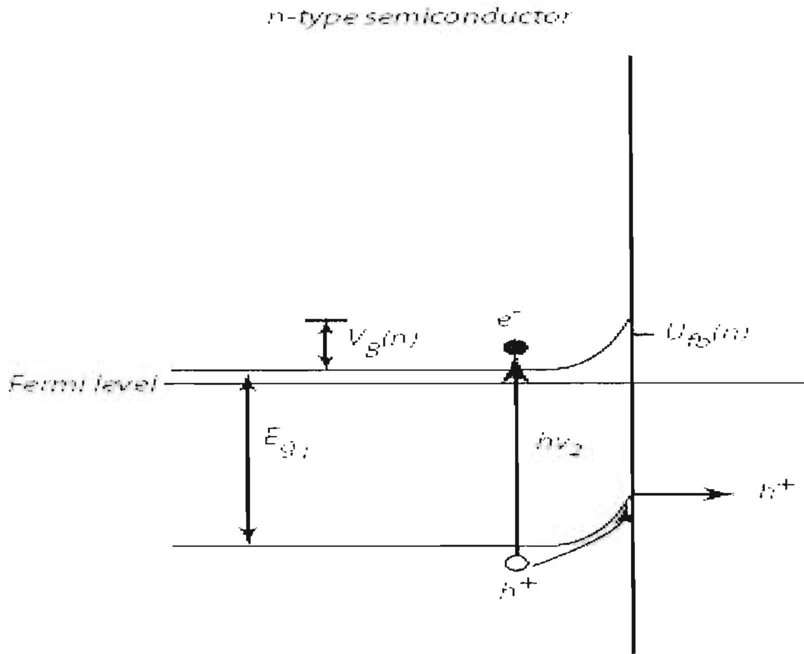


Figure 4: Flat band condition for an n-MOS.

The flat-band voltage is defined as the applied gate voltage such that there is no band bending in the semiconductor and, as a result, zero net space charge in this region. Figure 4 shows this flat-band condition. Because of the work function difference and possible trapped charge in the oxide, the voltage across the oxide for this case is not necessarily zero. We have implicitly been assuming that there is zero net charge density in the oxide material. This assumption may not be valid. A net fixed charge density, usually positive, may exist in the insulator. The positive charge has been identified with broken or dangling covalent bonds near the oxide-semiconductor interface. During the thermal formation of SiO_2, oxygen diffuses through the oxide and reacts near the Si-SiO_2 interface to form the SiO_2. Silicon atoms may also break away from the silicon material just prior to reacting to form SiO_2.

When the oxidation process is terminated, excess silicon may exist in the oxide near the interface, resulting in the dangling bonds. The magnitude of this oxide charge seems, in general, to be a strong function of the oxidizing conditions such as oxidizing ambient and temperature. The charge density can be altered to some degree by annealing the oxide in an argon or nitrogen atmosphere. However, the charge is rarely zero.

The net fixed charge in the oxide appears to be located fairly close to the oxide semiconductor interface. We will assume in the analysis of the MOS structure that an equivalent trapped charge per unit area, Q_{SS}, is located in the oxide directly adjacent to the oxide-semiconductor interface. For the moment, we will ignore any other oxide-type charges that may exist in the device. The parameter Q_{SS}, is usually given in terms of number of electronic charges per unit area.

For zero applied gate voltage, we can write

$$V_{OX0}+\varphi_{SO} = -\varphi_{ms} \tag{4}$$

If a gate voltage is applied, the potential drop across the oxide and the surface potential will change. Then we write

$$V_G = \Delta V_{OX}+ \Delta\varphi_S=(V_{OX} - V_{OX0}) + (\varphi_s - \varphi_{so}) \tag{5}$$

Using Equation (4), we have

$$V_G = V_{OX}+ \varphi_S+\varphi_{mS} \tag{6}$$

Figure 4 shows the charge distribution in the MOS structure for the flat-band condition. There is zero net charge in the semiconductor and we can assume that an equivalent fixed surface charge density exists in the oxide. The charge density on the metal is Q_m and from charge neutrality we have

$$Q_m + Q_{ss} = 0 \tag{7}$$

We can relate, Q_m , to the voltage across the oxide by

$$V_{ox}=\frac{Q_m}{C_{ox}} \tag{8}$$

where C_{ox} is the oxide capacitance per unit area. Substituting Equation (7) in Equation (8). we have,

$$V_{ox}=\frac{-Q_{SS}}{C_{ox}} \tag{9}$$

In the flat-hand condition, the surface potential is zero, or φ_s=0.Then from Equation (6). we have

$$V_G = V_{FB} = \varphi_{ms} - \frac{Q_{SS}}{C_{OX}} \tag{10}$$

Where V_{FB} is the flat band voltage for this MOS device [5].

1.4: Threshold Voltage

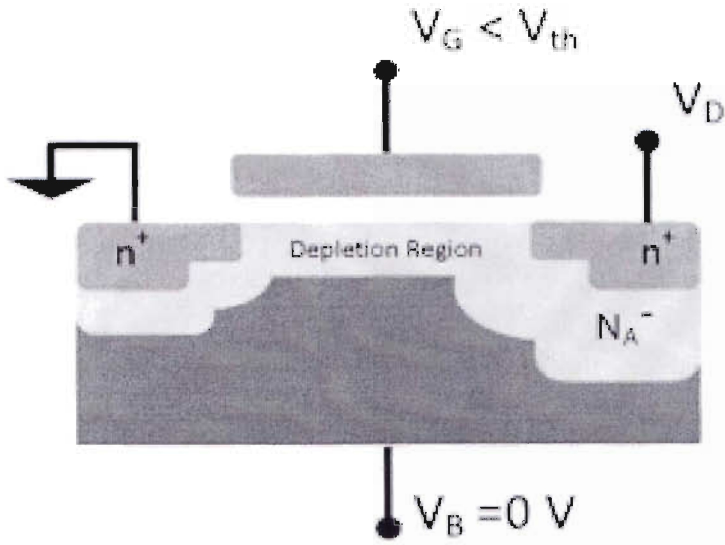


Figure 5: Depletion region of an n-MOSFET biased below threshold

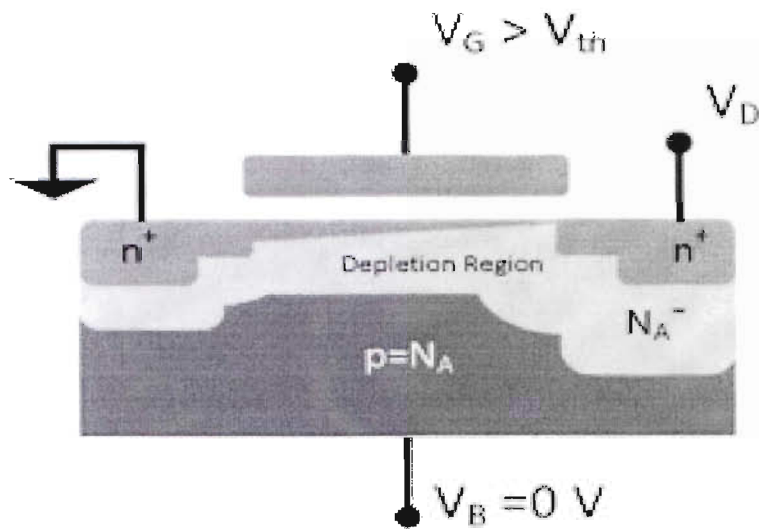


Figure 6: Depletion region of an n-MOSFET biased above threshold with channel formed.

The threshold voltage of a MOSFET is defined as the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor .

In an n-MOSFET, the substrate of the transistor is composed of p-type silicon, which has positively charged mobile holes as carriers. When a positive voltage is applied on the gate, an electric field causes the holes to be repelled from the interface, creating a depletion region containing immobile negatively charged acceptor ions. A further increase in the gate voltage eventually causes electrons to appear at the interface, in what is called an inversion layer, or channel. In practical, the threshold voltage is the voltage at which there are sufficient electrons in the inversion layer to make a low resistance conducting path between the MOSFET source and drain.

In figure 5, the source and drain are labeled n^+ to indicate heavily doped n-regions. The depletion layer dopant is labeled N_A^- to indicate that the ions in the depletion layer are negatively charged and there are very few holes. In the bulk the number of holes $p = N_A$ making the bulk charge neutral.

If the gate voltage is below the threshold voltage, the transistor is turned off and ideally there is no current from the drain to the source of the transistor. In fact, there is a current even for gate biases below threshold (sub threshold leakage current), although it is small and varies exponentially with gate bias.

If the gate voltage is above the threshold voltage, the transistor is turned on, due to there being many electrons in the channel at the oxide-silicon interface, creating a low-resistance channel where charge can flow from drain to source. For voltages significantly above threshold, this situation is called strong inversion. The channel is tapered when $V_D > 0$ because the voltage drops due to the current in the resistive channel reduces the oxide field supporting the channel as the drain is approached [6].

To account for the threshold shift from nonzero flat-band voltage whose main cause comes from fixed oxide charges Q_{SS} and the work-function difference φ_{ms} between the gate material and the semiconductor, the equation becomes,

$$V_T = V_{FB} + \varphi_S + \sqrt{\frac{2\varepsilon_S N_A \varphi_S}{C_{OX}}} \quad (11)$$

$$= \varphi_{ms} - \frac{Q'_{SS}}{C_{OX}} + \varphi_S + \sqrt{\frac{2\varepsilon_S N_A \varphi_S}{C_{OX}}} \quad (12)$$

$$=\varphi_{ms} - \frac{Q_{SS}}{C_{OX}} + 2\varphi_F + \sqrt{\frac{4\varepsilon_S N_A \varphi_F}{C_{OX}}} \quad (13)$$

where $\varphi_S = 2\varphi_F$ qualitatively, V_T is the gate bias beyond flat-band just starting to induce an inversion charge sheet and is given by the sum of voltages across the semiconductor ($2\varphi_F$) and the oxide layer. The square-root term is the total depletion-layer charge.

When a substrate bias is applied (negative for n-channel or p-substrate), the threshold voltage becomes

$$V_T = \varphi_{ms} - \frac{Q_{SS}}{C_{OX}} + \varphi_S + \sqrt{\frac{2\varepsilon_S N_A(\varphi_S - V_{BS})}{C_{OX}}} \quad (14)$$

where, $\varphi_F = V_T \ln\frac{N_A}{n_i}$ for p-substrate and V_{BS} is the reverse sub threshold voltage[7].

1.5: Body effect:

The body effect describes the changes in the threshold voltage by the change in V_{SB}, the source-bulk voltage. Since the body influences the threshold voltage (when it is not tied to the source), it can be thought of as a second gate, and is sometimes referred to as the "back gate"; the body effect is sometimes called the "back-gate effect" [8].

For an enhancement mode, n-MOSFET body effect upon threshold voltage is computed according to the Shichman-Hodges model (accurate for very old technology) using the following equation.

$$V_T = V_{T0} + \gamma\left(\sqrt{V_{SB} + 2\varphi_F} - \sqrt{2\varphi_F}\right) \quad (15)$$

where V_T is the threshold voltage when substrate bias is present, V_{SB} is the source-to-body substrate bias, $2\varphi_F$ is the surface potential, V_{T0} is the threshold voltage for zero substrate bias, and $\gamma = \left(\frac{t_{ox}}{\varepsilon_{ox}}\right)\sqrt{2q\varepsilon_S N_A}$ Is the body effect parameter. Here t_{ox} is oxide thickness, ε_{ox} is oxide permittivity, ε_S is the permittivity of silicon, N_A is a doping concentration, and q is the charge of an electron [9].

1.6: Basic structure and operation:

FETs are divided into two families: junction FET (JFET) and insulated gate FET (IGFET). The IGFET is more commonly known as metal–oxide–semiconductor FET (MOSFET), from their original construction as a layer of metal (the gate), a layer of oxide (the insulation), and a layer of semiconductor. Unlike IGFETs, the JFET gate forms a PN diode with the channel which lies between the source and drain. Functionally, this makes the N-channel JFET the solid state equivalent of the vacuum tube triode which, similarly, forms a diode between its grid and cathode. Also, both devices operate in the depletion mode, they both have a high input impedance, and they both conduct current under the control of an input voltage.

Metal–semiconductor FETs (MESFETs) are JFETs in which the reverse biased PN junction is replaced by a metal–semiconductor Schottky-junction. These, and the HEMTs (high electron mobility transistors, or HFETs), in which a two-dimensional electron gas with very high carrier mobility is used for charge transport, are especially suitable for use at very high frequencies (microwave frequencies; several GHz) [10].

FETs are further divided into depletion-mode and enhancement-mode types, depending on whether the channel is turned on or off with zero gate-to-source voltage. For enhancement mode, the channel is off at zero bias, and a gate potential can "enhance" the conduction. For depletion mode, the channel is on at zero bias, and a gate potential (of the opposite polarity) can "deplete" the channel, reducing conduction. For either mode, a more positive gate voltage corresponds to a higher current for N-channel devices and a lower current for p-channel devices. Nearly all JFETs are depletion-mode as the diode junctions would forward bias and conduct if they were enhancement mode devices; most IGFETs are enhancement-mode types.

We can see that the simple view of the MOS transistor is the figure 7. The transistor is formed on a p-type silicon body. If the gate potential is made sufficiently positive with respect to other parts of the structure, electrons can be attached directly below the insulator. these electrons can come through the n+ regions, where they exits in abundance, and can fill the channel between them, and the device is called an n-channel device. The number of electrons in the channel can be varied through the gate potential. This can cause a variation of the “strength” of the connection between the two n^+ regions, resulting in transistor action. If the two n+ region acts as a source for electrons, which then flow through the channel and are drained by the higher-potential n+ region. It is thus common to call the lower-potential n+ region source, and the higher-potential one drain [11].

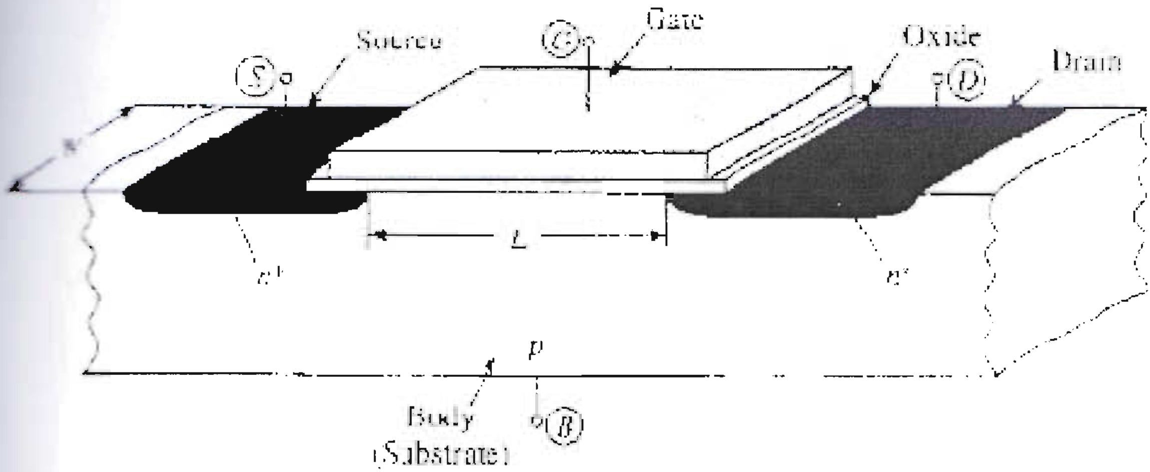


Figure 7: simplified structure of an n-MOSFET

The current in an MOS field-effect transistor is due to the flow of charge in the inversion layer or channel region adjacent to the oxide- semiconductor interface. We have discussed the creation of the inversion layer charge in enhancement-type MOS capacitors. We may also have depletion-type devices in which a channel already exists at zero gate voltage.

As can be seen on the figure the source and drain regions are identical. It is the applied voltages, which determine which n-type region provides the electrons and becomes the source, while the other n-type region receives the electrons and becomes the drain. The voltages applied to the drain and gate electrode as well as to the substrate, by means of a back contact, are referred to the source potential, as also indicated in Figure 7.

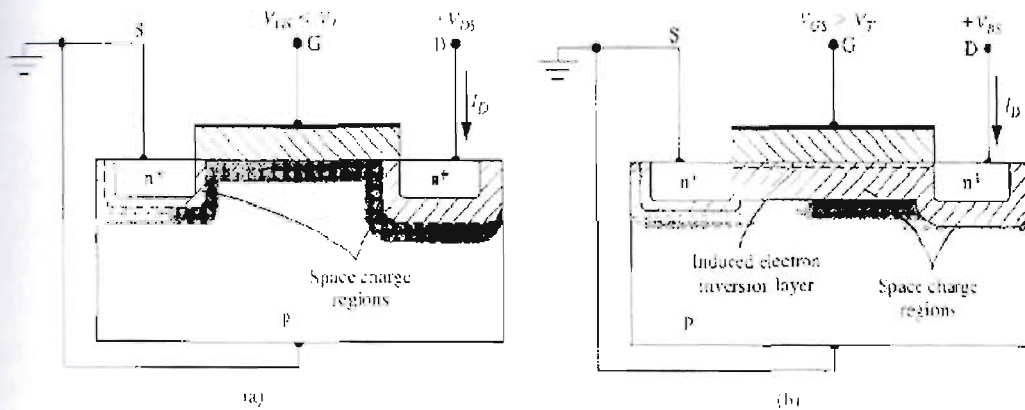


Figure 8: The n-channel enhancement mode MOSFET (a) with an applied gate voltage $V_{GS} < V_T$, and (b) with an applied gate voltage $V_{GS} > V_T$.

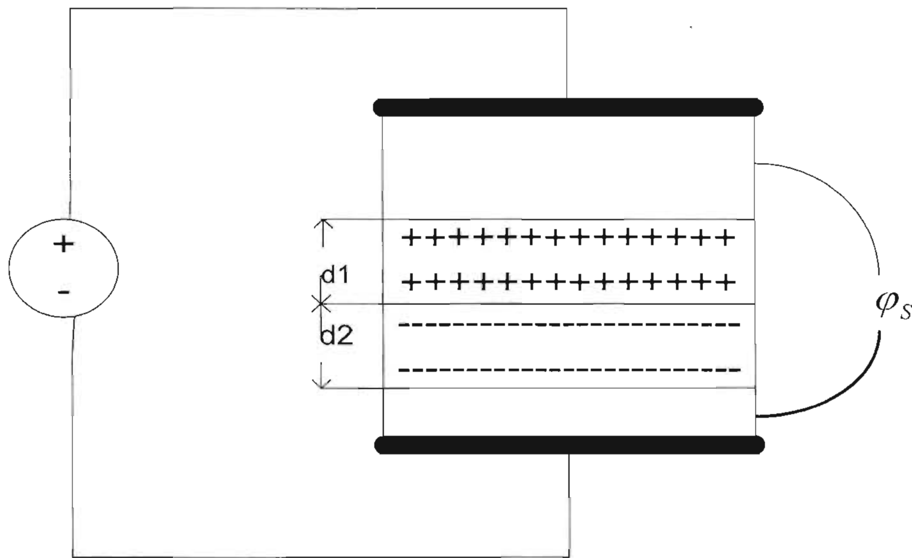


Figure 9: The MOS having the surface charge is zero.

The source and the drain form two pn junctions with the body as we have assumed above. These are reverse-biased.as has been shown in fig 8. In a pn junction the resulting depletion region extends to both the n and p sides. However, in the n-MOS transistor the part inside the n regions is much shallower, since the doping there is much heavier; thus that part is not shown for simplicity. We have assumed that the drain potential is more positive than the source potential. Thus, the reverse bias across the drain-body pn junction is larger, and the depletion region shown for that junction is deeper. As a result, there are large numbers of negatively charged acceptor atoms around the drain than there are near the source. This means that fewer electrons are needed in the channel near the drain to balance the positive charges on the gate. It is for the reason that the concentration of electrons shown to decreases as the drain is approached in Figure 7. The largest electron concentration is found near the source. The larger the value of the gate potential, the more the electrons and the "heavier" the inversion is at that point. A few volts of variation of the gate potential can vary the population of electrons there by several orders of magnitude. Although such variations continuous, we often say that as the gate potential is raised, we go from weak inversion to moderate inversion, and eventually to strong inversion. It will be seen that, when appropriately done, this division into three regions is convenient, as distinct types of behavior are observed in each of the three regions [12].

A MOSFET in Saturation.

Charge carriers in a MOSFET originate in source(S) and flow into drain(D). The total amount of charge that flows depends on how much charge is injected into channel from

source. This is controlled by the gate-source bias, V_{gs}. The drain current may or may not depend on the voltage drop between source and drain. It depends on Inversion Channel on the date-source Voltage and on the gate-drain Voltage.

First, the inversion channel at the Source-end is controlled by V_{gs}, and at the drain-end by V_{gd}. For an n-channel MOSFET, the inversion channel is present at the source-end of channel if $V_{gs} > V_t$ and is present at the drain-end of channel if $V_{gd} > V_t$.

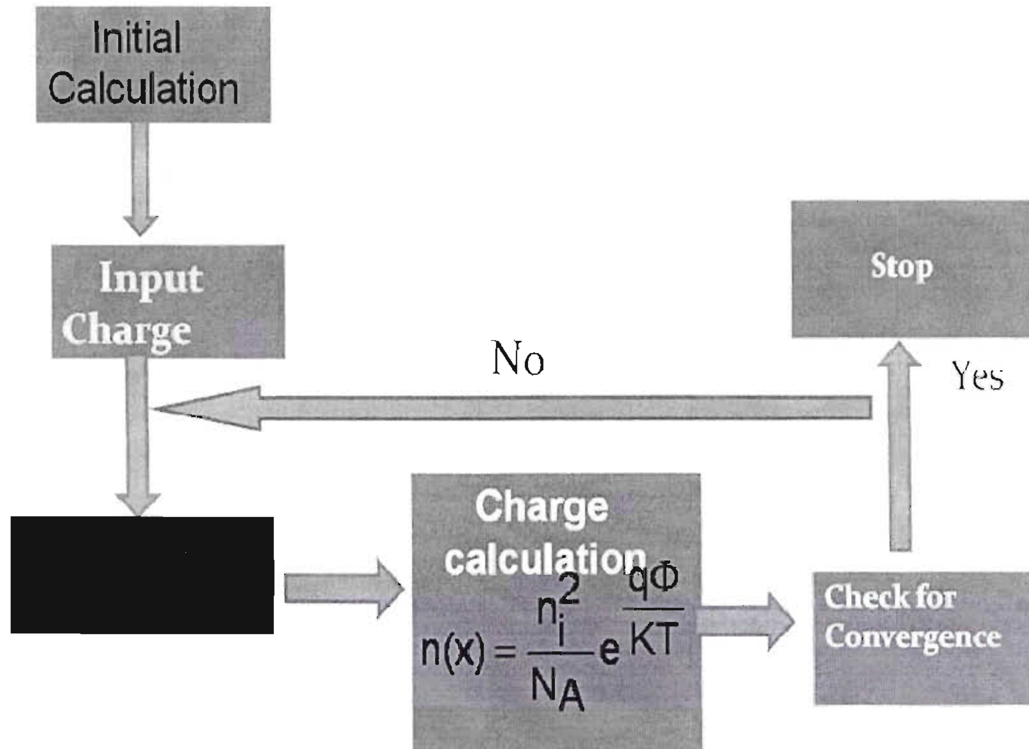
If $V_{gs} > V_t$ and $V_{gd} > V_t$, then the n-channel is continuous all the way from S to D. The S and D are connected by a conductor (or a resistor) of a given resistance. The drain current increases if the voltage drop between S and D increases. The channel resistance depends on how much charge is injected at the S-end, which in turn is controlled by V_{gs} The drain current I_d depends on both V_{gs} and V_{gd} (or V_{dg}), and thus we call this region of operation a Triode.

If $V_{gs} > V_T$ and $V_{gd} < V_T$, then n-channel is present (or induced) at the S-end, but the channel is depleted at the D-end. That is, the n-channel is pinched off at the drain-end. When the drain-end of channel is pinched off, the current no longer depends on the voltage drop between S and D (actually there is a small dependence of I_d on V_{gd})

If $V_{gs} < V_t$ (and of course, $V_{gd} < V_t$), then no n-channel is present and no current flows [13].

Chapter 2: Model

Self Consistent loop (SCF)



In this chapter, we discuss the simulation model that we use to generate the results. The discussion is given for n-MOS only. The band diagram of MOS inversion layer is shown in Figure 10. In the figure z=0 is the oxide-semiconductor interface and positive z is in silicon, E_i is the intrinsic Fermi level, E_f is the Fermi energy, and z_d is the depletion layer width.

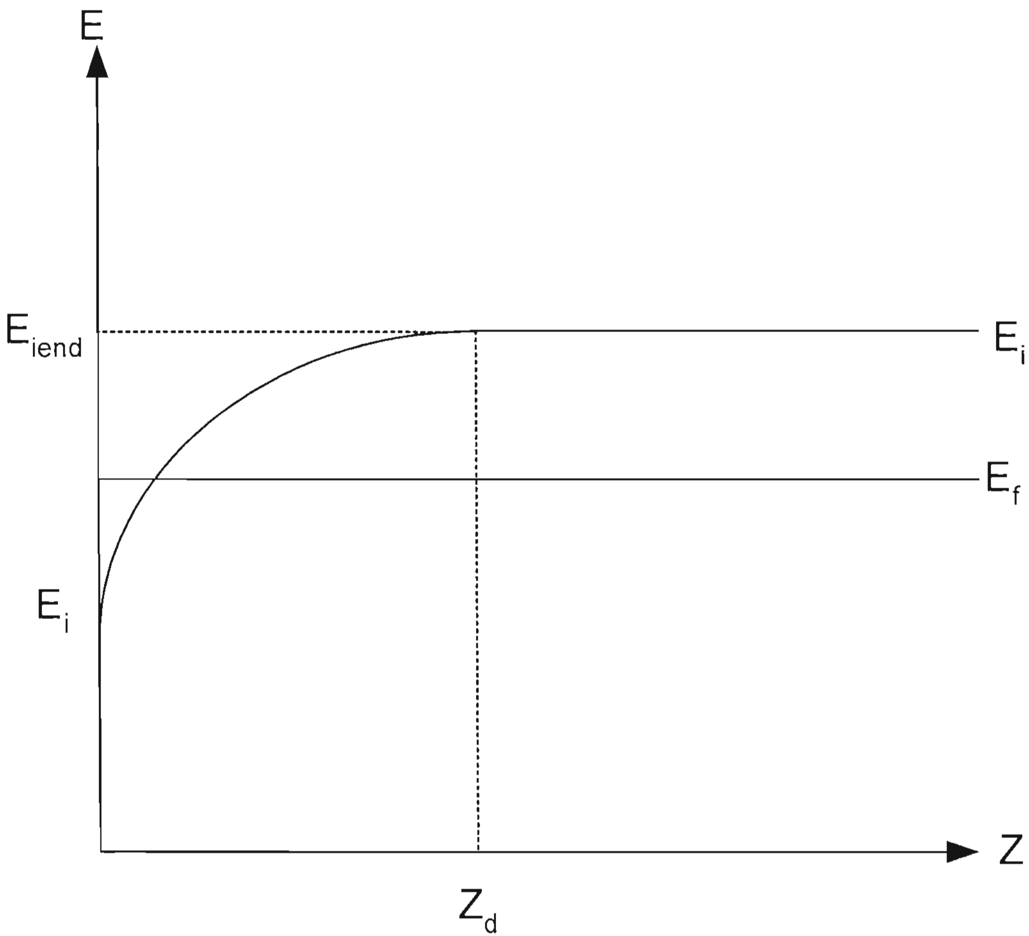


Figure 10: Band diagram of a MOS structure in inversion.

As there is no current flowing through the MOS structure E_f is constant. The electron and hole concentrations in silicon can be written as

$$n(z) = n_i e^{\frac{E_f - E_i(z)}{KT}} \qquad (16)$$

$$p(z) = n_i e^{\frac{E_i(z) - E_f}{KT}} \qquad (17)$$

Deep inside the silicon, where the band is flat, the electron and hole have their equilibrium values

$$n_o = n_i e^{\frac{-q\phi_F}{KT}} = n_i e^{\frac{E_f - E_{i\infty}}{KT}} \quad (18)$$

where $E_{i\infty}$ is the E_i at $z \to \infty$. Dividing Eq(17) by Eq(18), we get

$$n(z) = n_0 e^{\frac{E_{i\infty} - E_i(z)}{KT}}$$

$$n(z) = \frac{n_i^2}{N_A} e^{\frac{E_{i\infty} - E_i(z)}{KT}}$$

$$p(z) = N_A e^{-\left(\frac{E_{i\infty} - E_i(z)}{KT}\right)}$$

Therefore, the charge density at any position z in silicon is

$$\rho(z) = q(N_D - N_A - p(z) - n(z))$$

Poisson's equation for electric field is

$$\frac{d\xi}{dz} = \frac{\rho}{\varepsilon},$$

where ξ is the electric field given as $\xi = \frac{1}{q}\frac{dE_i}{\mathrm{dz}}$, Putting the expression of ξ , Poisson's equation becomes

$$\frac{d^2 E_i}{dz^2} = \frac{q\rho}{\varepsilon_0 \varepsilon_{si}}. \quad (19)$$

Using finite difference discretization with equal grid spacing of Δz , Equation (19) becomes

$$E_{n-1}^i - 2E_n^i + E_{n+1}^i = \frac{(\Delta z)^2 q}{\varepsilon_0 \varepsilon_{si}} \rho_n. \quad (20)$$

In matrix form eq.(20) becomes

$$\begin{bmatrix} -2 & 1 & & \\ 1 & -2 & 1 & \\ & & \ddots & \\ & & 1 & -2 \end{bmatrix} \begin{Bmatrix} E_1^i \\ E_2^i \\ \vdots \\ E_n^i \end{Bmatrix} = \frac{q(\Delta z)^2}{\varepsilon} \begin{Bmatrix} \rho_1 \\ \rho_2 \\ \vdots \\ \rho_n \end{Bmatrix}$$

As the boundary condition to solve Poisson's equation we set $E_i = 0$ at z=0 and $E_i = q\varphi_s$ at $z \to \infty$. Poisson's equation is self consistently solved with charge density defined in eqs. (16) & (17). The self consistent loop is started with $\rho(z) = qN_D$ for $z \le z_d$ and $\rho(z) = 0$ for $z > z_d$. Once the profile is converged, we have band diagram and calculate surface electric field and surface charge density as follows

$$F_s = \frac{1}{q}\frac{dE_i}{dz} = \frac{1}{q}\frac{E_1 - E_0}{z_1 - z_0}$$

$$|Q_s| = \varepsilon_0 \varepsilon_{si} F_s$$

2.1: Capacitance-Voltage Characteristics

The C-V characteristics of the MOS capacitor is studied by numerically evaluating the semiconductor capacitance as

$$C_S = \left| \frac{\partial Q_S}{\partial \phi_S} \right|$$

Here ϕ_S is the surface potential that we vary from 0 to 2.2 ϕ_F in the self consistent loop and obtain the gate voltage from

$$V_g = \phi_s + F_{ox} t_{ox} + V_{FB},$$

where F_{ox} is the oxide field given as

$$F_{ox} = \frac{\varepsilon_{si}}{\varepsilon_{ox}} F_s,$$

and V_{FB} is the flat band voltage given by

$$V_{FB} = -\frac{Q_i}{C_i} + \phi_{ms} \cdot$$

The oxide capacitance is

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

The total capacitance that is the gate capacitance is the series combination of the oxide capacitance and the semiconductor capacitance.

$$\frac{1}{C_G} = \frac{1}{C_{ox}} + \frac{1}{C_s}$$

$$C_G = \frac{C_s C_{ox}}{(C_s + C_{ox})}$$

2.2: Analytical Calculations

At any z, the Poisson's equation is

$$\frac{\partial^2 \phi}{\partial z^2} = -\frac{\rho(z)}{\varepsilon_s} \qquad (21)$$

and the charge density expression to solve for ϕ_s is

$$\rho(z) = q(N_D - N_A - p(z) - n(z)) \qquad (22)$$

We can solve this equation to determine the surface charge per unit area Q_S, as a function of the surface potential ϕ_s. Substituting n(z) and $\rho(z)$, we get

$$\frac{\partial^2 \phi}{\partial z^2} = \frac{\partial}{\partial z}\left(\frac{\partial \phi}{\partial z}\right) = -\frac{q}{\varepsilon_s}\left[p_o\left(e^{-\frac{q\phi}{kT}} - 1\right)n_o\left(e^{\frac{q\phi}{kT}} - 1\right)\right] \qquad (23)$$

Here $-\frac{\partial \phi}{\partial z}$ is the electric field ξ.

Integration the Eq (23) from the bulk towards the surface, we get

$$\int_{0}^{\frac{\partial\phi}{\partial z}}\left(\frac{\partial\phi}{\partial z}\right)d\left(\frac{\partial\phi}{\partial z}\right)=-\frac{q}{\varepsilon_s}\int_{0}^{\phi}\left[p_o\left(e^{-\frac{q\phi}{kT}}-1\right)n_o\left(e^{\frac{q\phi}{kT}}-1\right)\right]d\phi$$

After integration, we then get

$$\xi^2=\left(\frac{2kT\ p_o}{\varepsilon_s}\right)\left[\left(e^{-\frac{q\phi}{kT}}+\frac{q\phi}{kT}-1\right)+\frac{n_o}{p_o}\left(e^{\frac{q\phi}{kT}}-\frac{q\phi}{kT}-1\right)\right]$$

Substituting $\phi=\phi_s$ at the surface z=0, we get the expression of surface electric field

$$\xi_s=\frac{\sqrt{2}kT}{qL_D}\left[\left(e^{-\frac{q\phi_s}{kT}}+\frac{q\phi_s}{kT}-1\right)+\frac{n_o}{p_o}\left(e^{\frac{q\phi_s}{kT}}-\frac{q\phi_s}{kT}-1\right)\right] \qquad (24)$$

where the Debye screening length is

$$L_D=\sqrt{\frac{\varepsilon_s KT}{q^2 p_0}}\ . \qquad (25)$$

By using the Gauss's law at the surface, we can relate the integrated space charge per unit area to the electric field

$$Q_s=\varepsilon_s\xi_s\ . \qquad (26)$$

The positive charge Q_m on the metal is balanced by the negative charge Q_s in the semiconductor, which is the depletion layer charge plus the charge to the inversion region Q_n,

$$Q_m=-Q_s=qN_A z_d-Q_n \qquad (27)$$

Using the depletion approximation, we solve for z_d as a function of ϕ_s

$$z_d=\left[\frac{2\varepsilon_s\phi_s}{qN_A}\right]^{1/2} \qquad (28)$$

The depletion region grows with voltages across the capacitor until strong inversion is reached. After that, further increase in voltage results in stronger inversion rather than in more depletion. Thus the maximum value of the depletion width is

$$z_{dm} = \left[\frac{2\varepsilon_s \phi_s}{qN_A}\right]^{1/2} = 2\left[\frac{\varepsilon_s KT \ln(N_A / N_i)}{q^2 N_A}\right]^2 \quad (29)$$

The charge per unit area in the depletion region Q_d at strong inversion is

$$Q_d = -qN_A z_{dm} = -2(\varepsilon_s q N_A \phi_s)^2 \quad (30)$$

The applied voltage must be large enough to create this depletion charge plus the surface potential ϕ_s (inver).

2.3: I-V Characteristics

The induced charge Q_s in the semiconductor is composed of mobile charge Q_n and fixed charge in the depletion region Q_d.

$$Q_s = Q_n + Q_d$$

Mobile charge, $Q_n = -C_{ox}\left[V_G - \left(V_{FB} - \frac{Q_n + Q_d}{C_{ox}} + \phi_s\right)\right]$

Substituting Q_n+Q_d for Q_s,

$$Q_n = -C_{ox}\left[V_G - \left(V_{FB} - \frac{Q_s}{C_{ox}} + \phi_s\right)\right] \quad (31)$$

The threshold voltage is given by

$$V_T = -\frac{Q_d}{C_{ox}} + 2\phi_F - \frac{Q_{ox}}{C_{ox}} + \phi_{ms} \quad (32)$$

With a voltage V_D applied, there is a voltage rise V_z from the source to each point z in the channel. Thus the potential ϕ_s(z) is that required to achieve strong inversion ($2\phi_F$) plus the voltages V_z.

$$Q_n = -C_{ox}\left[V_G - V_{FB} - 2\phi_F - V_z - \frac{1}{C_{ox}}\sqrt{2q\varepsilon_s N_a(2\phi_F + V_z)}\right] \quad (33)$$

If we neglect the variation of $Q_d(z)$ with bias V_z, Eq. 38 can be simplified to

$$Q_n(z) = -C_{ox}(V_G - V_T - V_z) \quad (34)$$

This equation describes the mobile charge in the channel at point z. the conductance of the differential element dz is $\bar{\mu}_n Q_n(z) z_d / dz$, where z_d is the width of the channel and μ_n is a surface mobility. At point z we have

$$I_D dz = \mu z_d |Q_n(z)| dV_z \quad (35)$$

Integrating from source to drain

$$\int_0^L I_D dz = \mu z_d C_{ox} \int_0^{V_D} (V_G - V_T - V_z) dV_z$$

$$I_D = \frac{\mu z_d C_{ox}}{L}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right] \quad (36)$$

where $-\frac{\bar{\mu} z_d C_{ox}}{L}$ determines the conductance of the n-channel MOSFET. Again from the eq.34 for $Q_n(z)$, we obtains

$$I_D = \frac{\mu z_d C_{ox}}{L}\left[\left(V_G - V_{FB} - 2\phi_F - \frac{1}{2}V_D\right)V_D - \frac{2}{3}\frac{\sqrt{2\varepsilon_s q N_a}}{C_{ox}}\left\{(V_D + 2\phi_F)^{3/2} - (2\phi_F)^{3/2}\right\}\right] \quad (37)$$

2.4: Sub threshold current

If we look at the drain current expression (Eq.36), it appears that the current abruptly goes to zero as soon as V_G is reduced to V_T. In reality, there is still some drain conduction below threshold, and known as subthreshold conduction. This current is due to weak inversion in the channel between flatband and threshold (for bending between 0 and $2\phi_F$), which leads to a diffusion current from source to drain. The drain current in the subthreshold region is equal to

$$I_D = \mu_{eff} \frac{z_d}{L} \sqrt{\frac{\varepsilon q N_A}{2\phi_s}} \left(\frac{kT}{q}\right)^2 \left(\frac{ni}{N_A}\right)^2 * e^{\frac{q\phi_S}{KT}} \left(1 - e^{\frac{-qV_{GS}}{KT}}\right) \quad (38)$$

2.5: Quassi Fermi potential

The drain current expression is

$$I_D = (\mu C_{ox}) \frac{W}{L} [(V_g - V_T) V_{DS} - m - \frac{V_{DS}}{2}] \quad (39)$$

here $m = 1 + \frac{\sqrt{\varepsilon q N_A / 4\phi_F}}{C_{ox}}$

The semiconductor charge is given by

$$Q_S = -C_{ox}(V_G - V_{FB} - 2\phi_F - V)$$

here the fixed charge is

$$Q_d = -\sqrt{2\varepsilon q N_A (2\phi_F + V)^2}$$

$$= -\sqrt{2\varepsilon q N_A 2\phi_F} (1 + \frac{V}{2\phi_F})^{1/2}$$

$$= -\sqrt{2\varepsilon q N_A 2\phi_F} (1 + \frac{1}{2} \frac{V}{2\phi_F} + ...)$$

$$Q_d(z) = -\sqrt{2\varepsilon q N_A 2\phi_F} - \sqrt{\frac{\varepsilon V_z N_A}{4q\phi_F}}$$

$$Q_i = Q_S - Q_d$$

$$= - C_{ox}(V_G - V_{FT} - 2\phi_F - V) + \sqrt{2\varepsilon q N_A 2\phi_F} + \sqrt{\frac{\varepsilon V N_A}{4q\phi_F}}$$

$$-Q_i(v) = C_{ox}(V_G - V_{FB} - 2\phi_F - V) - \frac{\sqrt{4\varepsilon q N_A 2\phi_F}}{C_{ox}} - \left(1 + \frac{1}{C_{ox}} \sqrt{\frac{\varepsilon q N_A}{4\varphi_F}}\right) V$$

$$Q_i(V) = C_{ox}(V_g - V_T - mV)$$

$$I_D z = (\mu C_{ox})\{(V_g - V_T)V - \frac{m}{2}V^2\}$$

$$= (\mu C_{ox})\frac{W}{L}[(V_g - V_T)V_{DS} - m - \frac{V_{DS}}{2}]$$

$$= (\mu C_{ox})\{(V_g - V_T)V - \frac{m}{2}V^2\}$$

So, the Quasi Fermi potential

$$V = \frac{\frac{2}{m}(V_g - V_T) \pm \sqrt{\frac{z(V_g - V_T)}{m^2} - \frac{4z}{L}[\frac{2(V_g - V_T)}{m}V_{DS} - V_{DS}^2]}}{2}$$

$$\therefore V(z) = \frac{(V_g - V_T)}{m} - \sqrt{\frac{(V_g - V_T)}{m} - \frac{2z}{L}\frac{(V_g - V_T)}{m} + \frac{z}{2}V_{DS}^2}$$

Chapter 3:

Simulation Results and Discussions

In this chapter, we discuss the simulation results of both the MOS capacitor and the MOSFET.

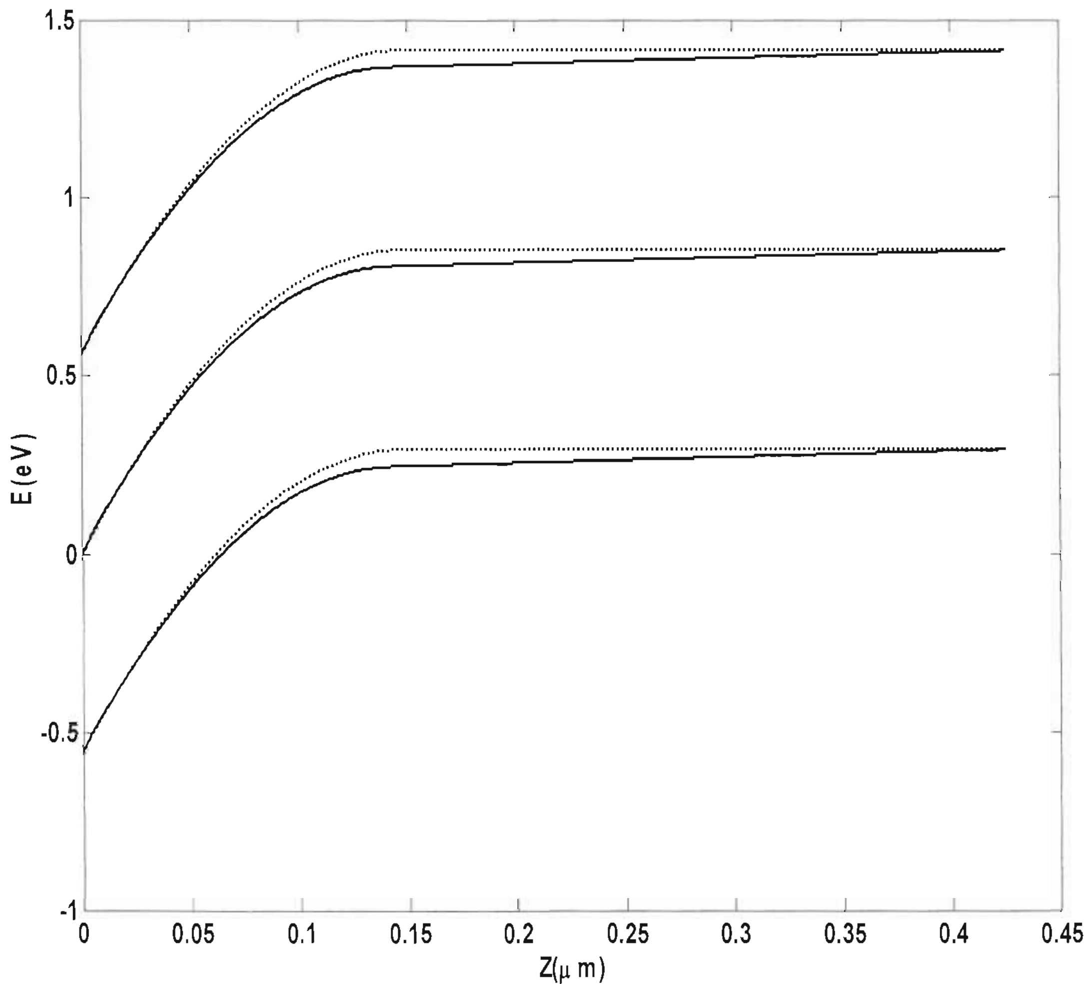


Figure11: Simulated band diagram for an n-MOS.

The simulated energy band diagrams are shown in the figure 11.The solid lines are self –consistent calculations and the dotted lines are analytical calculation under depletion approximation. The surface potential used in the calculation is $\varphi_s = 2\phi_F$ eV . Both the self-consistent and the analytical results match very well for this surface potential. We

notice that the results calculated in these two ways match pretty well for smaller ϕ_S and start to deviate when ϕ_S becomes ~ $2\phi_F$ or higher.

We apply a positive voltage to the gate metal. This raises the potential of the metal, lowering the metal Fermi level by qV relative to its equilibrium position. The positive voltage deposits positive charge on the metal and calls for corresponding net negative charges at the surface of the semiconductor. Such a negative charge in p-type material arises from depletion of holes from the region near the surface, leaving behind uncompensated ionized acceptors. This is analogous to the depletion region of a p-n junction .In the depletion region the hole concentration decreases, moving E_i closer to E_F, and bending the bands down near the semiconductor surface. If we continue to increase the positive voltage, the bands at the semiconductor surface bend down more strongly; in fact, a sufficiently large voltage can bend E_i below E_F. Since E_i>E_F implies electron concentration, the region near the semiconductor surface in this case has conduction band properties typical of n-type surface layer is formed not by doping, but instead by inversion of the originally p-type semiconductor due to the applied voltage. This inverted layer separated from the underlying p-type material by a depletion region, is the key to MOS operation.

Now we take a closer look at the inversion region, since it becomes the conducting channel in the FET. In the figure (11) we define a potential ϕ at any point z, measured relative to the equilibrium position of E_i. The energy $q\phi$ tells us the extent of band bending at z and $q\phi_s$ represents the bending at the surface. We note that ϕ_s=0 is the flat band condition. When ϕ_s < 0, the bands bend up at the surface, and we have hole accumulation. Similarly when ϕ_s > 0, we have depletion. Finally when ϕ_s is positive and larger than ϕ_F , the bands at the surface are bent down such that E_i (z=0) lies below E_F, and inversion is obtained

While it is true that the surface is inverted whenever ϕ_s is larger than ϕ_F , a practical criterion is needed to tell us whatever a true n-type conducting channel exists at the surface. The best criterion for strong inversion is that the surface should be as strongly n-type as the substrate is p-type. That is E_i should lie as far below E_F at the surface as it above E_F far from the surface. A surface potential of ϕ_F is required to bend the bands down to the intrinsic condition at the surface (E_i-E_F), and E_i must then be depressed another $q\phi_F$ at the surface to obtain the condition we call the strong inversion.

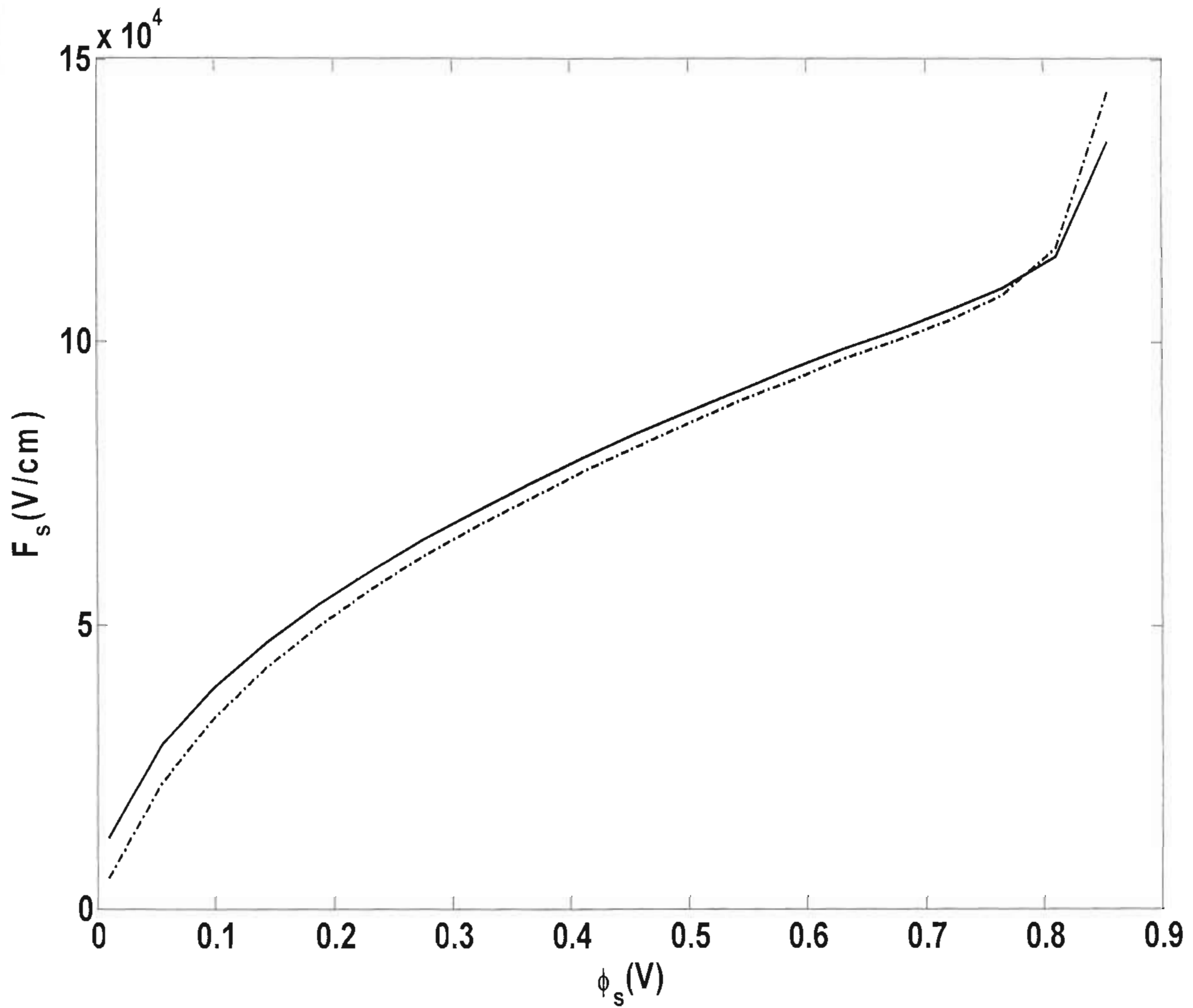


Figure12: Simulated surface electric field diagram for an n-MOS.

The simulated surface electric field diagrams are shown in the figure 12.The solid lines are self –consistent calculations and the dotted lines are analytical calculation. Initially self-consistent result leads the analytical result. When $\phi_S = 2\phi_F$, two results are exactly same. We notice that the results calculated in these two ways deviate for smaller ϕ_S and match pretty well for larger ϕ_S .

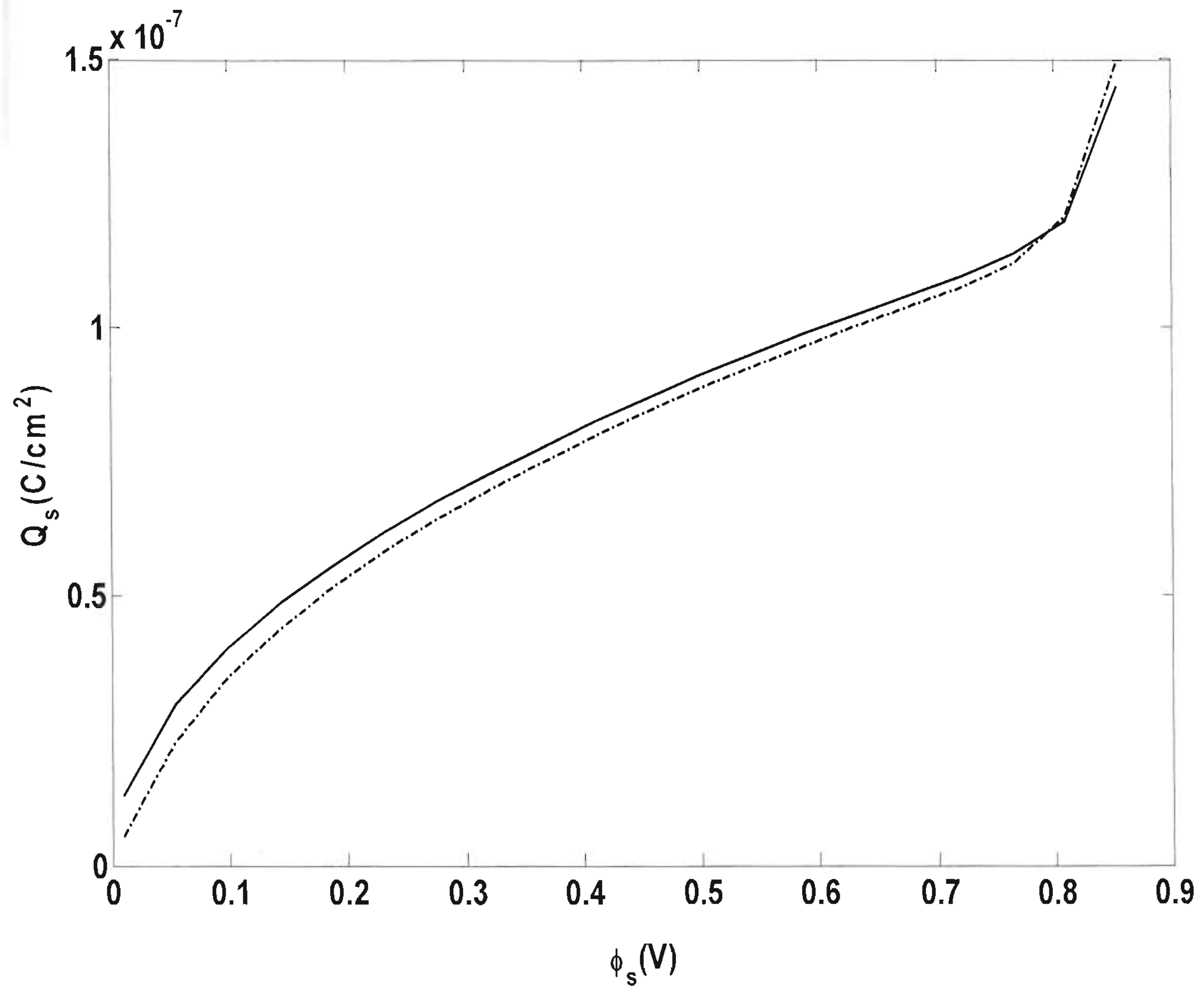


Figure13: simulated semiconductor charge density diagram for an n-MOS.

The simulated semiconductor charge density diagrams are shown in the figure 13.The solid lines are self –consistent calculations and the dotted lines are analytical calculation. The surface potential used in the calculation is $\phi_S = 2.2\phi_F$ eV. Initially self-consistent result leads the analytical result. When $\phi_s = 2\phi_F$, two results are exactly same. We notice that the results calculated in these two ways deviate for smaller ϕ_S and match pretty well for larger ϕ_S .

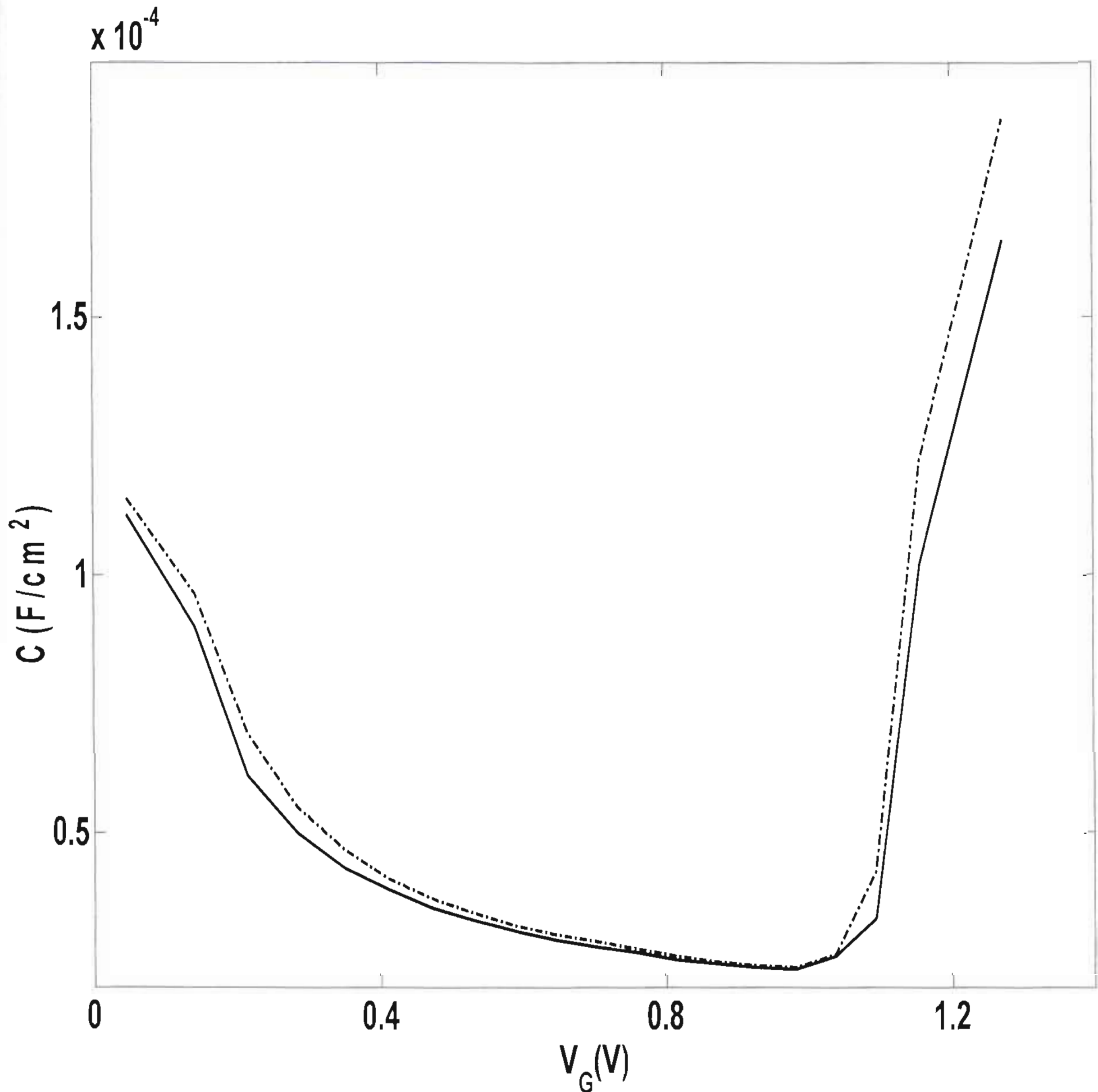


Figure 14: Simulated capacitance versus gate voltage diagram of an MOS capacitor.

The simulated capacitance versus gate voltage diagrams are shown in the figure 14.The solid lines are self –consistent calculations and the dotted lines are analytical calculation. The two results match pretty well in the depletion region and deviate in both the accumulation and the depletion regions.

Figure15: Simulated family of I_D versus V_{DS} curves for an n-channel MOSFET

The simulated families of ID versus VDS diagrams are shown in the figure 15.The solid lines are parabolic approximation and the dotted lines are long equation given in eq.36 and eq.37. The gate voltage used in the calculation is varied from 1 to 5 volts with an increment of 1 V. The drain voltage used in the calculation is varied from 1 to 5 volts. We notice that the results calculated in these two ways match pretty well for smaller V_D and V_G and start to deviate when V_D and V_G become ~ 2 V or higher. This means that the term that we ignore to derive the parabolic expression has larger contribution at higher voltages.

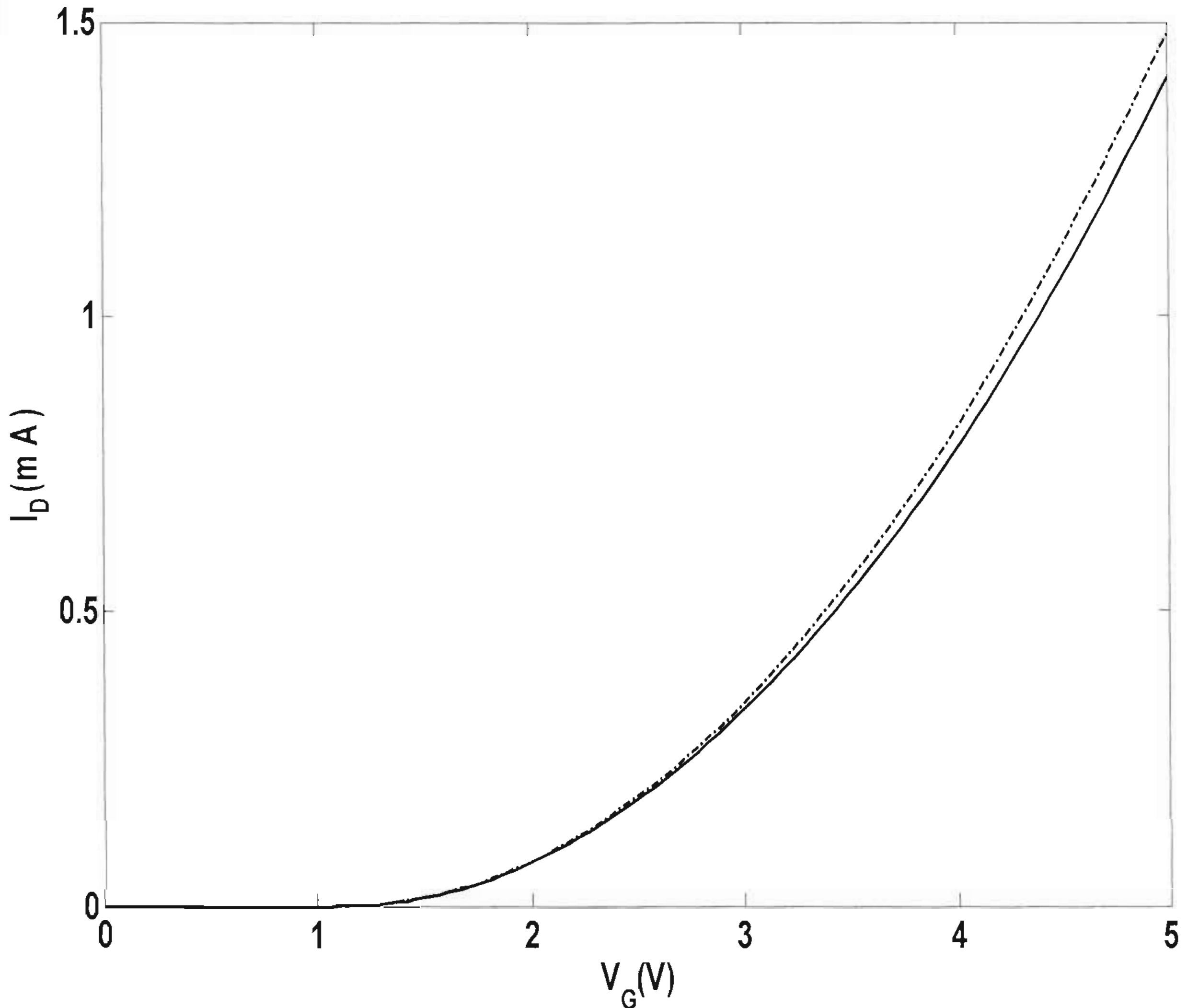


Figure16: Simulated I_D versus V_G (for fixed V_{DS}) diagram for enhancement mode MOSFET.

The simulated I_D versus V_G (for fixed V_{DS}) diagrams are shown in the figure 16.The solid lines are parabolic approximation and the dotted lines are long equation. The gate voltage used in the calculation is varied from 1 to 5 volts and the drain voltage is $V_D =$ 5V. Here we also noticed that the results calculated using eq.36 and eq.37 match well at lower V_G and deviate at larger gate biases.

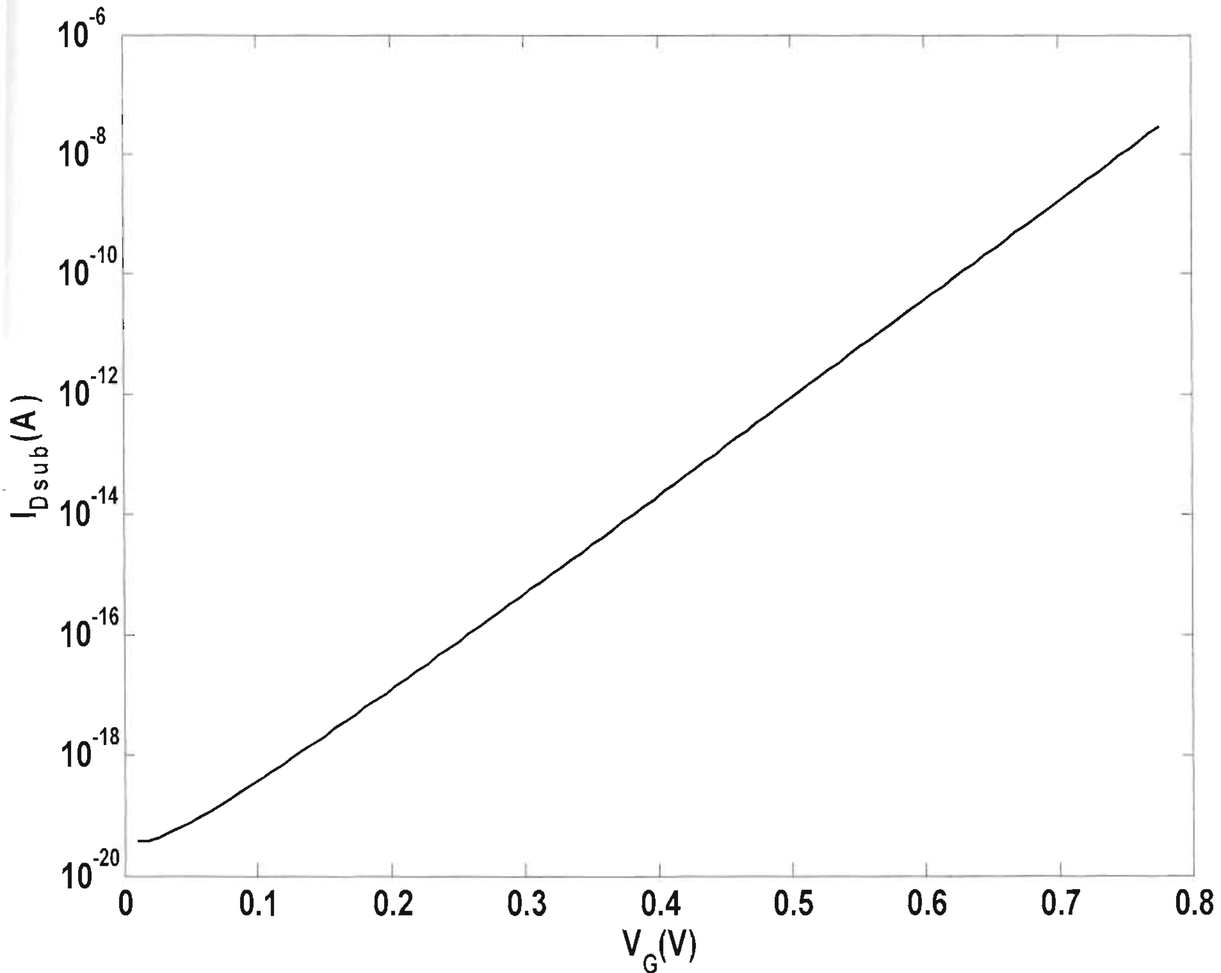


Figure17: Diagram I_{Dsub} versus V_G diagram of an n-MOS.

The simulated subthreshold current is shown in the figure 17. If we look at the drain current expression, it appears that the current abruptly goes to zero as soon as V_G is reduced to V_T and the value of V_T is 1.1V. The drain voltage is $V_D = 5$V. In reality, there is still some drain current below threshold, and this is known as sub threshold current. This current is due to weak inversion in the channel between flat band and threshold, and the current is mainly diffusion current.

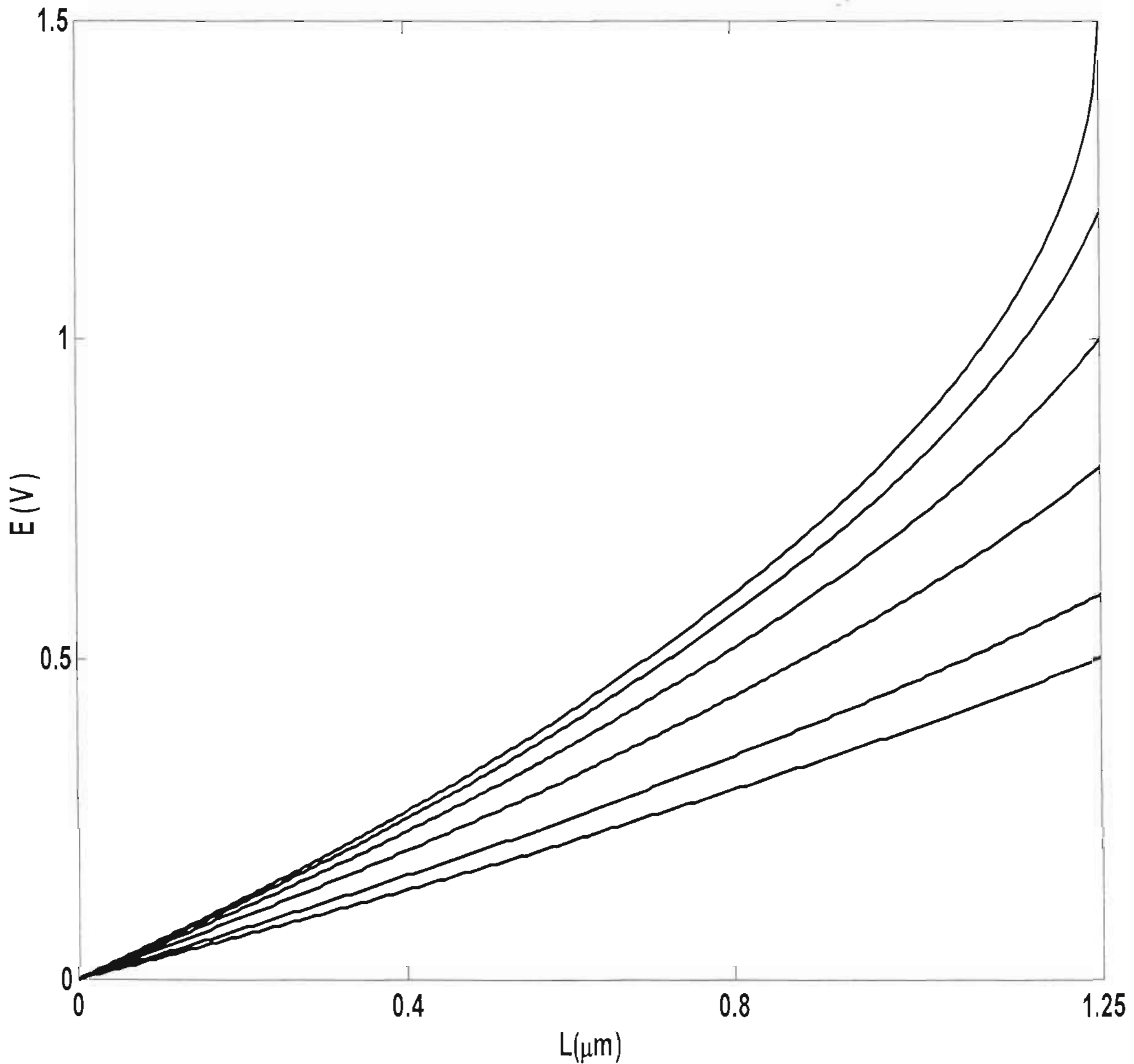


Figure 18: Simulated quasi Fermi potential versus the channel length diagram of the n-MOS

The simulated quasi Fermi potential versus the channel length diagrams are shown in the figure 18. Here we see for low voltage the lines are flat but when voltage increases the lines bend and for saturation voltage the line does not bend further. The drain current is directly proportional to the gradient of quasi-Fermi potential. As long as the quasi Fermi potential is straight line, the drain current is constant. As the quasi-Fermi potential stat to deviate from the straight line, the charge distribute in the change also have same to derivate to keep the drain current constant.

Chapter 4: Conclusion:

Self consistent simulation and analytical expressions are used to study a MOS capacitor and analytical expressions are used to study the I-V characteristic of a MOSFET. Analytical expressions are derived under depletion approximation. Then the analytical results are compared with the self-consistent simulation results. The analytical MOS capacitor match with the simulated results at relatively low biases. The current in MOSFETs with different approximation match pretty well at low bias and the parabolic approximation underestimate the current at higher biases. The subthreshold current (current at a gate bias below the threshold voltage) is mainly diffusion current and we simulate this current using analytical expression.

Chapter 5: Future work

The self-consistent model calculates the charge density from a semi-classical expression and therefore the quantum effects such as energy quantization are not studied. The model can be extended to include these effects by solving Schrodinger's equation with appropriate boundary conditions in the self-consistent loop.

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Appendix A:

Matlab code:

```
clear all
clc

%************************************************************************
%
%                         INPUT
%
%************************************************************************

NA = (5E16)*(1E6);          %substrate doping (/m3)
tox = (10)*(1E-9);          %oxide thickness (m)
phims = 0;                  %metal-semiconductor work function difference
Qss = 0;                    %oxide-Si interface trap chage density (C/m2)
W = (1.25)*(1E-6);          %device width (m)
L = (1.25)*(1E-6);          %device length (m)
mu = (650)*(1E-4);          %mobility (m2/V-s)
Ni = (1.5E10)*(1E6);        %intrinsic carrier concentration (/m3)
Eg = 1.12;                  %silicon band gap (eV)

%************************************************************************
%
%                         CONSTANT
%
%************************************************************************

q = 1.6E-19;                %electronic charge (C)
KB = 1.37824E-023;          %Boltzman constant (J/K)
T = 300;                    %temperature (K)
KBT = KB*T;                 %thermal energy (J)
KT = 0.0259;                %thermal energy (eV)
ep_air = 8.854E-12;         %free space permittivity (F/m)
ep_ox = 3.9;                %oxide dielectric constant
ep_si = 11.7;               %silicon dielectric constant

%************************************************************************
%
%                     A FEW CALCULATIONS
%
%************************************************************************

phif = (KBT/q)*log(NA/Ni);
Cox = ep_air*ep_ox/tox;
```

```
Wm = sqrt(4*ep_air*ep_si*phif/q/NA);
Vfb = phims-Qss/Cox;
VT = Vfb+q*NA*Wm/Cox+2*phif;

%************************************************************************
%
%        SELF CONSISTENT CALCULATION OF
%
%   (1) ENERGY BAND DIAGRAM, EiSCF (eV)
%   (2) SURFACE ELECTRIC FIELD, FsSCF (V/cm)
%   (3) DEPLETION CHARGE DENSITY, QdSCF (C/cm2)
%   (4) SEMICONDUCTOR CHARGE DENSITY, QsSCF (C/cm2)
%   (5) ELECTRON CHARGE DENSITY, QiSCF (C/cm2)
%
%************************************************************************

N = 500;
phis =linspace(0.01,2.2*phif,20);

Ei_0 = 0;
for nn = 1:length(phis)
   nn
   zd = sqrt(2*ep_air*ep_si*phis(nn)/q/NA);
   if phis(nn)<=2*phif
      zd = zd;
   else
      zd = sqrt(4*ep_air*ep_si*phif/q/NA);
   end
   z = linspace(0,3*zd,N);
   dz = z(2)-z(1);

   %*************** rho initialization **************

   rho = zeros(N,1);
   for ii = 1:length(z)
      if z(ii)<=zd
         rho(ii) = -q*NA;
      else
         rho(ii) = 0.0;
      end
   end
   rho = rho*dz*dz/ep_air/ep_si;

   %*************** initial profile **************

   pkernel = -2*diag(ones(N,1),0) + diag(ones(N-1,1),-1) + diag(ones(N-1,1),1);
```

```
%fixed (E_0) boundary at surface
rho = rho-pkernel(:,1)*Ei_0;
pkernel(:,1) = 0;
pkernel(1,:) = 0;
pkernel(1,1) = 1;
rho(1) = Ei_0;

%fixed (E_inf) boundary at deep in Si
rho = rho-pkernel(:,N)*phis(nn);
pkernel(:,N) = 0;
pkernel(N,:) = 0;
pkernel(N,N) = 1;
rho(N) = phis(nn);
Ei = pkernel\rho;

%*************** SELF-CONSISTENT ITERATION ****************

error = 100;
iter = 0;
Ei_old = Ei;
while (error>0.01 | iter<10)

    nz = (Ni^2/NA)*exp((Ei(end)-Ei)/KT);
    rho = zeros(N,1);
    for ii = 1:length(z)
        if z(ii)<=zd
            rho(ii) = -q*(nz(ii)+NA);
        else
            rho(ii) = -q*nz(ii);
        end
    end
    rho = rho*dz*dz/ep_air/ep_si;

    pkernel = -2*diag(ones(N,1),0) + diag(ones(N-1,1),-1) + diag(ones(N-1,1),1);
    %fixed (E_0) boundary at surface
    rho = rho-pkernel(:,1)*Ei_0;
    pkernel(:,1) = 0;
    pkernel(1,:) = 0;
    pkernel(1,1) = 1;
    %fixed (E_inf) boundary at deep in Si
    rho = rho-pkernel(:,N)*phis(nn);
    pkernel(:,N) = 0;
    pkernel(N,:) = 0;
    pkernel(N,N) = 1;
```

```
        rho(1) = Ei_0;
        rho(N) = phis(nn);

        Ei = pkernel\rho;
        Ei = 0.7*Ei + 0.3*Ei_old;

        error = max(Ei-Ei_old)*100;
        Ei_old = Ei;
        iter = iter+1; if iter==100 break; end
    end
    EiSCF(:,nn) = Ei;
    FsSCF(nn) = (1E-2)*(Ei(2)-Ei(1))/dz;
    QdSCF(nn) = (1E-4)*q*NA*zd;
    QiSCF(nn) = (1E-4)*(q*trapz(z,nz));
    QsSCF(nn) = QdSCF(nn)+QiSCF(nn);

end


%**************************************************************************

        ANALYTICAL CALCULATION OF

    (1) ENERGY BAND DIAGRAM, EiANT (eV)
    (2) SURFACE ELECTRIC FIELD, FsANT (V/cm)
    (3) DEPLETION CHARGE DENSITY, QdANT (C/cm2)
    (4) SEMICONDUCTOR CHARGE DENSITY, QsANT (C/cm2)
    (5) ELECTRON CHARGE DENSITY, QiANT (C/cm2)

%**************************************************************************

for nn = 1:length(phis)
    zd = sqrt(2*ep_air*ep_si*phis(nn)/q/NA);
    if phis(nn)<=2*phif
        zd = zd;
    else
        zd = sqrt(4*ep_air*ep_si*phif/q/NA);
    end
    K1 = (1/zd)*(phis(nn)+q*NA*zd^2/2/ep_air/ep_si);
    for ii = 1:length(z)
        if z(ii)<=zd
            EiANT(ii) = -q*NA*z(ii).^2/2/ep_air/ep_si+K1*z(ii);
            K2 = EiANT(ii);
        else
            EiANT(ii) = K2;
        end
```

```
  end
end
const = sqrt(2*KBT*NA/ep_air/ep_si);
term1 = exp(-q*phis./KBT)+q*phis/KBT-1.0;
term2 = ((Ni/NA)^2)*(exp(q*phis./KBT)-q*phis/KBT-1.0);
FsANT = (1E-2)*const*sqrt(term1+term2);
QsANT = (1E-4)*ep_air*ep_si*const*sqrt(term1+term2);
QdANT = (1E-4)*sqrt(2*ep_air*ep_si*q*NA)*phis;
Qi    = QsANT-QdANT;
if Qi<0
   QiANT = 0;
else
   QiANT = Qi;
end


%************************************************************************
%
%                 C-V CURVE
%
%              ANALYTICAL & SCF
%
%************************************************************************

CS = gradient(QsSCF,phis);
CgSCF = CS*Cox./(CS+Cox);
CgSCF = CgSCF/Cox;

CS = gradient(QsANT,phis);
CgANT = CS*Cox./(CS+Cox);
CgANT = CgANT/Cox;

VG = phis + (1E4)*QsSCF/Cox;


%************************************************************************
%
%                 DRAIN CURRENT CALCULATION
%
%              (1) LONG EQUATION
%              (2) SHORT EQUATION
%
%************************************************************************

Vg = [1 2 3 4 5];
Vd = linspace(0,5,100);
```

```
%Short equation
for kvg = 1:length(Vg)
   for kvd = 1:length(Vd)
      mm = 1+sqrt(ep_air*ep_si*q*NA/4/phif)/Cox;
      ID = (mu*Cox)*(W/L)*((Vg(kvg)-VT)*Vd(kvd)-mm*Vd(kvd)^2/2);
      Vdsat = (Vg(kvg)-VT)/mm;
      IDSS = (mu*Cox)*(W/L)*((Vg(kvg)-VT)*Vdsat-mm*Vdsat^2/2);
      if Vg(kvg)<VT
         ID_SE(kvg,kvd) = 0;
      elseif Vg(kvg)>=VT
         if Vd(kvd)>=(Vg(kvg)-VT)/mm
            ID_SE(kvg,kvd)= IDSS;
         else
            ID_SE(kvg,kvd) = ID;
         end
      end
   end
end

%Long equation
for kvg = 1:length(Vg)
   for kvd = 1:length(Vd)
      const = 2*sqrt(2*ep_air*ep_si*q*NA)/3/Cox;
      term1 = (Vg(kvg)-Vfb-2*phif-Vd(kvd)/2)*Vd(kvd);
      term2 = (2*phif+Vd(kvd))^(3/2)-(2*phif)^(3/2);
      ID = (mu*Cox)*(W/L)*(term1-const*term2);

      mm = 1+sqrt(ep_air*ep_si*q*NA/4/phif)/Cox;
      Vdsat = (Vg(kvg)-VT)/mm;
      term1 = (Vg(kvg)-Vfb-2*phif-Vdsat/2)*Vdsat;
      term2 = (2*phif+Vdsat)^(3/2)-(2*phif)^(3/2);
      IDSS = (mu*Cox)*(W/L)*(term1-const*term2);

      if Vg(kvg)<VT
         ID_LE(kvg,kvd) = 0;
      elseif Vg(kvg)>=VT
         if Vd(kvd)>=(Vg(kvg)-VT)/mm
            ID_LE(kvg,kvd)= IDSS;
         else
            ID_LE(kvg,kvd) = ID;
         end
      end
   end
end
```

```
%-----------------------------------------------------------------------



%-----------------------------------------------------------------------
Vg = linspace(0,5,100);
Vd = [5];

%Short equation
for kvg = 1:length(Vg)
   for kvd = 1:length(Vd)
      mm = 1+sqrt(ep_air*ep_si*q*NA/4/phif)/Cox;
      ID = (mu*Cox)*(W/L)*((Vg(kvg)-VT)*Vd(kvd)-mm*Vd(kvd)^2/2);

      Vdsat = (Vg(kvg)-VT)/mm;
      IDSS = (mu*Cox)*(W/L)*((Vg(kvg)-VT)*Vdsat-mm*Vdsat^2/2);
      if Vg(kvg)<VT
         ID_S(kvg,kvd) = 0;
      elseif Vg(kvg)>=VT
         if Vd(kvd)>=(Vg(kvg)-VT)/mm
            ID_S(kvg,kvd)= IDSS;
         else
            ID_S(kvg,kvd) = ID;
         end
      end
   end
end

%Long equation
for kvg = 1:length(Vg)
   for kvd = 1:length(Vd)
      const = 2*sqrt(2*ep_air*ep_si*q*NA)/3/Cox;
      term1 = (Vg(kvg)-Vfb-2*phif-Vd(kvd)/2)*Vd(kvd);
      term2 = (2*phif+Vd(kvd))^(3/2)-(2*phif)^(3/2);
      ID = (mu*Cox)*(W/L)*(term1-const*term2);

      mm = 1+sqrt(ep_air*ep_si*q*NA/4/phif)/Cox;
      Vdsat = (Vg(kvg)-VT)/mm;
      term1 = (Vg(kvg)-Vfb-2*phif-Vdsat/2)*Vdsat;
      term2 = (2*phif+Vdsat)^(3/2)-(2*phif)^(3/2);
      IDSS = (mu*Cox)*(W/L)*(term1-const*term2);

      if Vg(kvg)<VT
         ID_L(kvg,kvd) = 0;
      elseif Vg(kvg)>=VT
         if Vd(kvd)>=(Vg(kvg)-VT)/mm
```

```
            ID_L(kvg,kvd)= IDSS;
         else
            ID_L(kvg,kvd) = ID;
         end
      end
   end
end

%*************************************************************************
%
%           DRAIN CURRENT CALCULATION IN SUBTHRESHOLD
%
%*************************************************************************

VDS = 5;
PHIS = linspace(0.01,2*phif,100);
for ii = 1:length(PHIS)
   const = sqrt(ep_air*ep_si*q*NA/2/PHIS(ii))*(KBT/q)^2*(Ni/NA)^2;
   IDSTH(ii) = mu*(W/L)*const*exp(PHIS(ii)/KT)*(1-exp(-VDS/KT));
end

%*************************************************************************
%
%                QUASI FERMI LEVEL
%
%*************************************************************************
y = linspace(0,L,200);
m = 1;
Vd_sat =2.6-VT;
c= Vd_sat/m ;
Vds = [ 0.5 0.6 0.8 1 1.2 Vd_sat];
for i= 1:length(Vds)
   for j= 1:length(y)
    phi_n(i,j) = (Vd_sat/m )-sqrt((Vd_sat/m )^2-2*y(j)/L*(Vd_sat/m
)*Vds(i)+y(j)/L*Vds(i)^2);
   end
end
```