Feasibility Study of Sensor Application of Heavily Doped Nano-Ribbons Realized on Conventional SOI Platform

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The thesis title "Feasibility study of sensor application of heavily doped Nano-wires realized on conventional SOI platform" submitted by Mohammad Atikur Rahman [ID: 2010-2-80-025], Charles Dickens Tusha Falia [ID: 2010-2-80-031] And Sheikh Md. Razoan [ID: 2010-2-80-035] in the semester of spring, 2015 is approved satisfactory in partial fulfillment of the requirements for the requirements for the degree of Bachelor of Science in Electrical and Electronics Engineering.

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Declaration

We, hereby certify that our thesis work solely to be our own scholarly work. To the best of our knowledge, it has not been shared from any source without the due acknowledgement and permission. It is being submitted in partial fulfillment of requirements for the degree of Bachelor of Science in Electrical and Electronics Engineering. It has been submitted before any degree or examination of any other university.

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Spring Semester

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Abstract

We investigated feasibility of applying 100nm thick and 1μm long p-type Si NW with a body doping of $10^{18}/cm^3$ for sensor applications. It is found that such a p-type Si NW exhibits a subthreshold slope of 2772mV/dec to 9553.25mV/dec for backgate bias of 30V to -30V while applied V_D was positive. For negative V_D applications subthreshold slope vary from 2790mV/dec to 7989mV/dec when backgate bias is changed from 30V to -30V. Such a subthreshold slope is not promising sensor applications even though significant depletion is tried to be formed by 30V of backgate bias applications. Therefore, it may be concluded that 100nm thick SOI platform based Si NWs will not be suitable for sensor application at $10^{18}/cm^3$ body doping.

Acknowledgment

It is with immense gratitude that we acknowledge the help and help of our supervisor, Dr. Mohammad Mojammel AL Hakim, Associate Professor of Department of Electrical and Electronics Engineering, East West University. Without his guidance, encouragement and support this thesis would have remained a dream. We consider it an honor to work with him. We also indebted to our parents, other professors of the department, and friends for their support and encouragements. Finally thanks to almighty who gave us the patience to finish the task successfully.

Authorization Page

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CHAPTER 1: INTRODUCTION

The semiconductor nanowires are materials of great interest over the past daces due to their unique electrical characteristics for biochemical sensors applications. Biosensors based on silicon nanowire field-effect transistors (Si-NW-FETs) have drawn huge amounts of attention, due to their ultra sensitivity, label-free and real-time detection abilities. This ultra-high sensitivity detection can be attributed to their smaller size and large surface to volume ratio, enabling local charge transfers to result in a current change due to a field effect when analytic molecules bind to a specific recognition molecule at the surface of the nanowire [1]. The effect is so strong that single charge at the surface of the nanowire can even deplete or accumulate the entire cross sectional conductor path of these nanostructures [2].

Ample of works can be found in the literature employing Si-NWs for detecting biomarkers, individual bacteria or viruses. Unfortunately, in most of these works Si-NWS inherent characteristics have not been considered in detailed in which could have provided much better and unambiguous detection of biomarkers, bacteria or viruses. Si-NW biosensors hold great promise to realize point-of-care (POC) devices for disease diagnostics with potential for miniaturization and integration. In this work, we first time perform a systematic study on the electrical characteristics of 100nm thick heavily doped ($10^{18}/cm^3$) Si-NW. The work aims to perform a feasibility study on the application of heavily doped relatively thick Si-NW for Biosensor applications.

1.1 Background

The conductance changes of silicon nanowires upon attachment of bimolecular have been employed extensively for bio sensing applications. A number of works [3-6] can be founded in the literature exploiting this behavior for biosensors. However inherent nanowires electrical characteristics are found to be quite variable although they have been successfully applied for bio sensing application. These are discussed below.

A typical nanowire biosensor can be a single or an array of nanowires which is laid on an insulator between source and drain [Figure. 1.1]. Electrodes of these source and drain are isolated by a protection layer. On Si-NW surface, target receptors which have the capability of immobilizing the targets, e.g. ions, DNA, proteins are attached by molecular linkers. Due to large surface to volume ratio, the charges associated with the attached molecules can be deplete or accumulate entire cross sectional pathway. And hence nanowire conductance gets easily changed. This phenomenon resulted in the most promising breakthrough in the 21st century by possible application of simple nanowire device for disease diagnosis [7-14].

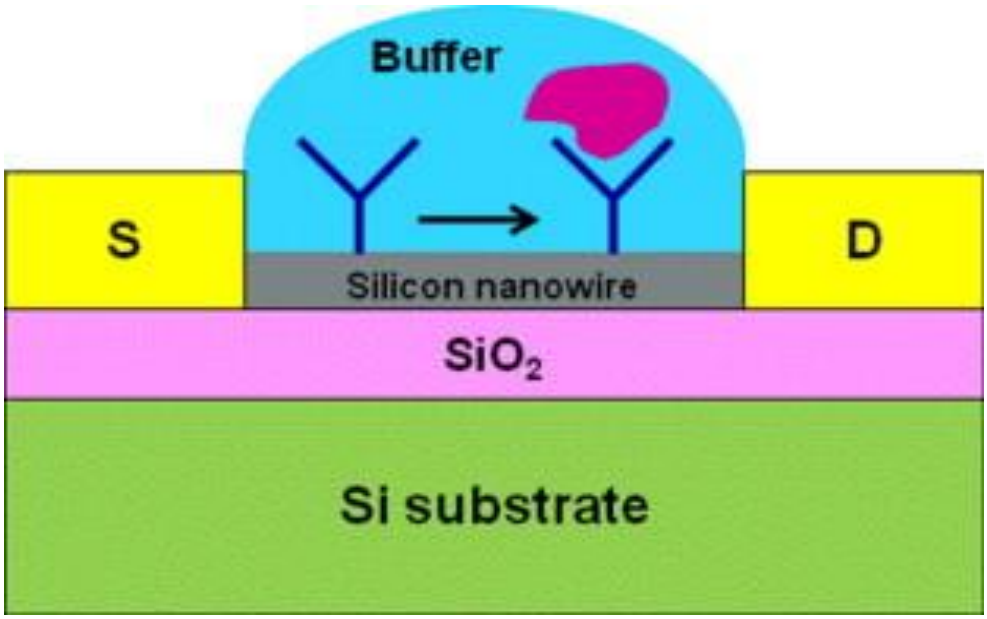

Figure 1.1: Schematic diagram of the structure of Si-NW biosensor.

Lieber et al. [3] successfully fabricated silicon nanowire biosensors on p-type semiconductor where the typical DC current voltage (I-V) characteristics were linear up to a small raise of applied bias. The ability of the fabricated biosensors was tested through pH response with or without modifying nanowire surface containing both amino or silanol receptor. It was shown that increase of the solution pH level resulted in the increase of nanowire conductance due to the reduction of the protons in the solution and vice versa with typical sensitivity around 10% to 20% only. Real time detection of clinically relevant protein streptavidin was demonstrated down to concentrations of 10pM. These results exhibited the promise of silicon nanowires as biosensor where nanowire's inherent DC characteristics were linear demonstrated general concept of nanowires just as simple constricted dimension resistors.

Chen et al. [15] An approach founded that which fabricated p-type silicon nanowires using size reduction method where silicon nanowires have height of 140nm, width of 100nm with triangular structure and a uniform doping concentration of $N_a=10^{17}$ cm^{-3}. Measured current voltage (I-V) characteristics exhibited typically non-linear diode like characteristics. According to provided I-V curves there were no conduction up to a drain bias of $V_{ds}<1V$. The conduction of nanowires were improved through the application of negative back gate bias thereby increasing the accumulation of holes and at $V_{backgate} = -20V$ the I-V characteristics showed linear behavior. It was noticeable that at small negative $V_{backgate}$ I-V characteristics were typically nonlinear. This was attributed to the fixed electronic charge located in the front oxide near the top silicon device layer surface and buried oxide near the bottom of silicon device layer due to reactive thermal oxidation of silicon surface. These nanowires were also successfully sensed pH level of the solution with sensitivity around 40mV/pH.

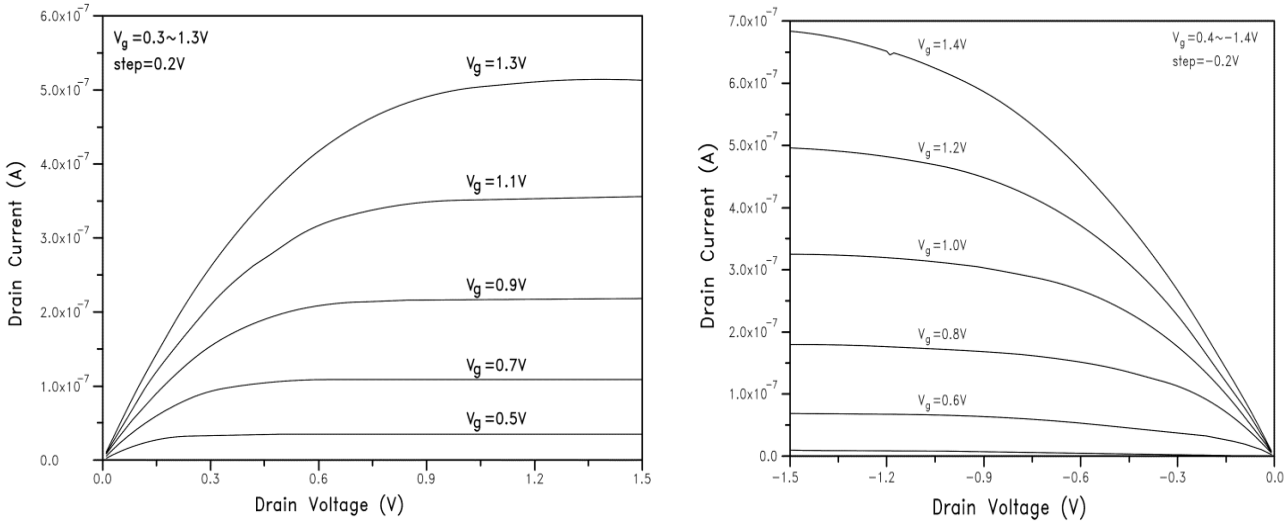

Figure 1.2: Measured output characteristics of junction less accumulation mode silicon nanowire transistors; a) drain current versus drain voltage for an n-type silicon nanowire and b) drain current versus drain voltage for different values for gate voltages for a p-type silicon nanowire. The width, W is 20nm and the gate length, L, is 1µm, such that W/L = 0.02(courtesy Jean-Pierre Colinge et al. [16].

Most recently, Jean-Pierre Colinge et al. [16] reported that Si-NW with a a few tens of nanometers wide, thickness of 20nm and uniform doping concentrations around $10^{19}cm^{-3}$, behave as transistor rather than simple resistor. Both p-type and n-type silicon nanowires were fabricated and measured characteristics showed that both n-type and p-type devices exhibited transistor action. These devices showed near ideal sub-threshold slope of 64mv dec^{-1} and quite decent output characteristics. Figure 1.2 and 1.3 shows that measured sub-threshold and output characteristics of such accumulation mode silicon nanowire transistors.

The aforementioned analysis shows that quit a variable electrical characteristic can be found in Si-NW that may depend on its dimension, interface states doping and contact issues. Conventional fabrication method of Si-NW usually employs 100nm SOI wafer ε-direct etch approach which actually is most straight forward approach of setting 100nm thick Si-NW. Suitability of such a NW while heavily doped is not yet investigated for sensor application.

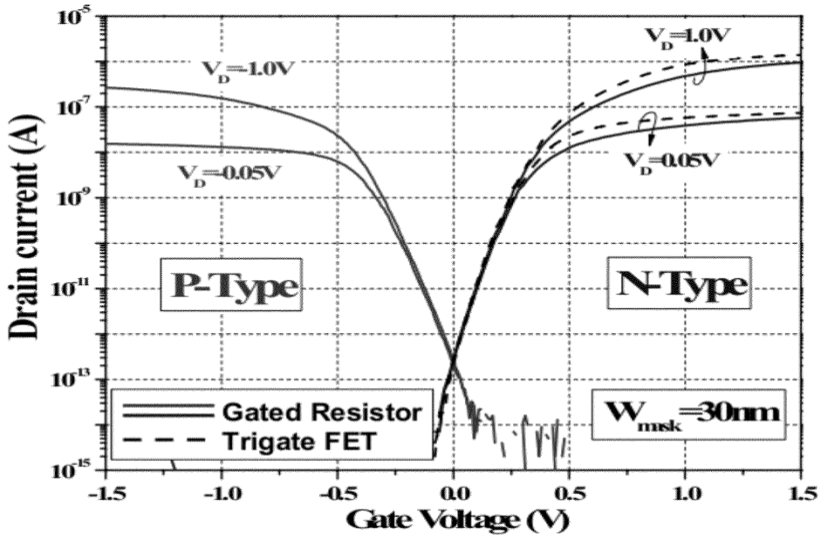

Figure 1.3: Measured sub-threshold characteristics of junction less accumulation mode silicon nanowire transistors. Drain current versus gate voltage for drain voltage of ±50mV and ±1 V for n-type and p-type silicon nanowires. The width of the nanowires is 30nm and the gate length, L, is 1µm (courtesy: Jean-Pierre Colinge et al. [15]).

1.2 Objective

In this work we first time perform a feasibility study of heavily doped Si-NW fabricated on conventional SOI platform for Biosensor application. Si-NWs are traditionally formed on SOI wafers using top down approaches and its buried Si layer could easily be used as an additional gate which may affect Si-NW's sensitivity as biosensor. In this work we perform a systematic study on the effect of backgate bias on the sensitivity of P-Type Si-NWs. A 100 nm thick, 1µm long P-Type Si-NW with a nominal doping of $10^{18}/cm^3$ has been investigated for different backgate biases and different drain bias polarities to gain insight into NW's sensitivity through backgate bias arrangements. Finally the possibilities of sensor application of such kinds of NWs are focused.

1.5 Thesis Organization

Chapter 1 provides the necessary background work on the electrical Characteristics of silicon nanowires. A number of research papers on Si-NW biosensor have also been surveyed to gain an understanding on the importance of this work.

Chapter 2 Describe device structures, simulation methodology and the required models for the simulation.

Chapter 3 Describe the simulation results for nanowire thickness of 100 nm with doping density 10^{-18} cm^{-3} for different backgate bias condition.

Finally, in chapter 4 and in chapter 5, the contribution of this work is summarized and discussed.

CHAPTER 2: METHODOLOGY

2.1 Device features and simulation models

The investigation on the sensitivity of Silicon nanowire for biosensor application were done with the help of numerical simulations using the SILVACO Atlas device simulator[17], installed on a VLSI lab of East West University. A p-type silicon nanowire with 100nm thickness was created on 100 nm oxide with a 500 nm buried Si layer. A secondary gate (backgate) is made with 20nm Al beneath the buried Si layer. The gate oxide thickness was 2nm and a heavily doped poly-silicon layer was used as top gate material. In the silicon nanowire, two heavily doped regions on the two sides of the channel were employed to ensure ohmic contacts on the source/drain regions. The gate doping was $10^{21}/cm^3$ and the source/drain regions were also heavily doped with the doping density of $10^{21}/cm^3$. The channel doping was $10^{18}/cm^3$. Here, the gate doping was n-type whereas the drain and the channel doping was p-type. To contact source to drain and gate, aluminum electrode was chosen.

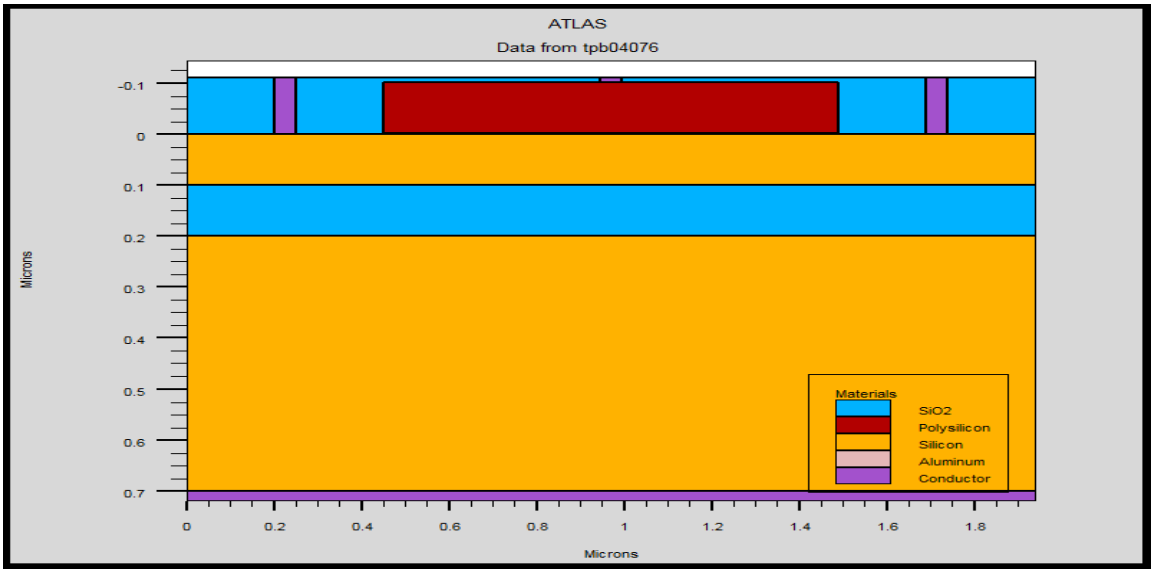

Figure. 2.1: Schematic of the simulated p-type silicon nanowire.

As Si-NW is 100nm thick quantum effect is neglected and a classical drift diffusion model is used to investigate Si-NW behavior. To accurately model carrier mobility in the constricted volume of NW Lombardi (CVT) model was used to take account temperature (T_L), perpendicular electric field ($E\perp$), parallel electric field ($E\parallel$) and doping concentration (N) effects [15]. In the CVT model, the transverse field, doping dependent and temperature dependent parts of the mobility are given by the three components that are combined using Mathiessen's rule. These components are surface mobility limited by scattering with acoustic phonons (μ_{AC}), the mobility limited by surface roughness (μ_{sr}) and the mobility limited by scattering with optical intervalley phonons (μ_b) are combined using Mathiessen's rule as follows[17]:

$$\mu_T^{-1} = \mu_{AC}^{-1} + \mu_b^{-1} + \mu_{sr}^{-1} \quad (2.1)$$

The first component, surface mobility limited by scattering with acoustic phonons equations [17]:

$$\mu_{AC.n} = \frac{BN.CVT}{E_\perp} + \frac{CN.CVT\ N^{\tau.CVT}}{T_L\ E_\perp^{1/3}} \quad (2.2)$$

$$\mu_{AC.p} = \frac{BN.CVT}{E_\perp} + \frac{CP.CVT\ N^{\tau P.CVT}}{T_L\ E_\perp^{1/3}} \quad (2.3)$$

The equation parameters BN.CVT, BP.CVT, CN.CVT, CP.CVT, TAUN.CVT, and TAUP.CVT used for this simulation are shown in Table 3-1 [18].

The second component, μ_{sr} is the surface roughness factor and is given by [17]:

$$\mu_{sr} = \frac{DELN.CVT}{E_\perp^2} \quad (2.4)$$

$$\mu_{sr} = \frac{DELP.CVT}{E_\perp^2} \quad (2.5)$$

The equation parameters DELN.CVT and DELP.CVT used for this simulation are shown in Table 3.1[17].

The third mobility component, the mobility limited by scattering with optical intervalley phonons is given by [17]:

$$\mu_{b,n} = MU0N.CVT exp\left(\frac{-PCN.CVT}{N}\right) + \frac{\left[MUMAXN.CVT\left(\frac{T_L}{300}\right)^{-GAMN.CVT} - MU0N.CVT\right]}{1+\left(\frac{N}{CRN.CVT}\right)^{ALPHN.CVT}} - \frac{MU1N.CVT}{1+\left(\frac{CSN.CVT}{N}\right)^{BETAN.CVT}} \quad (2.6)$$

$$\mu_{b,p} = MU0P.CVT exp\left(\frac{-PCP.CVT}{N}\right) + \frac{\left[MUMAXP.CVT\left(\frac{T_L}{300}\right)^{-GAMP.CVT} - MU0P.CVT\right]}{1+\left(\frac{N}{CRP.CVT}\right)^{ALPHP.CVT}} - \frac{MU1P.CVT}{1+\left(\frac{CSP.CVT}{N}\right)^{BETAP.CVT}} \quad (2.7)$$

Table 2.1: Parameters for Equations 2.1 to 2.7

Statement	Parameter	Default	Units
MOBILITY	BN.CVT	4.75×10^{7}	cm/(a)
MOBILITY	BP.CVT	9.925×10^{4}	cm/(a)
MOBILITY	CN.CVT	1.74×10^{5}	
MOBILITY	CP.CVT	8.842×10^{5}	
MOBILITY	TAUN.CVT	0.125	
MOBILITY	TAUP.CVT	0.0317	
MOBILITY	GAMN.CVT	2.5	
MOBILITY	GAMP.CVT	2.2	
MOBILITY	MU0N.CVT	52.2	$cm^2/(v\text{-}a)$
MOBILITY	MU0P.CVT	44.9	$cm^2/(v\text{-}a)$
MOBILITY	MU1N.CVT	43.4	$cm^2/(v\text{-}a)$
MOBILITY	MU1P.CVT	29.0	$cm^2/(v\text{-}a)$
MOBILITY	MUMAXN.CVT	1417.0	$cm^2/(v\text{-}a)$
MOBILITY	MUMAXP.CVT	470.5	$cm^2/(v\text{-}a)$
MOBILITY	CRN.CVT	9.68×10^{14}	cm^{-3}
MOBILITY	CRP.CVT	2.23×10^{17}	cm^{-3}
MOBILITY	CSN.CVT	3.43×10^{20}	cm^{-3}
MOBILITY	CSP.CVT	6.10×10^{20}	cm^{-3}
MOBILITY	ALPHN.CVT	0.680	
MOBILITY	ALPHP.CVT	0.71	
MOBILITY	BETAN.CVT	2.00	
MOBILITY	BETAP.CVT	2.00	
MOBILITY	PCN.CVT	0.0	cm^{-3}
MOBILITY	PCP.CVT	0.23×10^{16}	cm^{-3}
MOBILITY	DELN.CVT	5.82×10^{14}	v/s

The model for carrier emission and absorption processes proposed by Shockley-Read-Hall (SRH) is used to reflect the recombination phenomenon within the device. The electron and hole lifetimes $\tau_{n \text{ and }} \tau_p$ were modeled as concentration dependent. The equation is given by [17]:

$$R_{SRH} = \frac{pn - n_{ie}^2}{\tau_p\left[n + n_{ie}\exp\left(\frac{ETRAP}{kT_L}\right)\right] + \tau_n\left[p + n_{ie}exp\left(\frac{-ETRAP}{kT_L}\right)\right]} \quad (2.8)$$

$$\tau_n = \frac{TAUNO}{1 + \frac{N}{(NSRHN)}} \quad (2.9)$$

$$\tau_p = \frac{TAUPO}{1 + \frac{N}{(NSRHP)}} \quad (2.10)$$

Here N is called the local (total) impurity concentration. The used parameters TAUN0, TAUP0, NSRHN and NSRHP are Table 3-2[17]. This model was activated with the CONSRH parameter of the MODELS statement.

Table 2.2: Default Parameters for Equations 2.8 to 2.10

Statement	Parameter	Default	Units
METERIAL	TAUNO	1.0×10^{-7}	S
METERIAL	NSRHN	5.0×10^{16}	cm^{-3}
METERIAL	TAUPO	1.0×10^{-7}	S
METERIAL	NSRHP	5.0×10^{16}	cm^{-3}

To account bandgap narrowing effects, BGN model was used. These effects may be described by an analytic expression relating the variation in bandgap, ΔE_g, to the doping concentration, N. The expression used in ATLAS is from Slotboom and de Graaf [17]:

The used values for the parameters BGN.E, BGN.N and BGN.C are shown in Table 2.3[17].

Table 2.3: Default parameters of Slotboom's Bandgap Narrowing Model foe equation 2.11

Statement	Parameter	Default	Units
METERIAL	BGN.E	9.0×10^{16}	V
METERIAL	BGN.N	1.0×10^{16}	cm^{-3}
METERIAL	BGN.C	0.5	-

2.2 Simulation profile

Device simulation using silvaco atlas usually faces convergence problems and necessitates a long run times. To avoid these problems, the simulation of silicon nanowire MOSFET has been divided into a few groups. At first, structure definition was performed. In this definition the simulation focused on creating the structure with a suitable mesh density. Regions and electrodes were defined as depicted in figure 2.2. Finer nodes were assigned in critical areas, such as across the gate oxide for an accurate 10nm thickness to monitor channel activity and to get a better picture of the depletion layer and junction behavior near the source/drain boundaries. A coarser mesh was used elsewhere in order to reduce simulation run time.

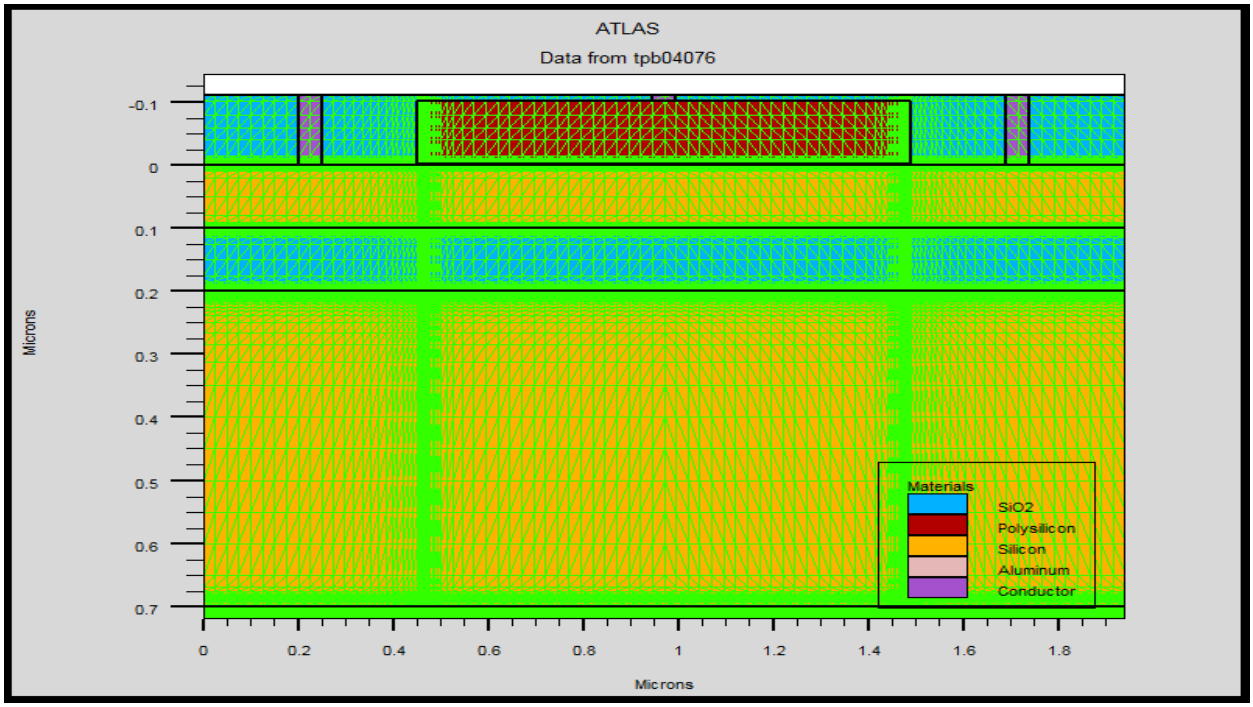

Figure. 2.2: Cross-sectional view of p-type nanowire showing the mesh density used in this simulation.

Once the structure and the mesh were found to be as desired, the simulation was performed with appropriate models as discussed in section 2.1 and numerical solving methods. The model was invoked by using the statements FERMI, CVT, CONSRH, BGN. The numerical solving methods GUMMEL, NEWTON were used to reduce the simulation run time, while keeping the accuracy of the simulation at an acceptable level.

CHAPTER 3: RESULTS

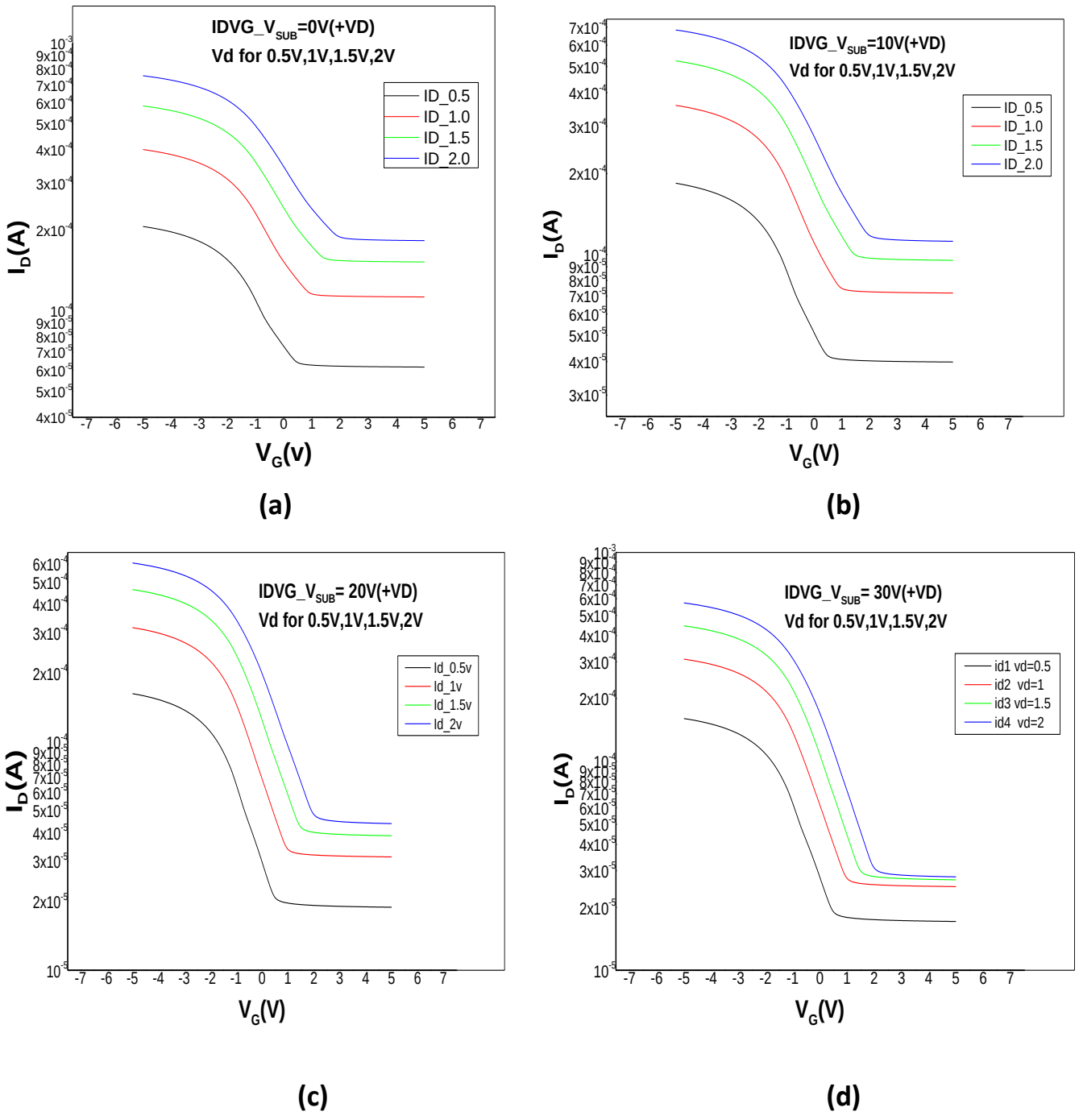

Figure 3.1: Transfer characteristics (I_D vs V_G) of Si-NW when V_D is positive and V_G is swiped from +5V to -5V for (a) $V_{backgate}$ = 0V, (b) $V_{backgate}$ = +10V (c) $V_{backgate}$ = +20V (d) $V_{backgate}$ = +30V.

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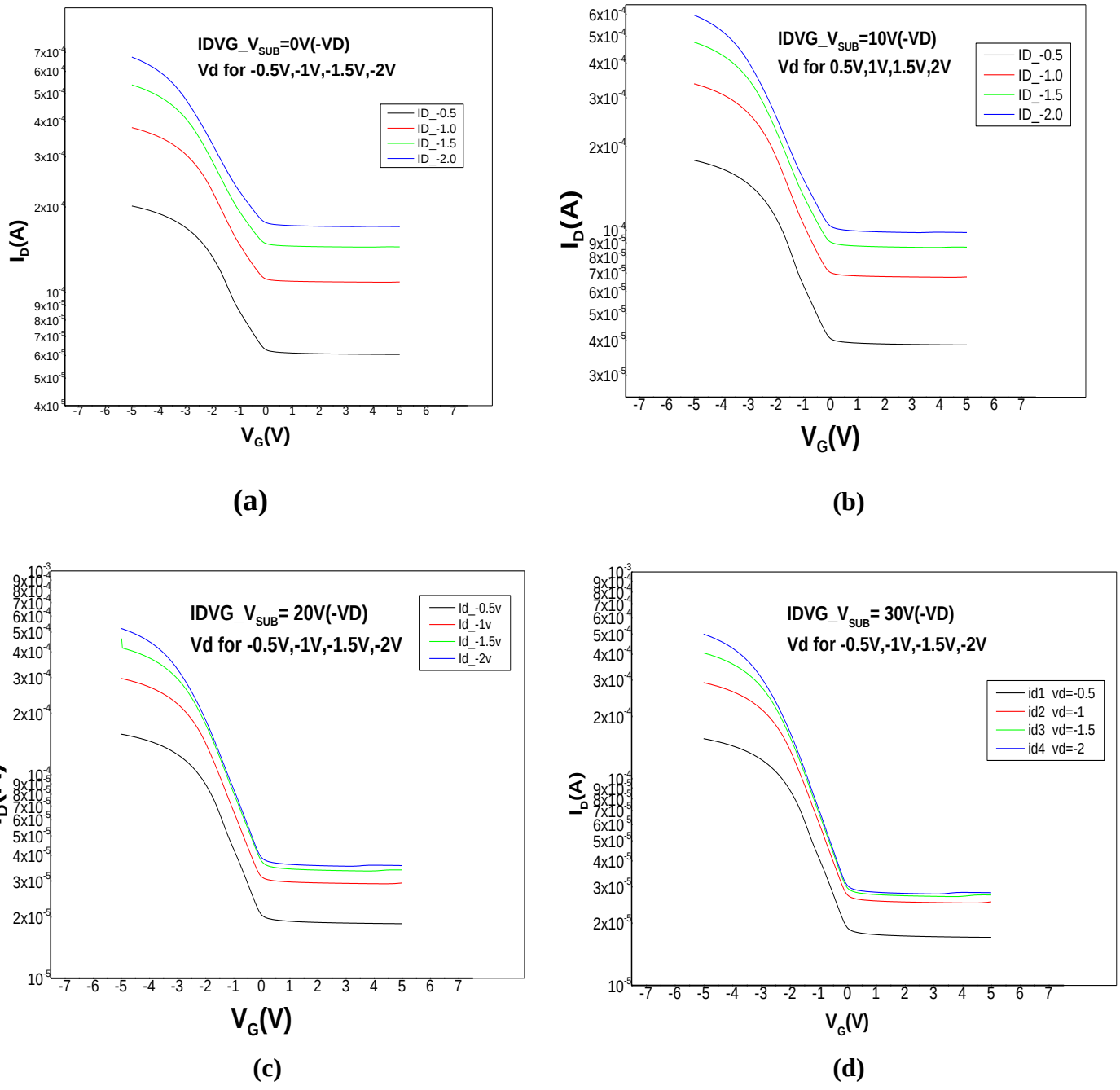

Figure 3.2: Transfer characteristics (I_D vs V_G) of Si-NW when V_D is negative and V_G is swiped from +5V to -5V for (a) $V_{backgate}$ = 0V, (b) $V_{backgate}$ = +10V (c) $V_{backgate}$ = +20V (d) $V_{backgate}$ = +30V.

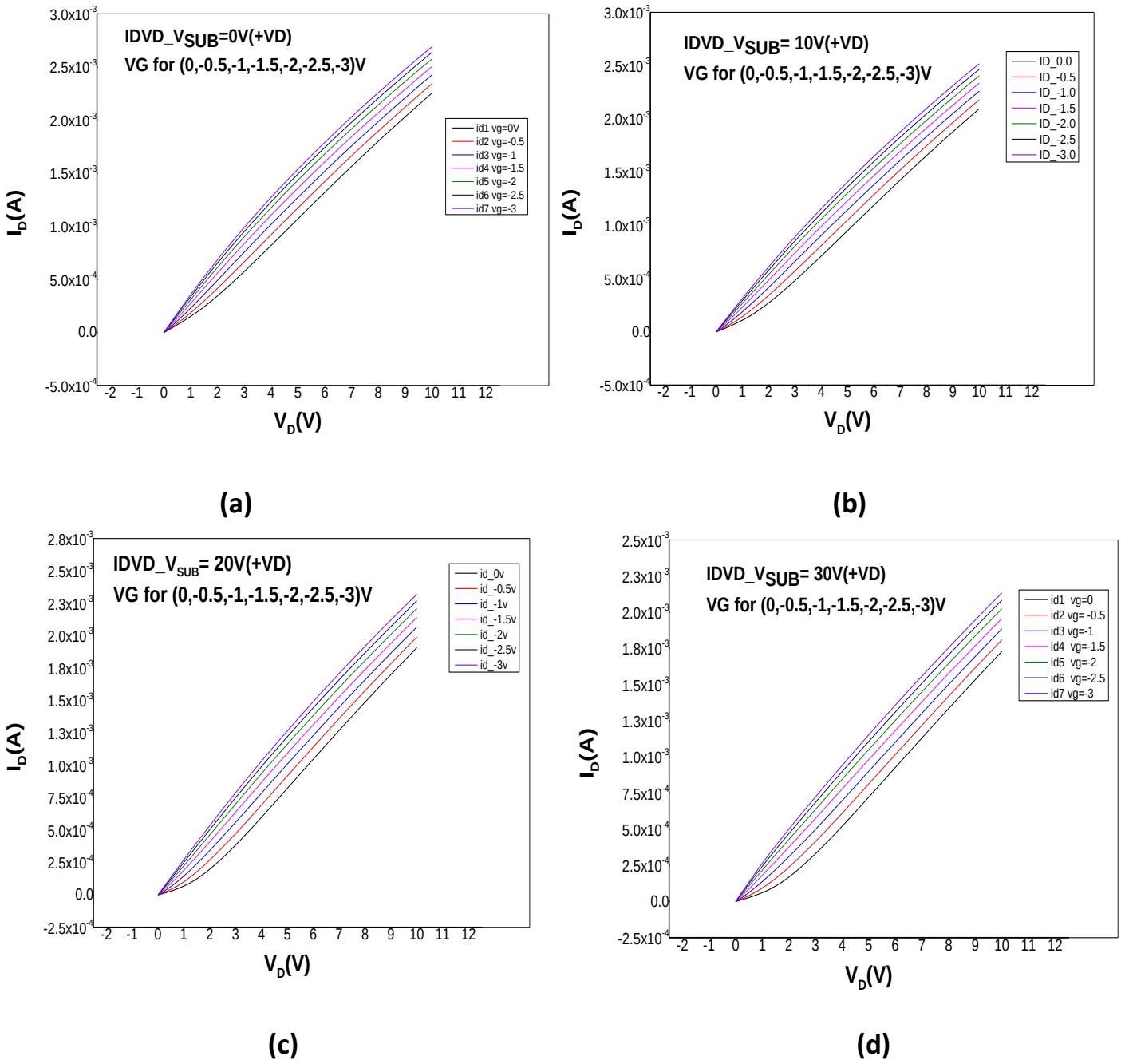

Figure 3.3: Output characteristics (I_D vs V_D) of Si-NW when V_D is positive and V_D is swiped from 0V to +10V for (a) $V_{backgate}$ = 0V, (b) $V_{backgate}$ = +10V (c) $V_{backgate}$ = +20V (d) $V_{backgate}$ = +30V.

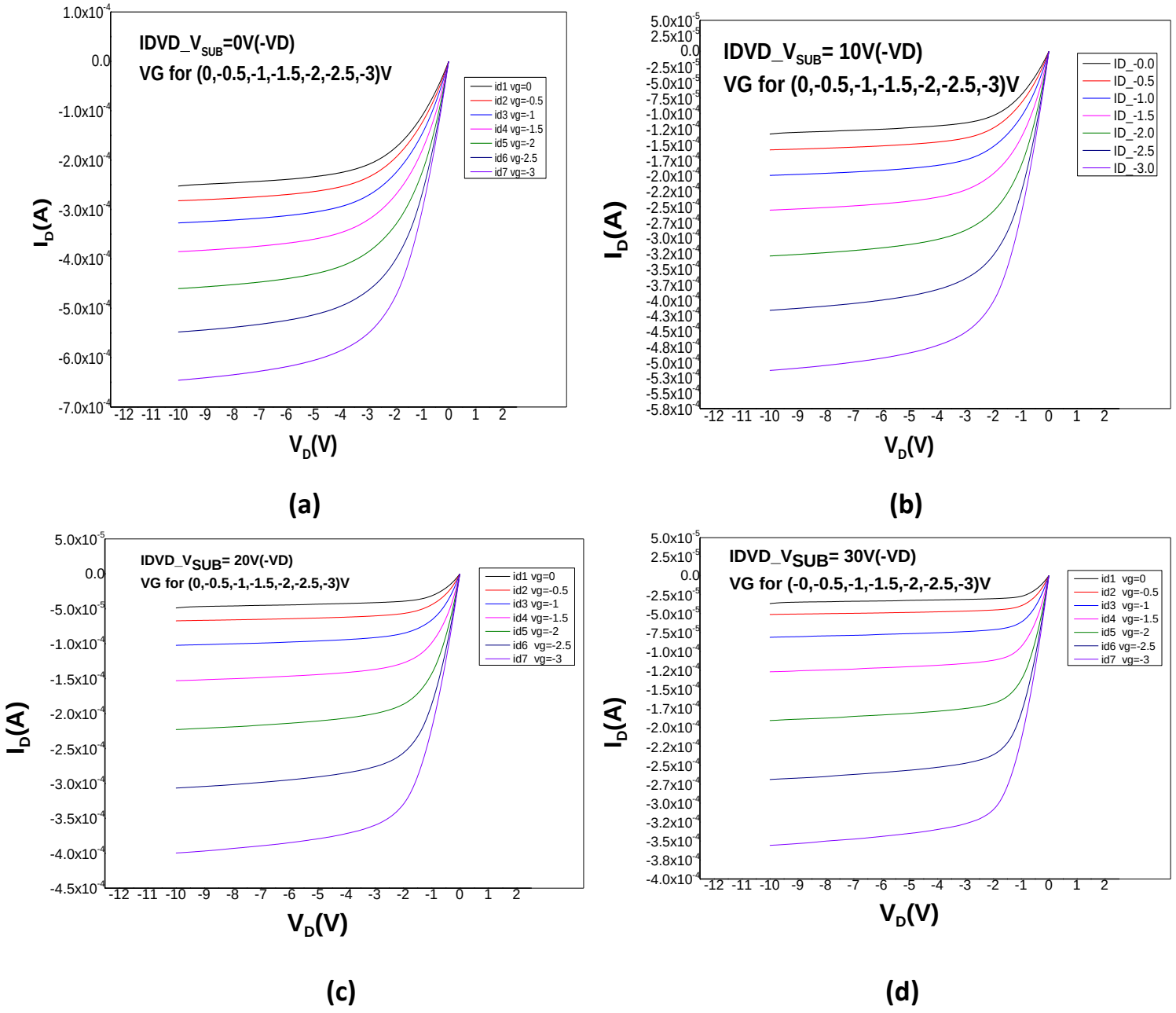

Figure 3.4: Output characteristics (I_D vs V_D) of Si-NW when V_D is negative and V_D is swiped from 0V to -10V for (a) $V_{backgate}$ = 0V, (b) $V_{backgate}$ = +10V (c) $V_{backgate}$ = +20V (d) $V_{backgate}$ = +30V.

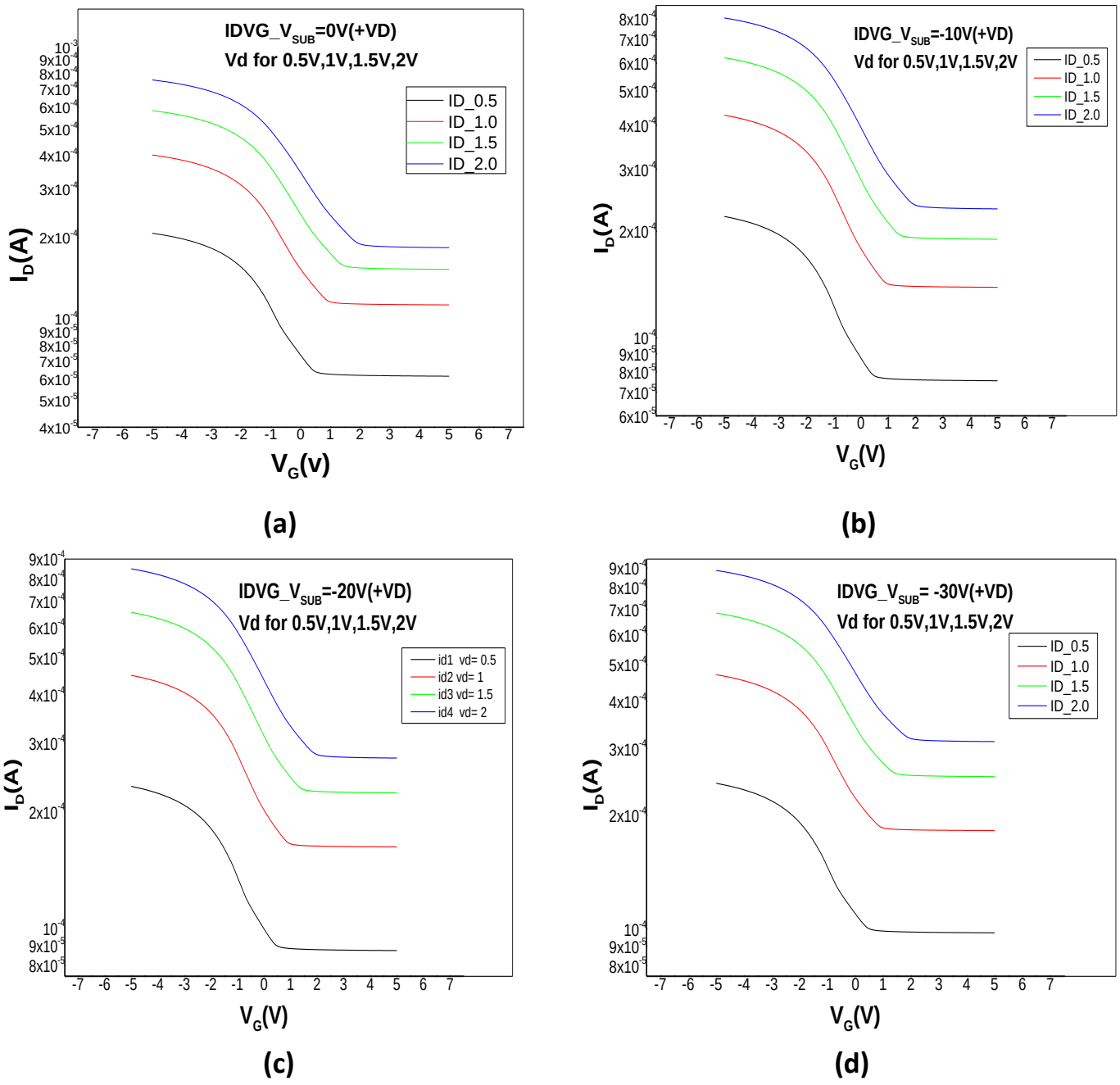

Figure 3.5: Transfer characteristics (I_D vs V_G) of Si-NW when V_D is positive and V_G is swiped from +5V to -5V for (a) $V_{backgate}$ = 0V, (b) $V_{backgate}$ = -10V (c) $V_{backgate}$ = -20V (d) $V_{backgate}$ = -30V

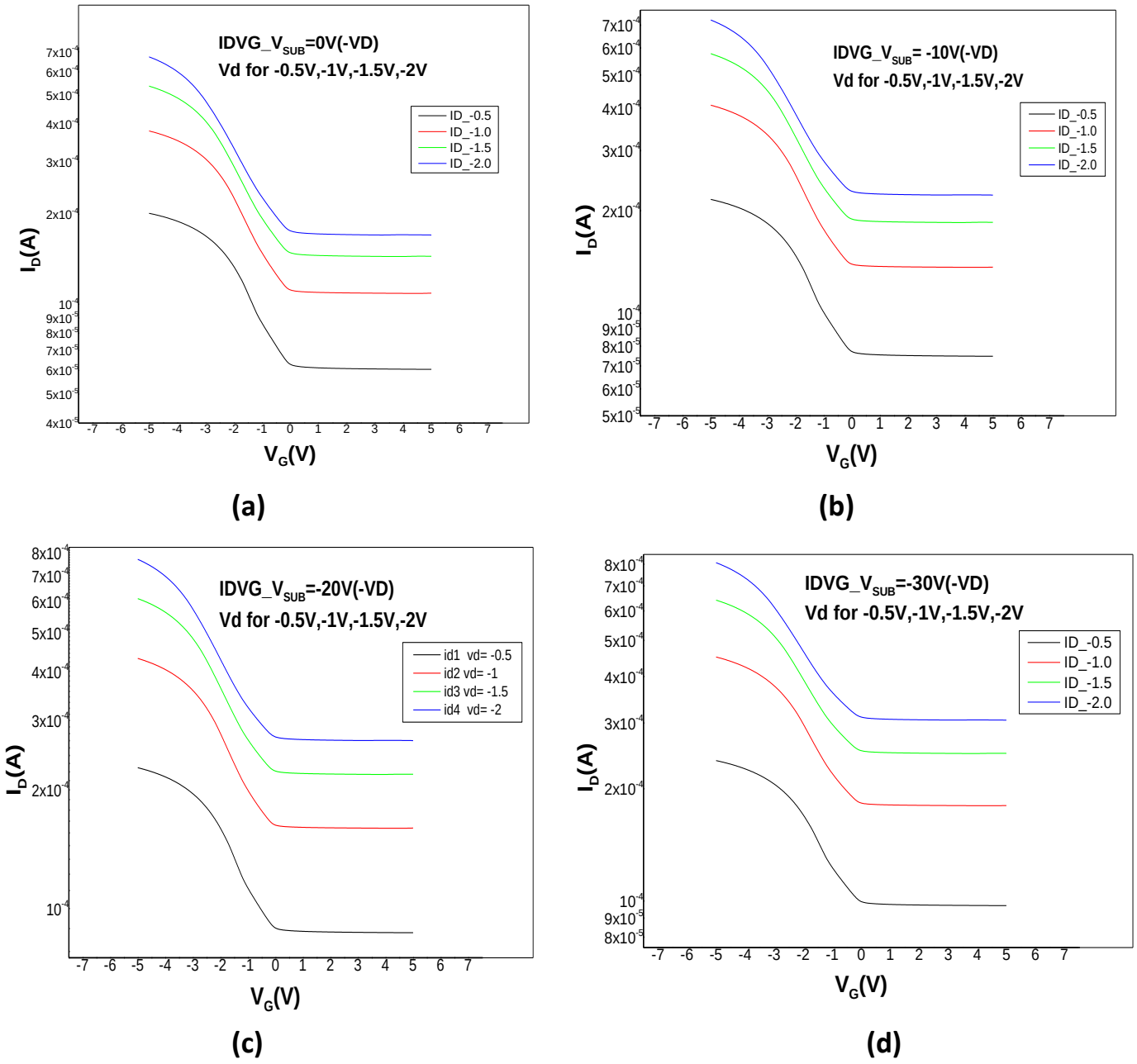

Figure 3.6: Transfer characteristics (I_D vs V_G) of Si-NW when V_D is negative and V_G is swiped from +5V to -5V for (a) $V_{backgate}$ = 0V, (b) $V_{backgate}$ = -10V (c) $V_{backgate}$ = -20V (d) $V_{backgate}$ = -30V.

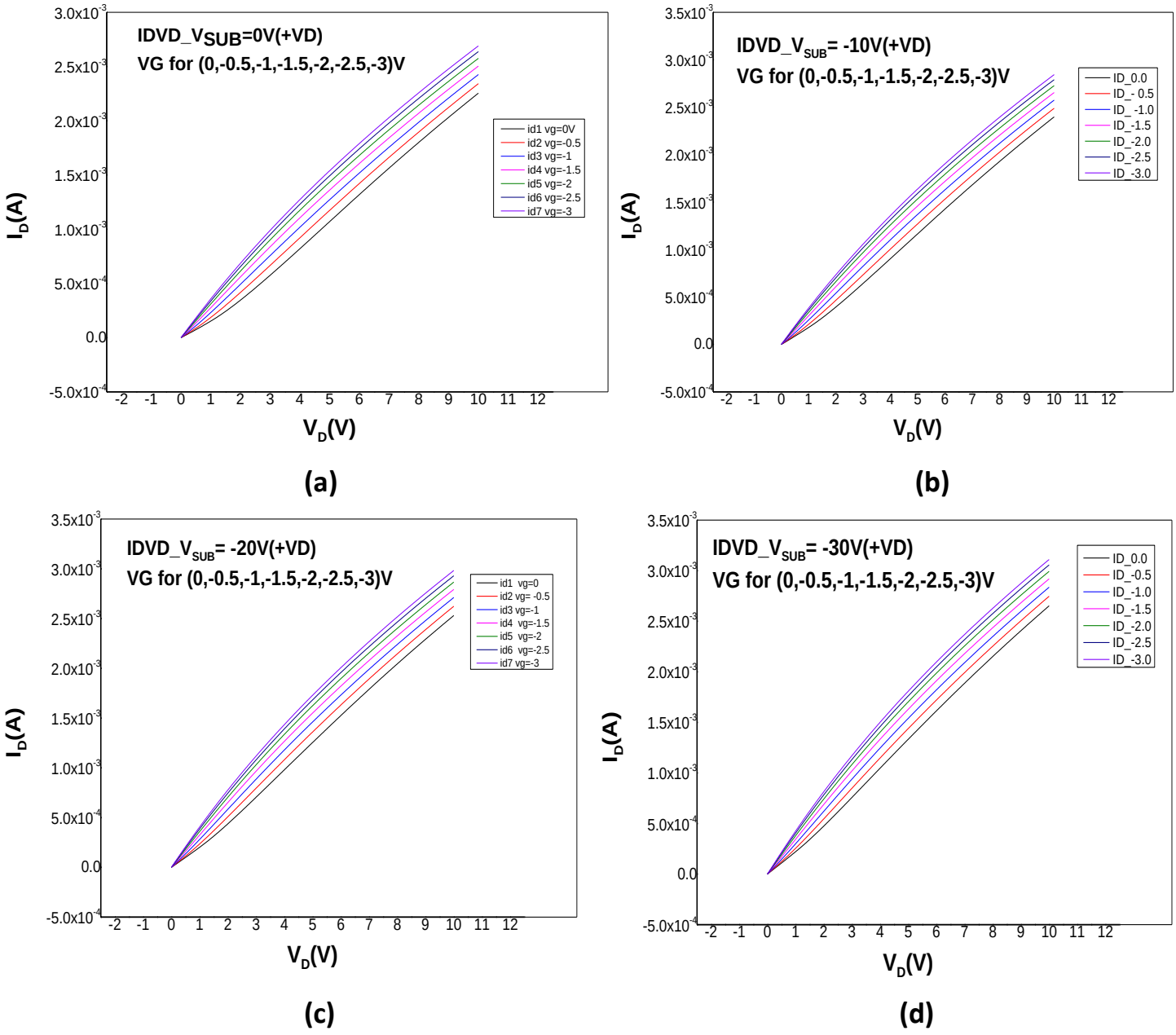

Figure 3.7: Output characteristics (I_D vs V_D) of Si-NW when V_D is positive and V_D is swiped from 0V to +10V for (a) $V_{backgate}$ = 0V, (b) $V_{backgate}$ = -10V (c) $V_{backgate}$ = -20V (d) $V_{backgate}$ = -30V.

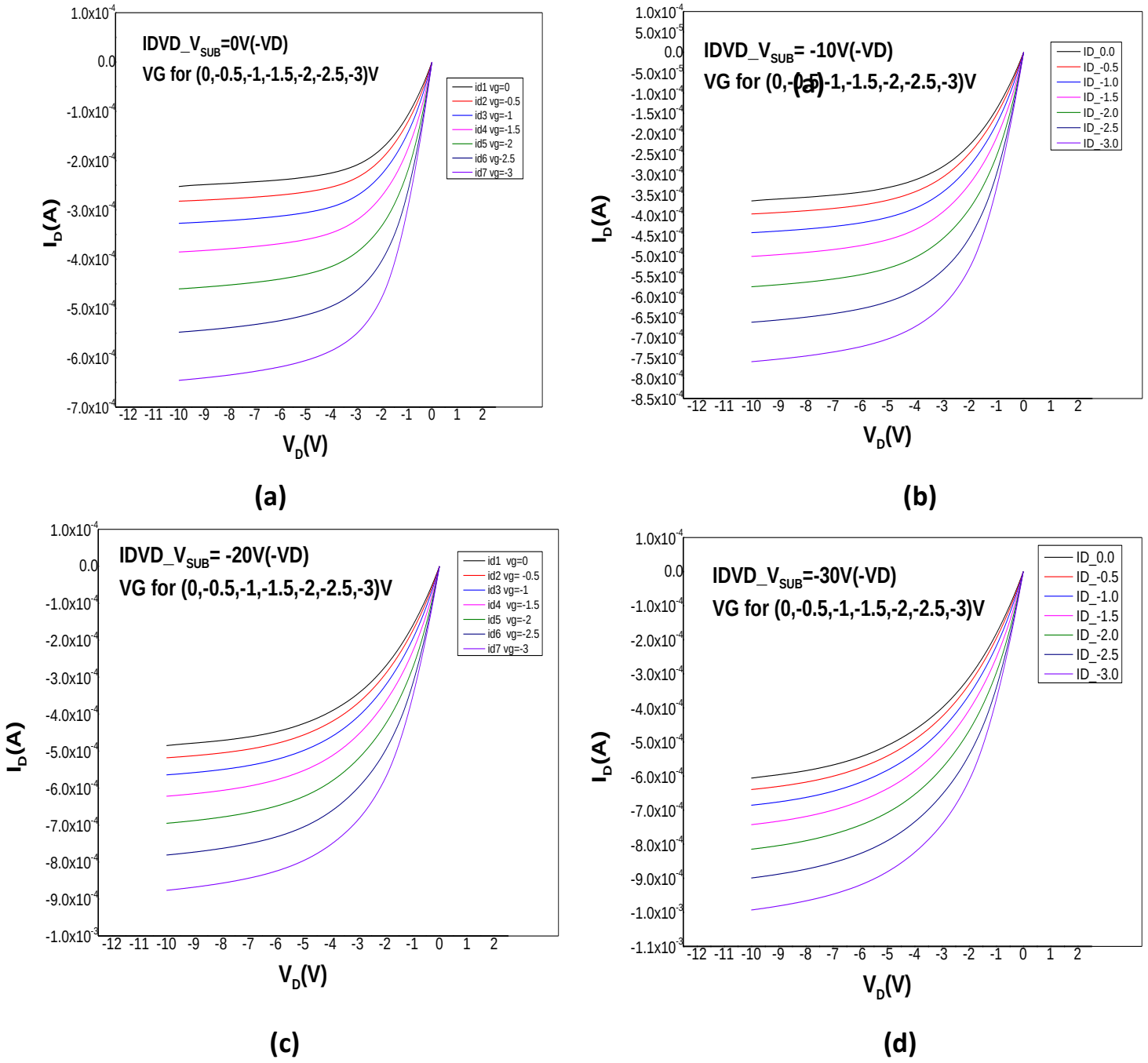

Figure 3.8: Output characteristics (I_D vs V_D) of Si-NW when V_D is negative and V_D is swiped from 0V to -10V for (a) $V_{backgate}$ = 0V, (b) $V_{backgate}$ = -10V (c) $V_{backgate}$ = -20V (d) $V_{backgate}$ = -30V.

Figure 3.1(a to d) shows transfer characteristics (I_D vs V_G) of Si-NW when V_D is positive and V_G is swiped from +5V to -5V and for different values of backgate bias. The nanowire have thickness of 100 nm, doping concentration of 10^{18} cm^{-3} and channel length of 1µm. For backgate bias of 0V in fig 3.1(a), it is found that a sub-threshold slope is 6311.31 6 mV/dec and DIBL is about 1800 mV/V. For backgate bias of 10V found that sub-threshold slope is 4884.88 mV/dec and DIBL is 1550 mV/V, which is slightly better than 0V backgate bias. For backgate bias of 20V (Fig 3.1(c)) and 30V sub-threshold slopes are 3188.95mV/dec and 2772mV/dec where as DIBL are 1300mV/V and 1100mV/V respectively. These results show that with increasing value of positive backgate bias device characteristics are slightly improving.

Figure 3.2(a to d) shows transfer characteristics (I_D vs V_G) of Si-NW when V_D is negative and V_G is swiped from +5V to -5V and for different values of backgate bias. For backgate bias of 0V in fig 3.2(a), it is found a sub-threshold slope of 5837.4 mV/dec and DIBL is about 700 mV/V. For backgate bias 10V sub-threshold is 4731.57 mV/dec and DIBL is 450 mV/V, for backgate bias 20V sub-threshold slope is 2898.66 mV/dec and DIBL is 100 mV/V and for back gate bias 30V sub-threshold slope is 2790.56 mV/dec and DIBL is 100 mV/V. These results show that for negative V_D application device characteristics are superior to that of the positive V_D applications.

Figure 3.3(a to d) shows output characteristics (I_D vs V_D) of Si-NW when V_D is positive and V_G is swiped from 0V to -3V for various backgate bias. The nanowire have thickness of 100 nm, doping concentration of $10^{18}cm^{-3}$ and channel length of 1µm. For backgate of 0V (fig 3.3(a)) it is found that I_D vs V_D characteristics are slightly nonlinear when V_G=0V there is no significant conduction up to certain level of drain bias with increasing negative gate voltage characteristics become more linear and conduction is found to increase. For back gate voltage 10V, 20V and 30V overall characteristics remains same, but current I_D is decreasing for a certain drain voltage while backgate is increasing.

Figure 3.4 (a to d) output characteristics (I_D vs V_D) of Si-NW when V_D is negative and V_G is swiped from 0V to -3V for various backgate voltage. The nanowire have thickness of 100 nm, doping concentration of $10^{18}cm^{-3}$ and channel length of 1µm. For negative V_D application I_D-V_D characteristics exhibit transistor like behaviour and with increasing backgate bias drive current is found to decrease.

Figure 3.5 (a to d) shows transfer characteristics (I_D vs V_G) of Si-NW when V_D is positive and V_G is swiped from +5V to -5V for various backgate voltage. For backgate bias of 0V in fig 3.5(a), it is found a sub-threshold slope of 6311.31 6 mV/dec and DIBL is about 1800 mV/V. For backgate bias -10V sub-threshold slope is 6917.30 mV/dec and DIBL is 1950 mV/V, for backgate bias -20V sub-threshold slope is 7108.60 mV/dec and DIBL is 2100 mV/V, and for backgate bias -30V sub-threshold slope is 9553.25 mV/dec and DIBL is 2250 mV/V. The results show that for negative backgate bias the sub-threshold characteristics of device gradually decrease.

Figure 3.6 (a to d) transfer characteristics (I_D vs V_G) of Si-NW when V_D is negative and V_G is swiped from +5V to -5V for various backgate bias. For backgate bias of 0V in fig 3.6(a), it is found a sub-threshold slope of 5837.4 mV/dec and DIBL is about 700 mV/V. For backgate bias -10V sub-threshold slope is 6534.2 mV/dec and DIBL is 900 mV/V, for backgate bias -20V sub-threshold slope is 8304.77 mV/dec and DIBL is 1050 mV/V, and for backgate bias -30V sub-threshold slope is 7989.60 mV/dec and DIBL is 1200 mV/V. Negative backgate bias with positive drain voltage shows higher DIBL and sub-threshold slop than negative backgate bias with negative drain voltage. The results again show that with negative backgate biases device characteristics decrease gradually even for negative V_D applications. However device characteristic remains superior to that of positive V_D applications.

In figure 3.7 (a to d) and figure 3.8 (a to d) shows the output characteristics (I_D vs V_D) of Si-NW when backgate bias is negative and for both positive and negative V_D applications. The device characteristics remain superior to that of positive backgate bias applications and overall trend is similar that of the 3.3 and 3.4.

The aforementioned analysis of 100nm thick and 1µm long p-type Si-NW electrical characteristics of body doping of $10^{18}/cm^3$ shows that sub-threshold characteristic for positive V_D application varies from 2772mV/dec to 9553.25mV/dec while backgate bias is varied from +30V to -30V. DIBL also varies from 1100mV/V to 2250mV/V while backgate bias is varied from +30 to -30V. For negative V_D applications sub-threshold slops varies from 2790mV/dec to 7989mV/dec while backgate bias is varied from +30V to -30V. DIBL is these conditions are found to vary from 100mV/V to 1200mv\V/V. These result show that at $10^{18}/cm^3$ doping 100nm thick conventional SOI platform built 1µm long NW will not exhibit good season behaviour for both negative and positive V_D applications. However, for negative V_D application device exhibit slightly better sub-threshold characteristics in caparison to positive V_D value where as significant improvement is found in DIBL characteristics upon negative V_D applications. These results imply that negative V_D application although provides better sensor operation for 100nm thick NWs at $10^{18}/cm^3$ doping, application of backgate bias upto +30V fails to significantly change sub-threshold characteristics of the device and hence, at this body doping 100nm thick NWs is not suitable for good sensor operations.

CHAPTER 4: DISCUSSION & CONCLUSION

We investigated feasibility of applying 100nm thick and 1μm long p-type Si NW with a body doping of $10^{18}/cm^3$ for sensor applications. It is found that such a p-type Si NW exhibits a subthreshold slope of 2772mV/dec to 9553.25mV/dec for backgate bias of 30V to -30V while applied V_D was positive. For negative V_D applications subthreshold slope vary from 2790mV/dec to 7989mV/dec when backgate bias is changed from 30V to -30V. Such a subthreshold slope is not promising sensor applications even though significant depletion is tried to be formed by 30V of backgate bias applications. Therefore, it may be concluded that 100nm thick SOI platform based Si NWs will not be suitable for sensor application at $10^{18}/cm^3$ body doping.

CHAPTER: 5 FUTURE WORKS

This research only shows the possibility of applying 100nm thick Si NW for sensor application using relatively heavy doping of $10^{18}/cm^3$ with the aim to reduce ambient noise. It is clear that 100nm thick NW at this body doping is not at all suitable for sensor application. A rigorous study is needed with varying Si thickness to find out optimum thickness at $10^{18}/cm^3$ doping for sensor applications.

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