EAST WEST UNIVERSITY

Numerical Analysis of a Si based Gate All Around Metal Semiconductor Field Effect Transistor

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In the Name of Allah, the Most Beneficent, the Most Merciful

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ABSTRACT

With the advent in time, as the Moore's law approaches horizon; novel semiconductor devices such as the Gate All Around Metal Semiconductor Field Effect Transistor (GAA-MESFET) transistor arrives at the stage as the next big thing in the world of electronics. This is because as the dimensions planar MOSFET shrinks to an even smaller scale, the increase in SCE(Short Channel Effect) becomes even more prominent thus degrading the device's performance. Thus the need of the hour is an transistor that can provide better control over SCE and GAA-MESFET can be just that ray of hope. It has become an extremely promising candidate in the sub 22 nm scale nano-devices due to its simpler fabrication process and remarkable short channel performances. In this undergraduate thesis, investigation of the behaviour of such GAA-MESFET by changing various physical parameters while trying to infer about its potential behaviour aka performance has been done. Use of High-K dielectric material alongside a stack of Low K and High k material as insulator was also done and its corresponding performance was observed.

Authorization

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Chapter 1

INTRODUCTION

1.1 Background:

It all begin with the perception of Lilienfeld of Insulated Gate Field Effect Transistor in 1925 which bore the potential to replace the vacuum tube technology with small sized semiconductor transistor technology [1]. The first transistor was presented at the Bell laboratories by William Shockley, John Bardeen and Walter Battain in December 1947. Since then, and in particular over the last 40 years, the semiconductor technology has developed with an amazing speed. The integrated circuit performance has grown exponentially with the scaling of the MOSFET (Metal oxide-semiconductor field effect transistor) dimensions as the primary driver. In high performance logic MOSFETs with 14nm physical gate lengths are now in production [2]. In 1958, Jack Kilby at Texes Instruments conceived the idea of the Integrated Circuits (IC) and Robert Noyce from the Fairchild Corp. fabricated the first IC (a S-R flip flop). It then came in 1959 when Richard Feynman delivered his notable speech, “There is plenty of room at the bottom”, acknowledging the high performance achievement of the materials at the reduced dimensions. The first practical demonstration took place in 1960 by Kahng and Atilla in the form of the Silicon based Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Another visionary prophecy from Gordon Moore, then with Fairchild Corp. and co-founder of Intel, states that, “The number of transistors on integrated circuits doubles approximately every two years”. The year 1962 saw the growth of the first logic family, the TTL. Intel introduced the first microprocessor in 1972 which used more than 2000 PMOS transistors.

Following the Moore’s law, the transistor count increased exponentially. Then next few microprocessors used the NMOS technology which was routed out soon due to heavy dynamic power consumption with the increased number of transistor per chip. Today's monolithic Integrated Circuits (ICs) use the MOSFET as a basic switching element for digital logic applications and as an amplifier for analog applications. This has resulted in chips that are significantly faster and have greater complexity in every generation while continually bringing down the cost per transistor [1].

1.2 Device Scaling – Moore's Law

Moore's Law describes an important trend in the history of computer hardware. It says that the number of transistor that can be inexpensively placed on an integrated circuit is increasing exponentially with time, doubling approximately every two years.

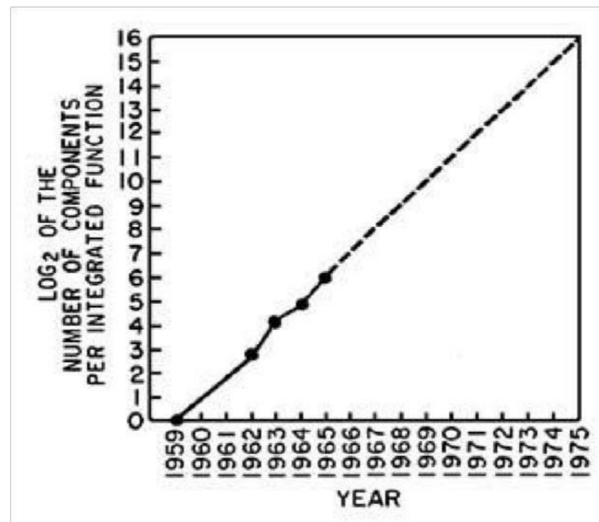


Figure 1.1: Invention of Moore's Law

In 1965, the observation was first made by Intel cofounder Gordon E. Moore. The trend has continued up till 2004. Almost every measure of the capabilities of digital electronic devices s linked to Moore's Law for example processing speed and memory capacity. All of these are improving at roughly exponential rates as well. This has dramatically increased the usefulness of digital electronics in nearly every segment of the world economy. Moore's Law describes this as a driving force of technological and social change in the late 20th and early 21^{st}century [2].

In 2015 Gordon Moore himself forecast that the rate of development would slow - "I see Moore's law dying here in the next decade or so." [3]. Though Moore's Law had said every two years, this rapid increase in technological production has lessened the period in the minds of technicians and users alike. The limitation which exists is that once transistors can be created as small as atomic particles, then there will be no more room for growth in the CPU market where speeds are concerned [4].

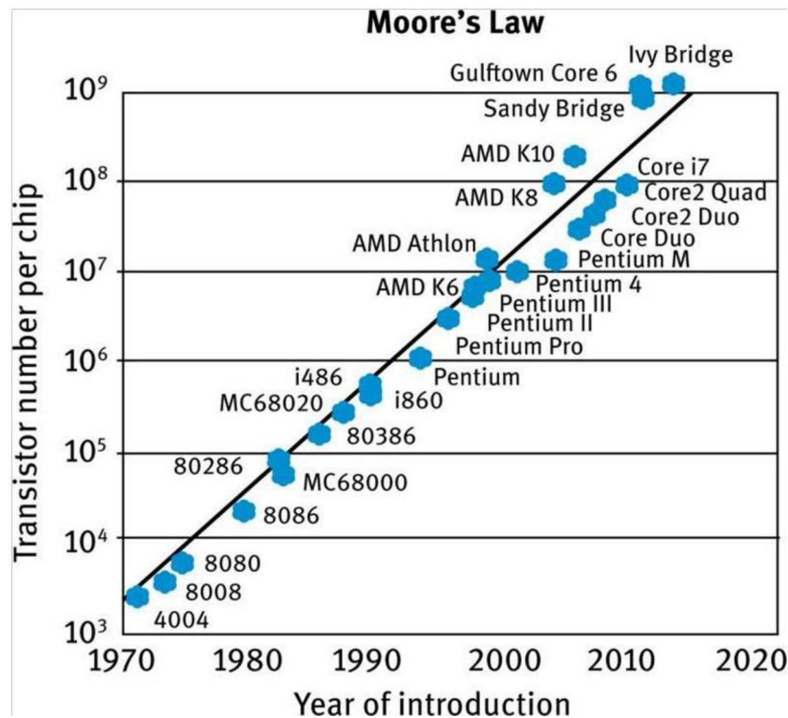


Figure 1.2: Moore's Law Curve

The search is now on for new technologies that will enable to continue increase the performance of electronics beyond Moore's Law. These technologies are known as More Moore and More than Moore.

- More Moore
- More than Moore

1.2.1 More Moore

With the size of CMOS transistors approaching the atomic dimension level, the 'More Moore', which implies the aggressive continuous downscaling, has encountered numerous difficulties [5]. The International Technology Roadmap for Semiconductors (ITRS) is a set of documents produced by a group of semiconductor industry experts. These experts are representative of the sponsoring organizations which include the Semiconductor Industry Associations of the United States, Europe, Japan, South Korea and Taiwan. The main goal of the ITRS include identifying key technical requirements and challenges critical to sustain the historical scaling of CMOS technology More Moore (MM) and stimulating the needed research and development to meet the

key challenges. The potential solutions in the ITRS are meant to simulate but not limit research exploring novel and different approaches. MM mission is listed below:
MM focus team in ITRS provides physical, electrical and reliability requirements for logic and memory technologies to sustain More Moore scaling for big data, mobility and cloud applications and forecast logic and memory technologies in main-stream/high-volume manufacturing [6].

1.2.2 More than Moore:

Researchers have realized that the value of a system does not only depend on the performance of the CMOS technology for the digital information processing but also on the functional diversification of semiconductor-based devices. Consequently, the term 'More than Moore' has been introduced to emphasize the trend of increasing the diversity of microelectronic chips for additional value. Integrated nano-photonics could offer promising, practical, and profound solutions to several aspects of 'More than Moore' such as radio-frequency signal processing and biochemical sensing due to unique advantages in processing analog signals. More importantly, integrated nano-photonic devices could be fabricated on semiconductor-based chips to build photonic integrated circuits (PICs), which could offer low-cost, high-reliability, and portable solutions to a variety of applications. In this dissertation, the design, fabrication, and characterization of various integrated nano-photonic devices will be presented to illustrate how integrated nano-photonics facilitates the development of 'More than Moore' [5]. More than Moore is a functional diversification incorporating functionalities that are more than digital and analog signals and architectures used in conventional semiconductors. More than Moore product definitions include MEMS, which integrate microelectronics with micromechanical structures that are scaled versions of larger mechanical structures via semiconductor processing techniques, as well as 3D packaging, LEDs, and Photovoltaic cells depending on the source. In the future there are NEMS, or Nano-Electrical-Mechanical-Systems. In all cases the use of manufacturing methods and metrology evolved from semiconductors [7].

1.3 Limitation of MOSFET

Introducing a new technology node is the reduction of circuit size. By making the transistors and the interconnection smaller, more circuits can be fabricated on each silicon wafer and therefore each circuit becomes cheaper.

For this reason, we have to place so many MOSFETs in a small area, which creates some problem in MOSFET and default in device. This limitation of MOSSFETs are,

- Sub-threshold Swing
- Short Channel Effect
- Gate Insulator Thickness

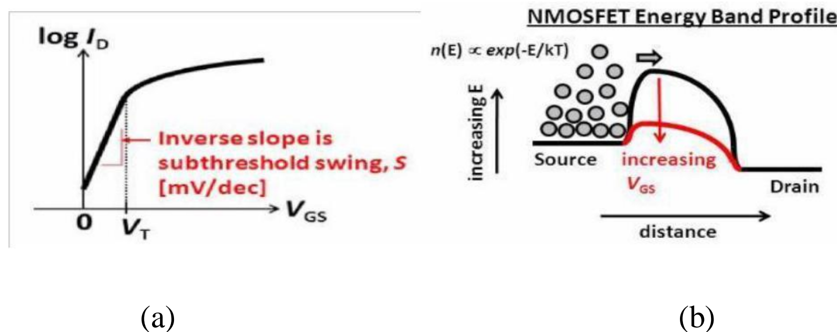
1.3.1 Sub-threshold Swing:

The sub-threshold swing is defined as the gate voltage required changing the drain current by one order of magnitude, per decade. In the MOSFET, the sub-threshold swing is limited to (kT/q) ln10 or 60 mV/ decade at room temperature.

A device characterized by steep sub-threshold slope exhibits a faster transition between off (low current) and on (high current) states. Circuit speed improves with increasing I_{on}; therefore, it would be desirable to use a small V_t. At $V_{gs}<V_t$, an N-channel MOSFET is in the off-state. However, an undesirable leakage current can flow between the drain and the source. The MOSFET current observed at $V_{gs}<V_t$ is called the sub-threshold current. This is the main contributor to the MOSFET off-state current, I_{off}. I_{off} is the I_d measured at $V_{gs}=0$ and $V_{ds}=V_{dd}$. It is important to keep I_{off} very small in order to minimize the static power that a circuit consumes even when it is in the standby mode.

$$S = \left(\left(d\,(\log 10)/dV\right)\right)^{-1}$$

$$= (kT/q) * \ln(10)\,(1+(C_{dep,min}/C_{ox}))$$



(a) (b)

Figure 1.3: (a) I-V curve of sub-threshold swing. (b) Pinch Off condition by increasing V_{gs}

1.3.2 Short Channel Effect:

A MOSFET is considered to be short when the channel length 'L' is the same order of magnitude as the depletion layer widths. The potential distribution in the channel now depends upon both transvers field Ex due to gate bias and also on the longitudinal field Ey due to drain bias when the gate channel length <<1 µm short channel effect become important this leads to many undesirable effects in MOSFET. Six different physical phenomena have to be considered in short channel devices:

- Drain induced barrier lowing (DIBL)
- Surface scattering
- Velocity saturation
- Impact ionization
- Hot electrons
- Mobility degradation

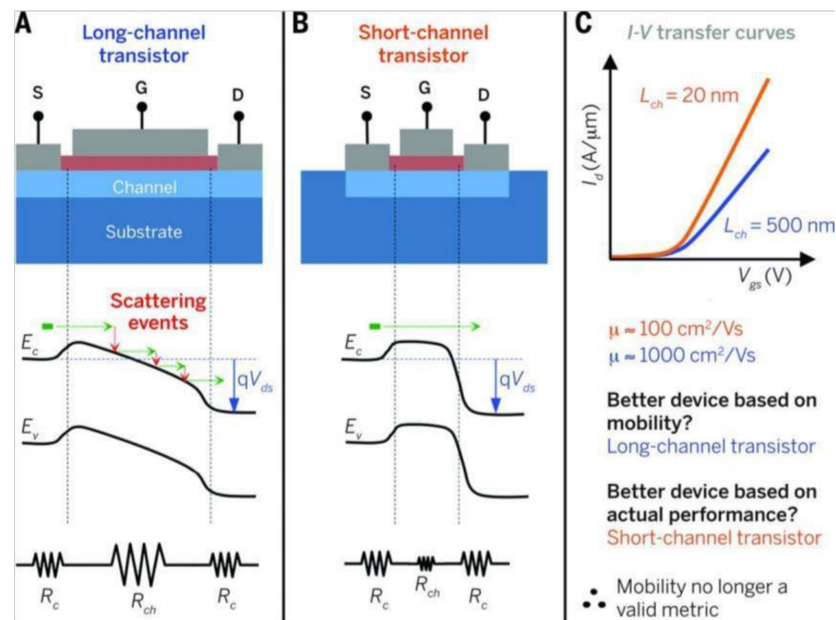


Figure 1.4: Comparison of Long Channel Transistor and Short Channel Transistor

In figure 4, shows that illustrates how the band structure and relevant resistances change between long- and short-channel transistors. Extraction of mobility from two such transistors could yield

mobility that is an order of magnitude smaller for the short-channel devices, even though the performance is much better.

(A) Generic schematic of a long-channel transistor with a corresponding energy band diagram illustrating how the scattering events (red) of electrons (green) moving across the channel lead to a potential drop (sloped bands) of the applied drain-source field (qV_{ds}) and, hence, a substantial resistance in the channel (R_{ch}) compared with resistance at the contacts (R_c). E_c, conduction band edge; E_v, valence band edge.

(B) Same as (A), but for a short-channel transistor where there are very few scattering events in the channel (quasi-ballistic) and hence the potential is dropped at, and the device is limited by, the contacts.

(C) Conceptual transfer curves for the two devices, showing how mobility (μ) mistakenly suggests better performance in the long channel. This diagram illustrates why mobility is no longer a meaningful metric for short-channel (high-performance) transistors but is still valid in long channel (thin-film) transistors. I, current; V, voltage; I_d, drain current.

1.3.2.1 Drain Induced Barrier Lowing (DIBL)

There is a potential barrier between the source and the channel region. The height of this barrier is a result of the balance between drift and diffusion current between these two regions. If a high drain voltage is applied, the barrier height can decrease, leading to an increased drain current. Thus the drain current is controlled not only by the gate voltage, but also by the drain voltage. For device modeling purposes this parasitic effect can be accounted for by a threshold voltage reduction depending on the drain voltage [8].

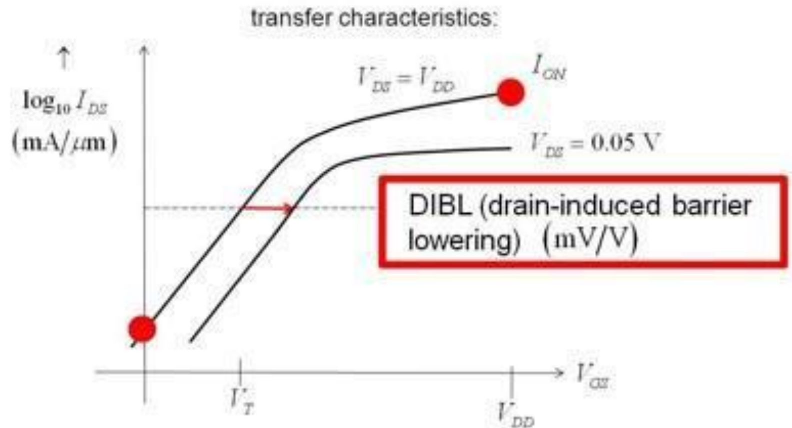


Figure 1.5: IV curve with DIBL

1.3.2.2 Surface Scattering:

Electron transport through metal-oxide-semiconductor field-effect transistor (MOSFET) devices is affected by various scattering mechanisms which shorten the free flight of the electrons flowing inside the device [9]. Electrons scattering can reduce the electron channel mobility [9] and decrease the amount of current that is able to flow through the device [10]. These effects are particularly noticeable when the device is operating at lower temperatures [9]. The boundary between silicon (Si) and silicon dioxide (SiO2) interface at the surface of the device is rough [9] and, since electrons are not allowed to enter the oxide, they must scatter from the rough surface [11].

The surface roughness at the Si-SiO2 interface occurs during the oxide growth stage of fabrication

[12]. The roughness of this boundary is affected by the temperature during the oxide growth and the temperature during the post oxidation annealing phase [10] The roughness at the Si-SiO2 interface leaves a fluctuation of thickness in the oxide, as well as an inconsistent minimum boundary at the surface in the channel region of the device [12], which causes the electric field to vary at the Si-SiO2 interface. The variation in the electric field causes the electron to scatter [13].

1.3.2.3 Velocity Saturation:

In modern day MOSFETs, the channel length is very small, the electric field in the channel is very high, and the velocity saturation effects are very important. The measured electron and hole mobility's in the inversion layer may be quite different than those measured in the bulk.

The channel, in reality, is under a two-dimensional electric field, one directed longitudinally F_v from the gate to the substrate, and the other directed laterally F_x along the length of the channel. The effective inversion layer thickness d_{ch} is approximately given by $d_{ch} = kT/qF_v$ thus, a large vertical field creates a narrow inversion layer, and vice versa. Electrons in the channel move in random directions, undergoing surface scattering, which increases for narrow channels thus their mobility drops.

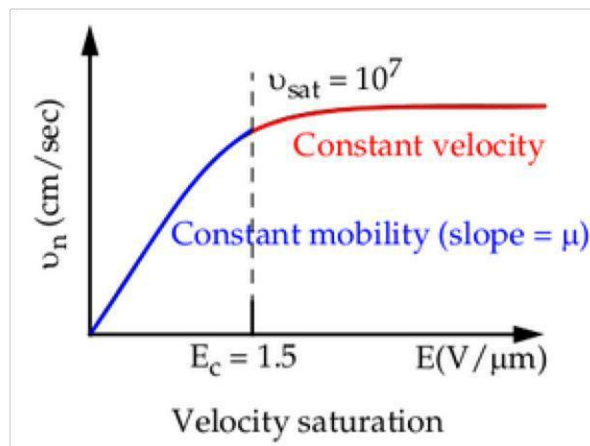


Figure 1.6: IV curve with Velocity Saturation

1.3.2.4 Impact Ionization:

Impact ionization is a typical non-equilibrium process which requires a large electric field. An electron (or hole) in the conduction (or valence) band gains its energy by external electric fields and becomes so highly energetic that it can create an electron-hole pair by colliding with an electron in the valence band and exciting it to the conduction band. Electron-hole pair can also have a rather high energy. In this case the avalanche effect is triggered and the carrier density increases heavily. The device behavior is heavily affected by impact-ionization.

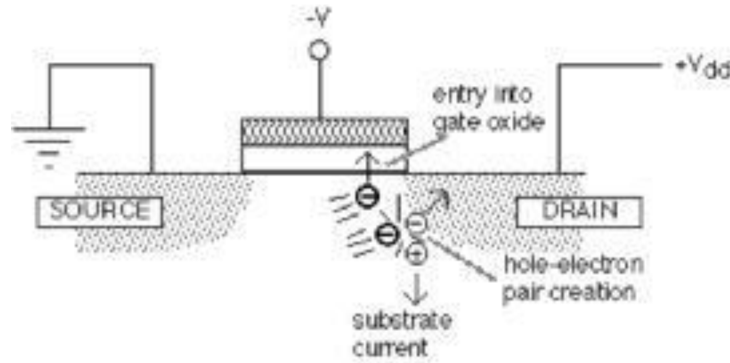


Figure 1.7: Impact Ionization

1.3.2.5 Hot Electron:

Hot electron effect is caused by high electric fields in short channel MOSFETs. High electric fields result in high kinetic energy of electrons and some electrons may get enough energy to overcome the barrier between the body and the gate. This leads to deposition of negative charge on the gate which leads to an increase in threshold voltage by increasing flat band voltage.

This effect is usually limited to n channel devices as holes have much lower mobility than electrons and barrier between valence band of oxide and silicon is higher at about 5eV compared to 3 eV between conduction band of silicon and oxide.

1.3.2.6: Mobility Degradation:

Invers layer charge induced by a vertical field. A positive gate voltage produced force on electrons in the inversion layer towards the drain are attracted to the surface, but they are repelled by localized columbic forces surface scattering. Surface scatter reduce mobility. If V_{gs} increase, mobility decrease.

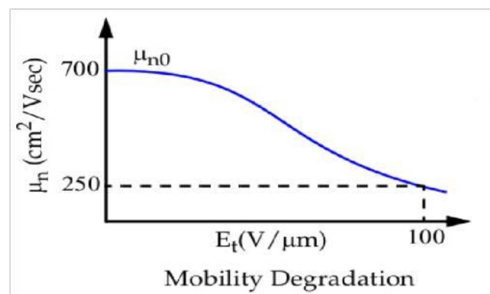


Figure 1.8: Mobility Degradation Curve

1.3.3 Gate Insulator Thickness:

Downscaling is known as performance enhancer for high performance logic products. The International Technology Roadmap for Semiconductors (ITRS) [14] sets strict guidelines for several transistor parameters, which could not be obtained without new manufacturing processes. Performance enhancer in the last years was the reduced physical and capacitive equivalent thickness (CET) of the gate insulator. Further scaling of them is almost impossible without highk insulator materials. Barring the gate leakage issue, thinner gate insulators increase the electric field in the channel region. This will increase the inversion charge density, but also reduce the carrier mobility and force quantum effects in the vicinity of the gate oxide [14].

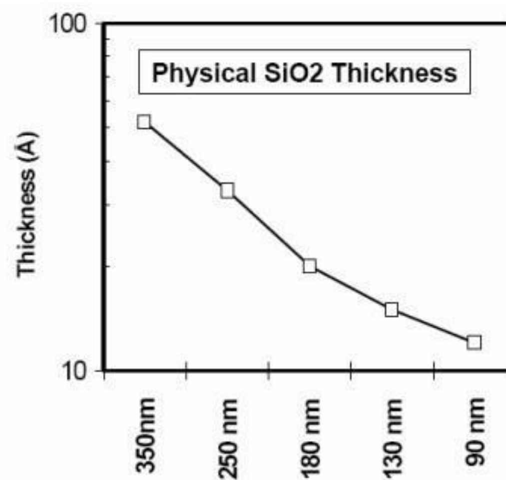


Figure 1.9: Gate Insulator Thickness

1.4 Solution of MOSFET Limitation

There is some solution to overcome that limitation of MOSFET. They are,

- Shallow Junction Technology
- Trade-off between Ion and Ioff
- More Scalable Device Structures

1.4.1 Shallow Junction Technology:

Conventional shallow junctions are made using low energy implants followed by rapid thermal annealing to activate the dopants. This works well for n junctions, which are formed using 'As' as is a large atom, and therefore has a lower implantation range for a given energy than smaller atoms such as P and B. Additionally, channeling is not as severe a problem, and it is therefore possible to obtain box-like profiles for As-doped source / drain junctions. Implantation is typically performed at a 7°angle to minimize channeling [15].

1.4.2 Trade-off between Ion and Ioff:

Ioff would not be a problem if Vt is set at a very high value. That is not acceptable because a high Vt would reduce Ion and therefore reduce circuit speed. Using a larger Vdd can raise Ion, but that is not an acceptable solution because a larger Vdd would raise the power consumption, which is already too large for comfort. Most other changes that could reduce the leakage would also hurt Ion.

1.4.3 More Scalable Device Structures:

This problem of MOSFET limitation can be overcome by changing the structure. There are two ways to change the structure,

- Ultra-Thin-Body MOSFET
- Multi-gate MOSFET

In this thesis paper we are discussing about a types of Multi-gate.

1.5 Multi-Gate MOSFET

In the past decades, the Metal Oxide Semiconductor (MOSFET) has repeatedly been scaled down in size; classic MOSFET channel lengths were once many micrometers, however fashionable integrated circuits square measure incorporating MOSFETs with channel lengths of tens of

nanometers. Intel began production of a method that includes a thirty-two nm feature size (with the channel being even shorter) in late 2009. The semiconductor trade maintains a "roadmap", the ITRS that sets the place for MOSFET development. Historically, the difficulties with decreasing the scale of the MOSFET are related to the semiconductor fabrication method, the necessity to use terribly low voltages, and with poorer electrical performance necessitating circuit plan and innovation (small MOSFETs demonstrate higher outflow currents, and lower output resistance). A multi-gate device or multiple gate junction transistor (MuGFET) refers to a MOSFET (metal–oxide–semiconductor field-effect transistor) which includes quite one gate into a sole device. The multiple gates could also be controlled by one gate. Conductor, whereby the multiple gate surfaces act electrically as one gate, or by freelance gate electrodes.

A multi-gate device using freelance gate electrodes is usually referred to as a Multiple Insulated Gate Field impact electronic transistor (MIGFET). Multi-gate transistors square measure one in every of quite a few ways being developed by CMOS semiconductor makers to form ever-smaller microprocessors and memory cells, conversationally spoken as extending Moore's Law. Development efforts into multi-gate transistors are reported by AMD, Hitachi, IBM, Infineon Technologies, Intel Corporation, TSMC, Free scale Semiconductor, University of American state, Berkeley et al. and also the ITRS.

1.6 Types of Multi-Gate

There are lots of type of multi-gate MOSFET but in our paper we are considering few of them.

1.6.1 Double-Gate MOSFET:

In 1993, Frank designed a 30nm double gate MOSFET [16]. The schematic cross section of the

Double-Gate MOSFET is illustrated to the left in figure 10. As indicated x is the direction from source to drain, parallel to the gate contact and y the direction perpendicular to the gate. The third dimension of the Double-Gate device, the width W, is typically much larger than the other dimensions.

1.6.1.1 Advantages of Double Gate MOSFET:

- Higher drain current
- Higher gate to channel coupling
- Lower short channel effects
- Better scaling possibility

1.6.1.2 Disadvantages of Double Gate MOSFET:

- SCE scaling difficult
- Sensitivity to silicon thickness
- Gate capacitance
- Complex process

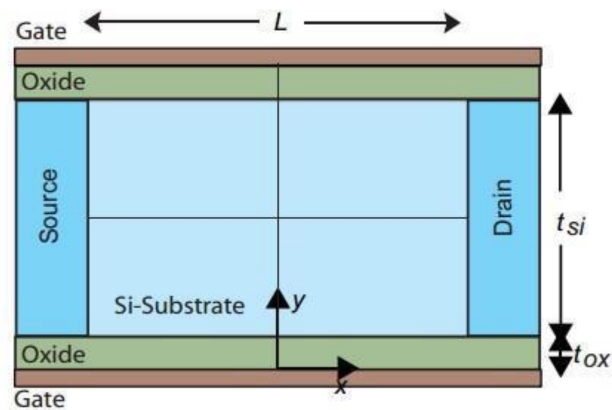


Figure 1.10: Double Gate MOSFET

1.6.2 FINFET

The term Fin-FET was coined by University of American state, Berkeley researchers (Profs. Chenming Hu, Tsujae King-Liu and Jeffrey Bokor) to explain a non-planar, double-gate electronic transistor engineered on associate SOI substrate, supported the previous DELTA electronic transistor style. The distinctive feature of the Fin-FET is that the conducting channel is wrapped by a skinny semiconductor ‘fin’ that forms the body of the device. The thickness of the

fin determines the effective channel length of the device. In current usage the effective Fin-FET feature a less actual definition. Among silicon chip makers, AMD, IBM and Motorola describe their double-gate development efforts as Fin-FET extension where as Intel avoids mistreatment the term to explain their closely connected tri-gate design [17].

1.6.2.1 Advantages of FinFET:

- Higher technological maturity than planer DG
- Suppressed short channel effect
- Better in driving current
- More compact
- Low cost

1.6.2.2 Disadvantages of FinFET

- Reduce mobility for electrons
- Higher source and drain resistance [18]
- Both improve or degrade reliability compared to the planar technologies.

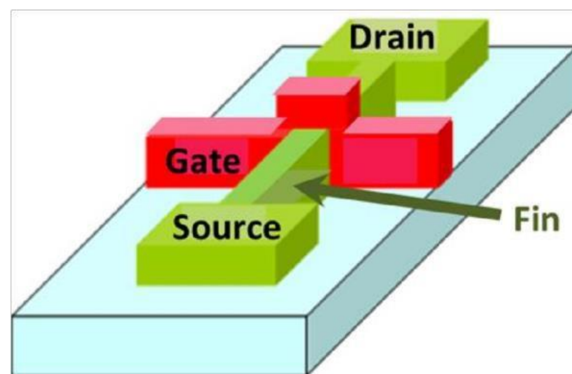


Figure 1.11: FINFET

1.6.3 Tri Gate MOSFET:

The Tri-Gate technology gets its name from the fact that transistors using it have conducting channels that are formed on all three sides two each side, one across the top of a tall and narrow

silicon fin that rises vertically from the silicon substrate. The gate is the terminal that drives the transistor on and off, and acts like a capacitance where charge is stored making the channel conductive [19]. An Intel 3D transistor design introduced in 2011 with tri gates Ivy Bridge microarchitecture. The Tri-Gate design is considered 3D because the gate wraps around a raised source-to-drain channel, called a "fin," instead of residing on top of the channel in the traditional 2D planar design.

1.6.3.1 Advantages of Tri gate:

- Improved switching characteristics
- Higher driving current
- More impact

1.6.3.2 Disadvantages of Tri gate:

- The major issue of such devices is corner effect which occurs due to presence of trapped charges at the edge of the corner. Thus the device exhibits high temperature and causes reliability issues, high leakage current and also worsens the SCEs.

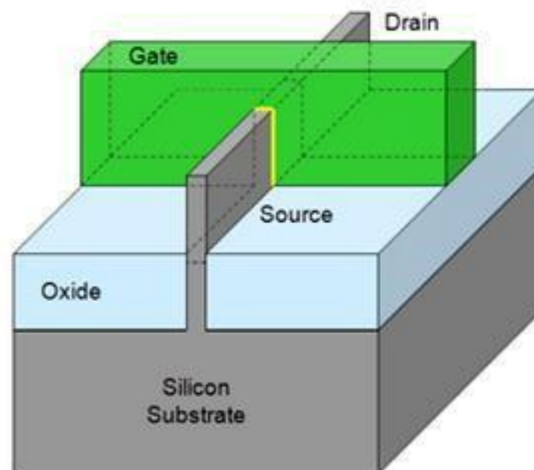


Figure 1.12: Tri Gate MOSFET

1.6.3 Gate-All-Around MOSFET:

The cylindrical gate all around (GAA) MOSFET is one of the novel devices which further enables scaling without hindering the device performance [20]. Today mobile and computing markets

continue to innovate at a dramatic rate delivering more performance in smaller form factors with higher power efficiencies. According to Moore’s law, the number of transistors in an area should double every month. To make this into reality, transistors should get shrink in size to accommodate double the number per unit area. While scaling down the device channel length, the short channel effects are raised. As the technology scaling continues, GAA is known to be a probable alternative to solve the problems related to short channel effects of planar technology. Cylindrical gate all around (GAA) MOSFET is a drastic invention and a potential candidate to replace other multi-gate MOSFET [21].

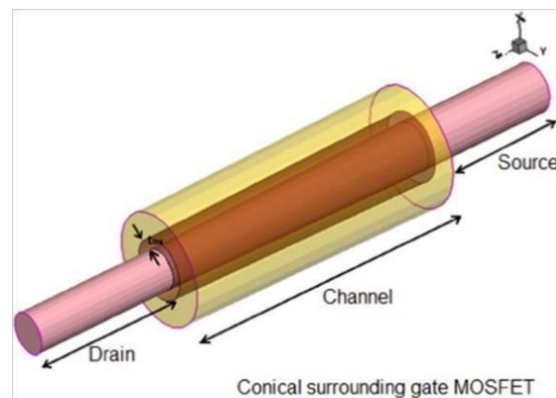


Figure 1.13: Gate-All-Around MOSFET structure

1.7 Device Structure Gate-All-Around (GAA) MOSFET

In terms of electrostatic control to scale to shortest possible channel length, GAA is the ultimate structure. When the gate length scaling is no longer effective due to the limits of contact width, a transition to a vertical structure, which is not limited by restriction in the perpendicular direction, is needed. The vertical structure can be implemented in different layout configurations [22]. A GAA MOSFET includes a source, channel and drain surrounded by a top gate and a buried bottom gate, the latter of which also has application for other buried structures and is formed on a bottom gate dielectric which was formed on source, channel and drain semiconductor layer. After forming a planar bottom insulator layer on the bottom gate and gate dielectric, the device is flip-bonded to an oxide layer of a bulk silicon wafer, thereby encapsulating the buried bottom gate electrode in insulating oxide. The semiconductor layer forms the source, drain and channel in a mesa structure on which is deposed a top gate dielectric a top gate, and top gate insulator as well as four conductors

for connecting to the source, drain, top gate and bottom gate. The latter two electrodes can be independently controlled or commonly controlled for enhanced operating of GAA MOSFET having improved isolation and reduced parasitic capacitance due to the use of encapsulating layers of the merged wafer consisting of two bonded wafers [23].

1.8 Advantages of GAA

- Higher packing density as compared to the other multiple- gate MOSFETs
- Proper design parameters are attractive for circuit design in nanometer era because of better scalability.
- Used for low voltage, low power and high frequency applications.
- Low cost, high operational speed and better performance, the dimension of the conventional transistors need to be downscaled to sub-nanometer region.
- Better gate control.

1.9 Fabrication of GAA

Hashemi, Pouya, a group from Massachusetts Institute of Technology proposed a paper about GAA FET fabrication which contains ‘69’step, ‘Gate-all- around silicon nanowire MOSFETs: top-down fabrication and transport enhancement techniques’.

1.10 Literature Review:

The research of multi-gate MOSFET happened about quarter century ago, in 1980’s. The first multi-gate transistor was that published by Hieda etal [25] in 1987. From that paper authors realized that fully depleted body of silicon based transistor helps to improve switching due to lessened body bias effect. A year later the same group reported an ultimate multi-gate transistor-gate-all-around(GAA), which was formed around vertical pillar of silicon [26]. One year later, Hisamoto et al [27] demonstrated an ancestor of Fin FET- first double gate transistor, in bulk silicon, called DELTA. In 1990, J.P. Colinge (researchers from IMEC, Leuven, Belgium) they describes the process fabrication and found the characteristics of SOI (silicon-on-insulator) MOSFET with gate oxide GAA (gate-all-around) device. They have found that, the trans-conductance of the 'gate-all-around' device is more than twice that of a conventional SOI device,

and its sub-threshold slope is nearly 60 mV/decade at room temperature [28]. In 1994, E. Simoen and C. Claeys (IMEC, Belgium) published a paper on DC characteristics of gate-all-around (GAA) silicon-on-insulator MOSFETs at cryogenic temperatures. This paper describes the static I-V characteristics at cryogenic temperatures (77 K and 4.2 K) of so-called dual-gate Silicon-On-Insulator (SOI) MOSFETs, fabricated in the Gate-all-Around (GAA) technology [29]. In 1996, inventors Donandl C. Mayer, Palos Verdes from USA proposed a paper about Silicon on insulator GAA MOSFET device and fabrication methods. This invention relates to the class of transistors called metal-oxide-semiconductor field-effect transistors (MOSFETs) and more particularly to MOSFETs formed in semiconductor layers on insulated substrates of a silicon-on-insulator (SOI) wafer, and more particularly to the class of SOI MOSFETs formed with gate electrodes at the top and bottom of the semiconductor layer substantially forming gate-all-around (GAA) MOSFETs, hereinafter referred to as SOI GAA MOSFETs [23]. After two years in 1998, some Japanese researchers (ToshikazuMukaiyama, Ken-ichiSaito, HirokiIshikuro) research about fabrication of gate-all-around MOSFET by silicon anisotropic etching technique. Fabrication process of gate-all-around (GAA) MOSFETs using an anisotropic etching technique has been proposed. In this technology, the channel width of the GAA device is not limited by the lithography resolution and the density of the wire channel is doubled [30]. In between 2000 to 2003, researchers research on GAA. In 2004, David Jimenez, J. Saenz, Benjamin Iniguez published in IEEE Electron Device Letters about Modeling of Nano scale gate-all-around MOSFETs. They present a compact physics-based model for the nanoscale gate-all-around MOSFET working in the ballistic limit. The current through the device is obtained by means of the Landauer approach, being the barrier height the key parameter in the model [31]. In 2005, Juan José Sáenz, Jordi Suñé Lluis Francesc Marsal proposed a paper about Compact Model of the Nano scale Gate-All-Around MOSFET [32]. Next year, South Korean group (Jae Young Song, Woo Young Choi and Ju Hee Park) published a paper in IEEE Transactions on Nanotechnology on Design optimization of gate-all-around (GAA) MOSFETs. The design of gate-all-around (GAA) MOSFETs was optimized and compared with that of double-gate MOSFETs. They discussed the optimal ratio of the fin width to the gate length and investigated short-channel effects of GAA MOSFETs [33]. In 2007, Hamdy Abd El Hamid and Benjamin Iniguez (Departament d' Enginyeria Electronica, Electrica i Automatica, Univ. Rovira i Virgili, Tarragona) published a paper in IEEE Transactions on Electron Devices about analytical Model of the threshold voltage and sub-threshold swing of un-doped cylindrical gate-all-around-

based MOSFETs. Analytical physically based models for the threshold voltage, sub-threshold swing, and drain-induced barrier lowering (DIBL) of un-doped cylindrical gate-all-around MOSFETs have been derived based on an analytical solution of 2-D Poisson's equation (in cylindrical coordinates) in which the mobile charge term has been included [34]. In 2008, Zhihong Chen (Member, IEEE) published a paper about Externally Assembled Gate-All-Around Carbon Nanotube Field-Effect Transistor. In this paper, we demonstrate a gate-all-around single wall carbon nanotube field-effect transistor. This is the first successful experimental implementation of an off-chip gate and gate-dielectric assembly with subsequent deposition on a suitable substrate. The fabrication process and device measurements are discussed in the paper [35]. On that year, Yu-Sheng Wu and Pin Su (Dept. of Electron. Eng., Nat. Chiao Tung Univ., Hsinchu) proposed a paper in IEEE Transactions on Electron Devices about Sensitivity of Gate-All-Around Nanowire MOSFETs to Process Variations—A Comparison With Multi-gate MOSFETs. This paper investigates the sensitivity of gate-all-around (GAA) nanowire (NW) to process variations compared with multi-gate devices using analytical solutions of Poisson's equation verified with device simulation. GAA NW and multi-gate devices with both heavily doped and lightly doped channels have been examined regarding their immunity to process-induced variations and dopant number fluctuation [36] in 2009, there is a journal by B. Nae, A. Lazaro, and B. Iniguez about High frequency and noise model of gate-all-around metal-oxide-semiconductor field-effect transistors. The gate-all-around (GAA) metal-oxide-semiconductor field-effect transistor is one of the most promising candidates for the downscaling of complementary metal-oxide-semiconductor technology toward the sub-50-nm channel length range since the SGT architecture allows excellent control of the channel charge in the silicon film, thus reducing short channel effects [37]. In 2010, Ru Huang (Peking University (PKU) Beijing 100871, China) proposed a presentation about Gate-All-Around Si Nanowire Transistors (SNWTs) for Extreme Scaling: Fabrication, Characterization and Analysis [38]. In that same year, Hashemi, Pouya proposed a paper on Gate-all-around silicon nanowire MOSFETs: top-down fabrication and transport enhancement techniques. Scaling MOSFETs beyond 15 nm gate lengths is extremely challenging using a planar device architecture due to the stringent criteria required for the transistor switching. The gate-all-around geometry enhances the electrostatic control and hence gate length scalability. In addition, it enables use of an undoped channel, which has the potential to minimize threshold voltage variation due to reduced random dopant fluctuations. However, there is little known about carrier mobility in Si nanowire

MOSFETs [39]. Next year, J. J. Gu, Y. Q. Liu, Y. Q. Wu proposed a paper on First Experimental Demonstration of Gate-all-around III-V MOSFETs by Top-down Approach. The first inversion-mode gate-all-around (GAA) III-V MOSFETs are experimentally demonstrated with a high mobility In0.53Ga0.47As channel and atomic-layer-deposited (ALD) Al2O3/WN gate stacks by a top-down approach. A well-controlled InGaAs nanowire release process and a novel ALD high-*k*/metal gate process has been developed to enable the fabrication of III-V GAA MOSFETs [40]. In 2012, J. J. Gu, X. W. Wang proposed a paper in School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette about III-V Gate-all-around Nanowire MOSFET Process Technology: From 3D to 4D. In this paper, they have experimentally demonstrated, for the first time, III-V 4D transistors with vertically stacked InGaAs nanowire (NW) channels and gate-all-around (GAA) architecture. Novel process technology enabling the transition from 3D to 4D structure has been developed and summarized [41]. In this same year, S.L.Tripathi, Ramanuj Mishra, R.A.Mishra (Department of Electronics and Communication Engineering, MNNIT, Allahabad) published a paper on High fin width MOSFET using GAA structure [42]. In 2013, Rajni Gautam, Manoj Saxena, R. S. Gupta (India) proposed a paper in IEEE Transactions on Nanotechnology on Gate-All-Around Nanowire MOSFET With Catalytic Metal Gate For Gas Sensing Applications. In this paper, gate-all-around (GAA) MOSFET with catalytic metal gate is proposed for enhanced sensitivity of gas sensor. The GAA nanowire MOSFET has already been demonstrated experimentally for bio-sensing and chemical sensing applications. However, cylindrical GAA MOSFET with catalytic metal gate for gas sensing applications is proposed for the first time in this paper [43]. Next year, Liu Ying, He Jin, Chan Mansun (School of Electronics and Computer Science, Peking University, Beijing 100871, China) published a paper about an analytic model for gate-all-around silicon nanowire tunneling field effect transistors. In this paper they describe Tunneling field effect transistors (TFETs) have received much attention in the semiconductor academic research and industry fields for their superior performance in the sub-threshold region [44]. Another group (Neeraj Gupta and A.K. Raghav) proposed a paper on a study on multi material gate all around SOI MOSFET [4]. In 2015, research of GAA is increasing and lots of paper of was published on that year. Biswajit Jena, Kumar Prasannajit Pradhan, Sidharth Dash published a paper on investigation on cylindrical gate-all-around (GAA) to nano wire MOSFET for circuit application. The purpose of this paper to get low cost, high operational speed and better performance, the dimension of the conventional

transistors need to be downscaled to sub-nanometer region. The reduction of MOSFET dimensions will degrade the gate control over the channel due to the close proximity between the sources and drain [46]. Another group Kuan-Chou Lin, Wei-Wen Ding proposed a paper about an Analytical Gate-All-Around MOSFET Model for Circuit Simulation [47]. In 2016, Tarun Kumar Sachdeva, Dr. S.K. Aggarwal, (Research Scholar, EEE Department, YMCAUST, Faridabad and Professor,
EEE Department, YMCAUST, Faridabad) published a paper on Design, Analysis & Simulation of 30 nm Cylindrical Gate all around MOSFET. In this work, electrical characteristics of cylindrical GAA (CGAA) MOSFET at 50nm channel length, 10nm channel thickness are systematically analysed. Various electrical characteristics such as on current (ION), sub-threshold leakage current (IOFF), the threshold voltage, DIBL are calculated and analysed at various device design parameters [21]. On this year, Julien Happich proposed an article about Imec stacks Gate-all-Around Si nanowires vertically in CMOS MOSFETs. In this paper, as well as building the GAA nanowire MOSFETs, the researchers also reported their findings on how the intrinsic ESD performance of the MOSFET is impacted by the novel nanowire architecture, proposing the integration of two different ESD protection diodes, a gate-structure defined diode (gated diode) and a shallow-trench isolation defined diode (STI diode). GAA nanowire transistors enable ultimate CMOS device scaling, with low degree of added complexity compared to alternative scaling scenarios, stated Dan Mocuta, Director Logic Device and Integration at imec [48]. subindu kumar, Amrita Kumari published a journal on Modeling gate-all-around Si/SiGe MOSFETs and circuits for digital applications. Apart from excellent electrostatic capability and immunity to short-channel effects, the performance of gate-all-around (GAA) nanowire (NW) metal-oxide-semiconductor field-effect transistors (MOSFETs) can be further enhanced by incorporating strain [49]. Another paper proposed by K. Takase, Y. Ashikawa on highly gate-tunable rashba spin-orbit interaction in a gate-all-around InAs nanowire MOSFETs [50]. There is another journal by Suman Sharma, Rajni Shukla about an Extensive Evaluation of Futuristic Gate All Around Junction-less Nanowire MOSFET Using Numerical Simulation. This paper presents an extensive review of homogeneously doped Junction-less Cylindrical Gate-All-Around (JL-C-GAA) MOSFET using numerical simulations to look into deep physical insight of the device. The electrical and analog/RF performance has been investigated [51]. In this year Vandana Nath, Subhasis Haldar proposed a paper in IEEE Transactions on Electron Devices on Gate-Induced Drain Leakage Reduction in Cylindrical Dual-Metal Hetero-Dielectric Gate-All-Around
MOSFET.

In this paper, an analytical model of dual-metal hetero-dielectric (DM-HD) cylindrical gate all around (GAA) MOSFET has been proposed to address and solve a substantial issue of gate-induced drain leakage (GIDL) current in order to improve the device reliability, band-to-band tunneling (BTBT), and OFF state leakages. The structure is based upon asymmetric gate oxide structure by combining silicon dioxide (SiO_2) gate dielectric at source side and vacuum dielectric at drain side, which significantly reduces BTBT and OFF-state gate leakages, thereby making it suitable for low-power applications [52].

1.11 Thesis objective and motivation

In this thesis we have analyzed a Gate All Around MESFET which can be a possible candidate of traditional MOSFET. We have analyzed the device performance like potential, electric field, drain current for varying device parameters. Channel length, oxide thickness and radius of the Si body have been changed to see the performance of the device electrical characteristics. From the current-voltage curve, threshold voltage, sub threshold slope and DIBL have been observed. Threshold voltage roll-off has also been studied. Finally, high-k dielectric and gate stack structure have been investigated to see whether it improve the device performance.

1.12 Thesis layout

The thesis is dividing into 4 chapters; the first chapter provides the background about the traditional MOSFET its limitation and possible solution.
Different structure is processed by the scientist to address the problem here by MOSFET. Some of these structures have been discussed.
Chapter 2 focuses on the numerical analysis of the device using TCAD software SILVACO. The chapter unveils the process and methodology in order to define complex structure in process simulator like ATLAS. After the definition of the devices physical parameters, like channel length, gate length cavity length etc. Biasing condition is applied using the Tony Plot tool for different electrical properties of the device like surface potential, energy band etc. can be extracted for that device using Tony plot.

Chapter 3 focused on the analysis of various device electrical characteristics biasing parameter. Potential, electron concentration, transfer characteristics curve threshold, sub slope and DIBL have been analysis to evaluate device perform.

Finally chapter 4 concludes the thesis by depicting scopes limitations of the work

Chapter 2

Numerical Modeling

2.1 Introduction:

Most real-word applications lead to mathematical problems which cannot be solved with exact formulas, or analytically. A numerical model is solved with numerical methods, introducing additional errors which gives one an insight into physics based simulation. That model uses some sort of numerical time-stepping procedure to obtain the models behavior over time. Normally there are large number of governing equations which represents device dependency on different process parameters. With increasing complexity like this work of asymmetric B-channel MOSFET, the number of equation may get even larger than expected. This equation is send to predict the electrical characteristics at different points which are called nodes in a given framework of device structure. As there may be thousands of nodes to analyze, the set of equation has to be solved repeatedly to determine characteristics and extract important parameters. Such modeling is very time consuming but comes up with greater accuracy. Numerical modeling of semiconductor devices is normally done different Technological Computer Aided Design software. SILVACO is an example of such TCAD software. SILVACO delivers a full TCAD-to-signoff flow for vertical markets including: displays, power electronics, optical devices, radiation and soft error reliability and advanced CMOS process and IP development. For over 30 years, SILVACO has enabled its customers to bring superior products to market at reduced cost and in the shortest time.

2.2 Overview of Numerical Software

In this software ATLAS provides general capabilities for physically-based two (2D) and three dimensional (3D) simulation of semiconductor devices. Silvaco ATLAS is a physically-based device simulator which predicts the electrical characteristics that are associated with specified physical design and bias conditions. By applying a set of differential equations, based on Maxwell's laws, we can simulate the transport of carriers through a device [53]. Physically-based simulation is very different from analytical modeling which provides efficient approximation and interpolation but does not provide insight, or predictive capabilities, or encapsulation of the theoretical knowledge [54]. Atlas predicts the electrical and optical characteristics which are

connected with specified physical structures and voltage bias conditions. This is achieved by approximating the operation of a device onto a two or three dimensional mesh, consisting of a number of grid points called nodes. The mesh of device structure was made before. By applying a set of differential equations, derived from Maxwell's laws, onto this grid we could simulate the transport of carriers through a structure. Physically-based simulation is very important for two reasons. Firstly, it is usually much quicker and cheaper than performing experiments. Secondly, it provides information that is difficult or impossible to measure. ATLAS includes with DECKBUILD, TONYPLOT, DEVEDIT, MASKVIEWS, and OPTIMIZER. DECKBUILD provides an interactive run time environment. TONYPLOT supplies scientific visualization capabilities. DEVEDIT is an interactive tool for structure and mesh specification and refinement. MASKVIEWS is an IC Layout Editor. The OPTIMIZER supports black box optimization across multiple simulators [53]. There are three physically-based simulations. These are:

- It is predictive.
- It provides insight.
- It conveniently captures and visualizes theoretical knowledge.

In ATLAS, there three tasks to simulate a device:

- Physical structure to be simulated
- Physical models to be used
- The bias conditions to obtain electrical characteristics

2.3 Simulation Method

In the previous sections it has been mentioned that in ATLAS to simulate a device one need to define the physical structure, models and bias conditions. In this section a broad discussion will be provided hoe these steps will be defined.

The whole process in the simulation can be divided into five groups as follows-

1. Structure Specification
2. Material Specification
3. Numerical Method Specification
4. Solution Specification
5. Result Analysis

These five groups specification has to be maintained in an ordered passion as shown in figure 2.1

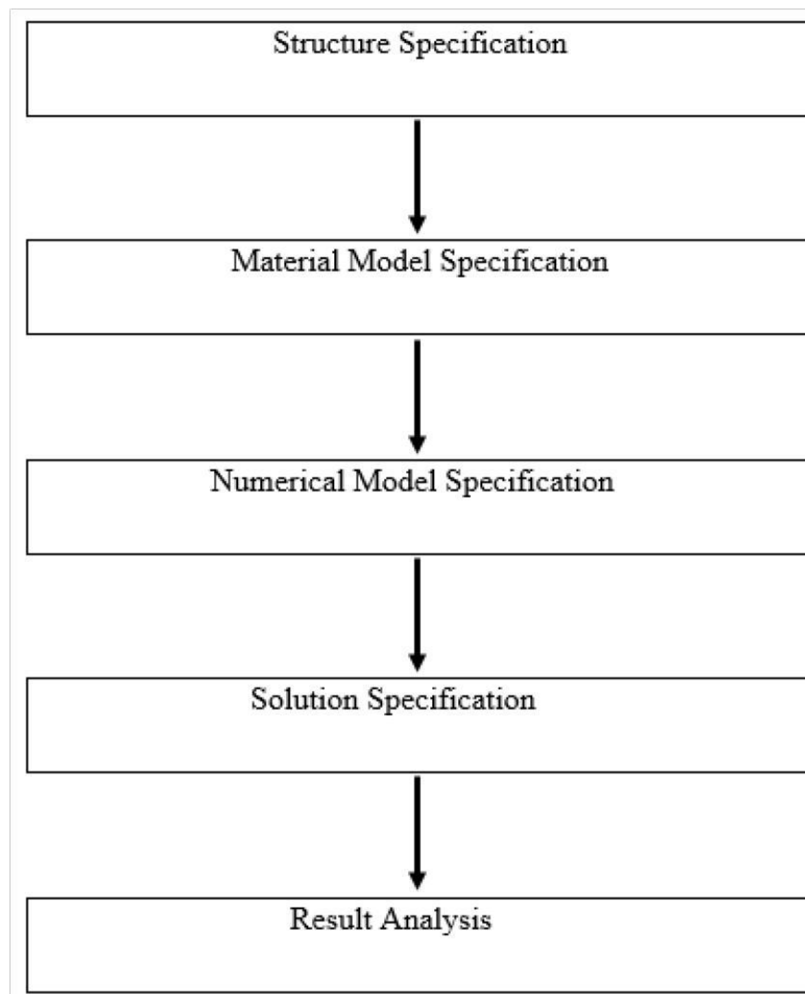


Figure 2.1: five group of operations in order to simulate a device.

The five groups and analysis are again sub-divided into a number of groups. In the following sub section these sub-division of primary groups are discussed.

2.3.1 Structure specification

In this section, first of all two or three dimensional grid points are specified. In order to analyze junction less Gate-All-Around device here, two dimensional grid specification has been done by MESH specification. A typical order of structure specification is shown in flow diagram in figure 2.2.

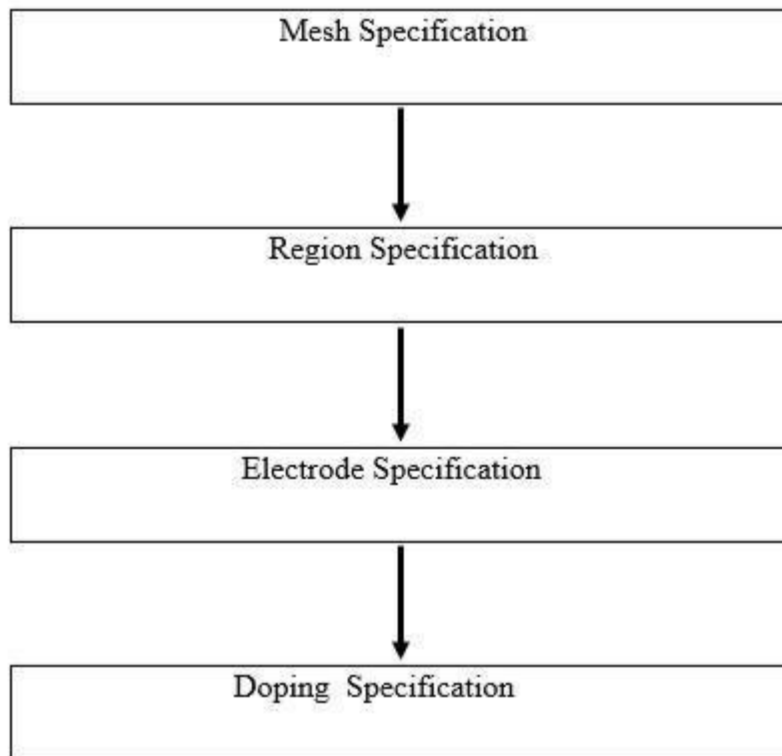


Figure 2.2: components of structure specification in an ordered manner.

While specifying mesh, it is also possible to achieve greater resolution in any particular region, especially on the boundaries. For an example, for the junction less gate all around MOSFET is shown on figure 3.1, greater resolution has been specified on the source, drain and channel length. The greater resolution on those boundaries increases grid points at those regions. As ATLAS simulated electrical characteristics based on the grid point or commonly known as nodes, more accurate electrical behavior will be obtained with increased numbers of nodes. A typical mesh specification is shown in figure 2.3.

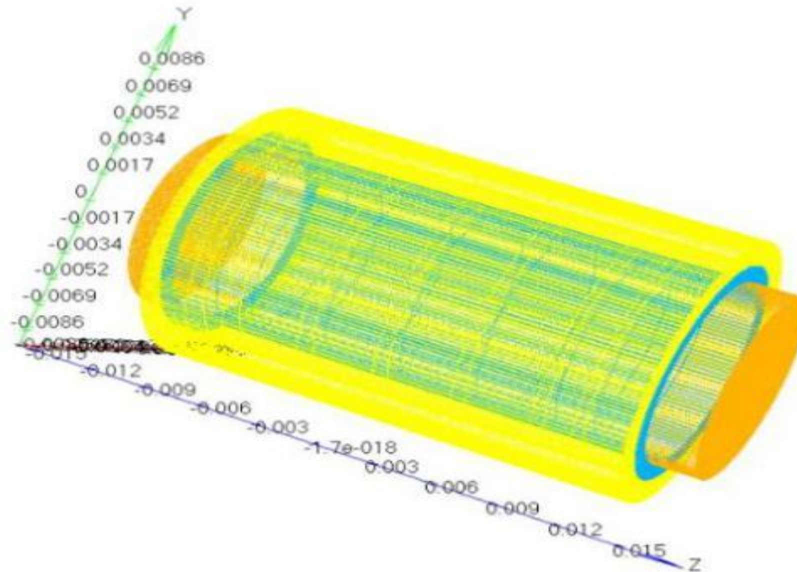


Figure 2.3: Landscape of an n-type junction less cylindrical surrounding gate transistor with visible mesh

Next step in this group is to specify REGIONs. The device may be fabricated with different materials in different regions. This can be specified in the simulator by using REGION specification. The devices can be divided into regions by specifying minimum and maximum x and y co-ordination. After specifying regions, different materials can be assigned in these regions.

The electrodes of the device normally lie on source, drain and gate side. Material of the electrode may vary which is specified in contacts, a sub-division of material model specification group.

A typical diagram of Regions and another diagram of Electrodes of a junction less cylindrical surrounding gate transistor is shown in figure 2.4 and figure 2.5. Different materials are specified in different regions. For example, Si assigned in substrate region and SiO_2 is assigned in oxide region.

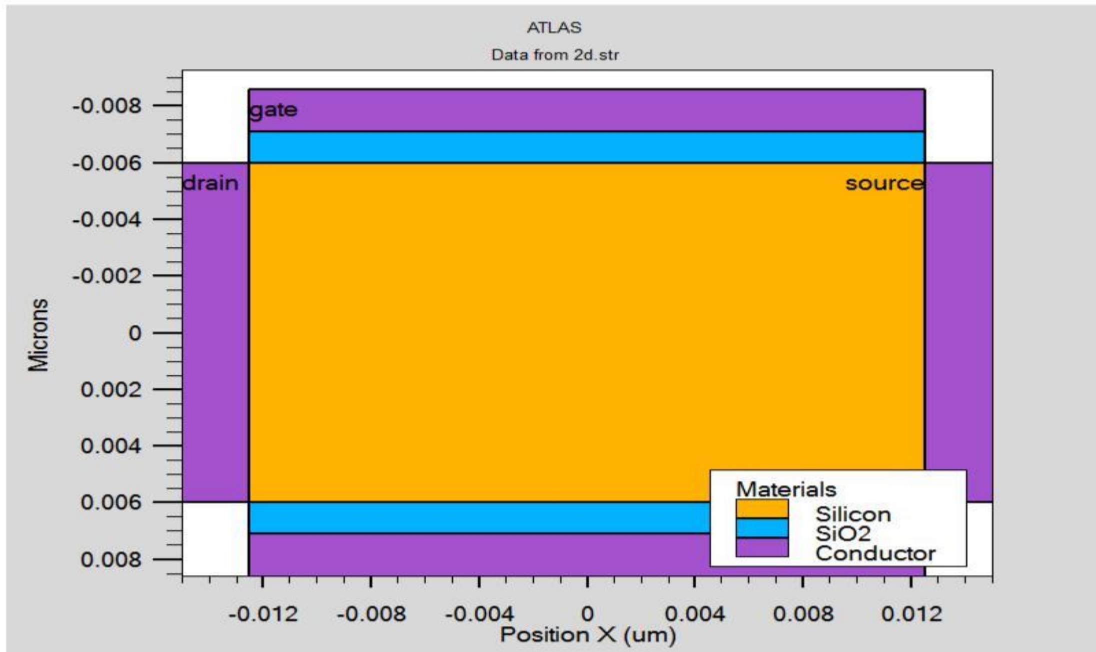


Figure 2.4: Regions in a device structure

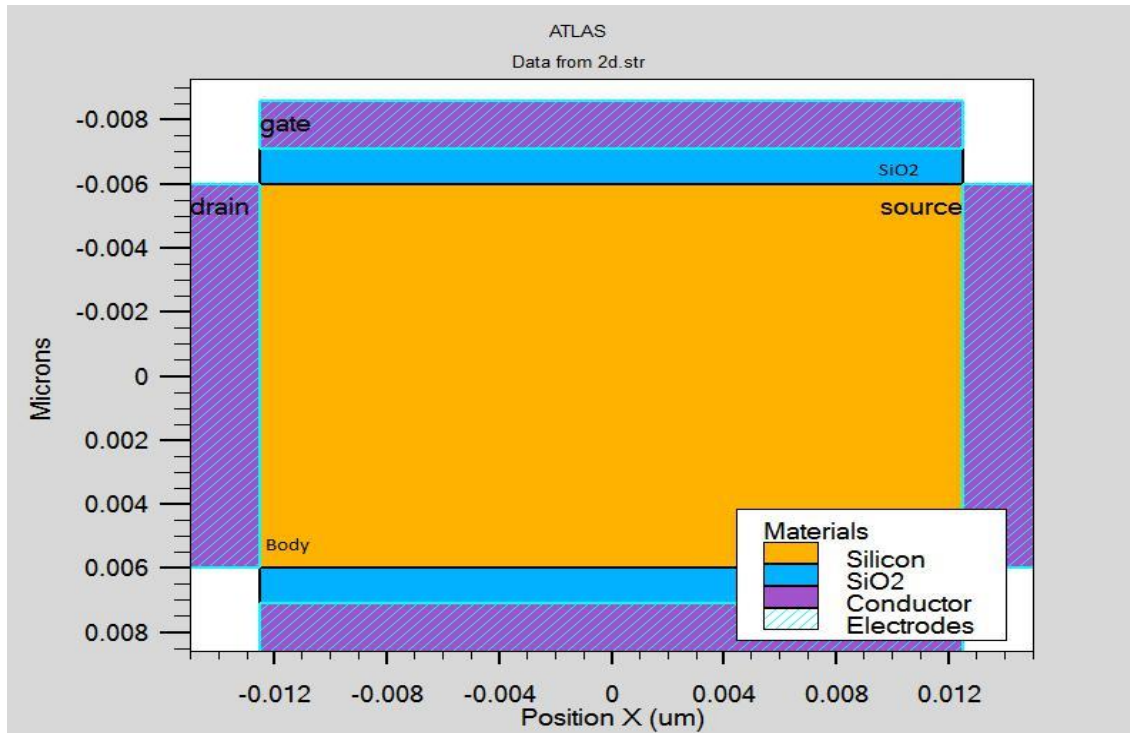


Figure 2.5: Electrodes in a device structure

After assigning different regions into different materials and electrodes, necessary doping is assigned. Doping can be assigned in specified regions or by defining maximum minimum x-y-z co-ordinates. While specifying doping, the doping type, n-type or p-type and the doping level in per cm^3 unit has to be assigned. As it is junction-less Gate-All-Around MOSFET, so the doping should be either n-type or p-type for source, drain and channel, like n-n-n type or p-p-p type. The first group structure specification terminates with specifying doping level and types and then next group takes the action. There is a diagram of Landscape of an n-type junction less cylindrical surrounding gate transistor in figure 2.6.

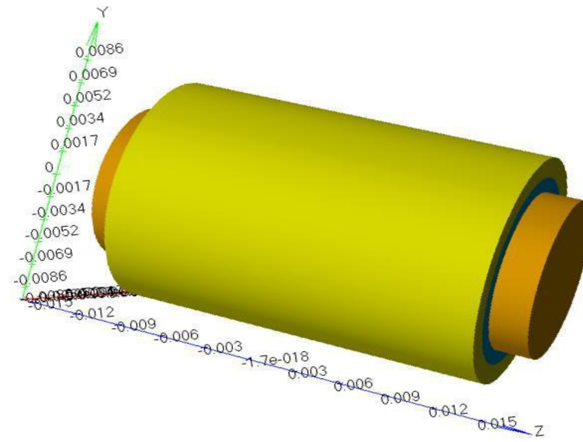


Figure 2.6: Landscape of an n-type junction less cylindrical surrounding gate transistor

2.3.2 Materials Model Specification

As shown in the flow chart diagram in figure 2.1 the second group is called Material Model specification. The group contains a number of sub divisions among which two are considered as shown in figure 2.7 in an ordered manner.

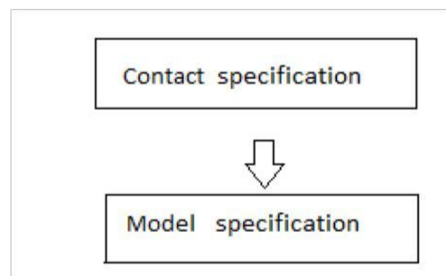


Figure 2.7: Components of materials model specification in an ordered manner

In this group, the first of all contact of the device has to be specified. Electrodes placement has been assigned under the electrode specification in the first group. Contact specification specifies the materials that to be incorporated with these electrodes and necessary properties can also be specified like specifying work function of the contact. In this work, the electrodes are set as conductor as well as the front and back gate.

After establishing contact parameters, model has to be specified by which a set of differential conditions of the given device can be set. There are different kinds of models exist in ATLAS which is used to include carious physical mechanism and parameter.

2.3.3 Model specification

In this paper we are using some models,

- Boltzmann
- Masetti
- Print

2.3.3.1 Boltzmann

The use of Boltzmann statistics instead of Fermi-Dirac statistics makes subsequent calculations much simpler. The use of Boltzmann statistics is normally justified in semiconductor device theory, but Fermi-Dirac statistics are necessary to account for certain properties of very highly doped (degenerate) materials. The Fermi-Dirac statistics have been implemented in ATLAS in a similar form to Boltzmann statistics. The remainder of this section outlines derivations and results for the simpler case of Boltzmann statistics which are the default in ATLAS. You can have ATLAS use Fermi-Dirac statistics by specifying the FERMIDIRAC parameter in the MODEL statement.

2.3.3.2 Masetti

The low field carrier mobility can be defined in five different ways. The first way is use the MUN and MUP parameters to set constant values for electron and whole mobility's. The second way is by using a look-up table model (CONMOB) to relate the low field mobility at 300K to the impurity concentration. The third way is by choosing the analytic low field mobility models, ANALYTIC, ARORA, or MASETTI, to relate the low field carrier mobility to impurity concentration and temperature. The fourth way is by choosing a carrier-carrier scattering model (CCSMOB, CONWELL, or BROOKS) that relates the low field mobility to the carrier concentrations and temperature. The fifth way is to use a unified low field mobility model (KLAASSEN) that relates the low field mobility to donor, acceptor, lattice, carrier-carrier scattering, and temperature.

2.3.3.3 Print

As with the case for lumped elements, ATLAS can print out a value of contact resistance for each contact in the run time output. Since the actual value depends on the length of each surface segment for distributed contacts, ATLAS prints out the value of CON.RESIST/WIDTH which is the same for all contact surface segments. This runtime output is enabled by adding the PRINT option on the MODELS statement.

2.3.4 Numerical Method Specification

After establishing the model that is a set of differential equations for the device, a numerical method has to be followed to obtain the solution of such complex equations. In ATLAS there are different nu electrical metrical methods are available like Newton-Raphson method, Gummel method, single position method etc. in this work, Newton-Raphson method has been applied to solve the set of mathematical equations in iterative manner.

2.3.4.1 Newton Method

The newton method solves the total system of unknowns together. It is useful when the system of equations is strongly coupled and has quadratic convergence. It may spend extra time solving for quantities that are essentially constant or weakly coupled. However, for almost all cases, this

method is preferred and it is the default. The following cases require the Newton method to be set for isothermal drift diffusion simulations:

- Current boundary condition
- External element
- AC analysis
- Impact ionization

2.3.5 Solution Specification

Different terminal of devices is applied different bias voltage. Using ATLAS applying DC voltage at different terminals of the device, electrical characteristics can be found DC solution. Electrical characteristic of the device consists electrical current through the device, carrier concentration, electric field etc. To obtain Drain current vs Gate voltage characteristic, gate voltage has been swept from an initial value to a final value with appropriate step value like 0.01 and the result are stored in a LOG file, later the LOG file has been used in TONYPLOT to analyze the result.

2.3.6 Result Analysis

Result of the simulated device van be analyzed in three ways.

1. Run time output

2. Solution file

3. Log file

2.4 ATLAS Modeling Summary

The summary of operations that to be followed to successfully model a semiconductor device in two dimension is show in following figure 2.8.

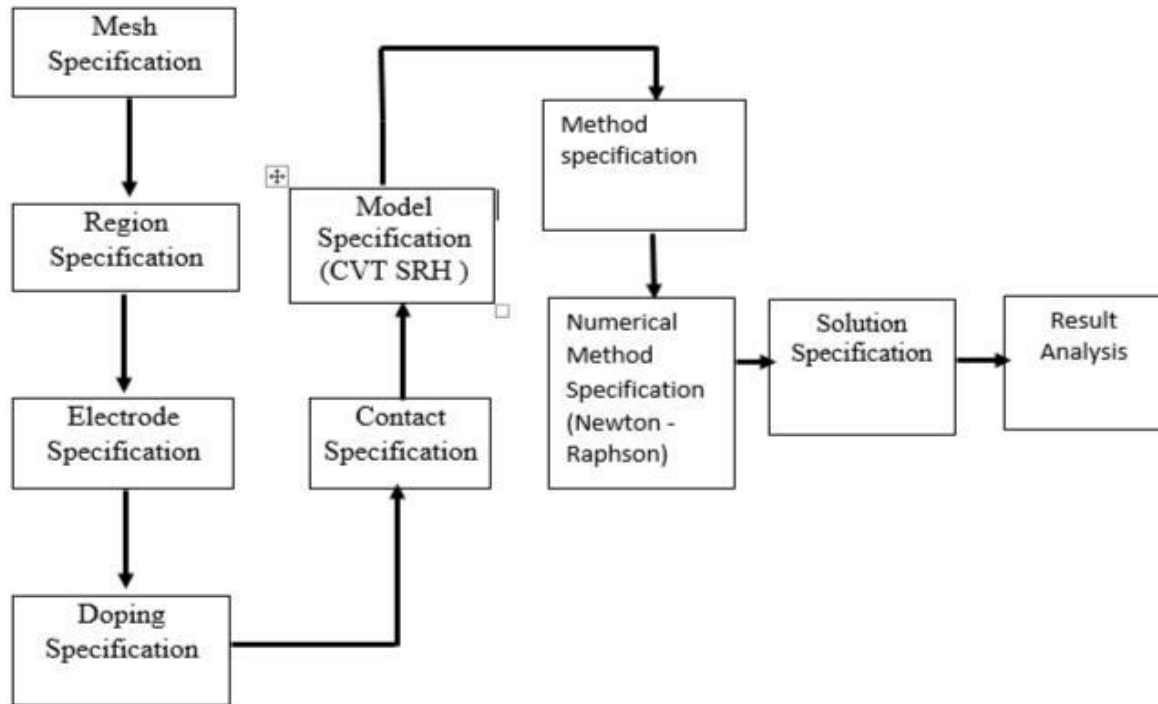


Figure 28: Summarization of device modeling in ATLAS.

Chapter 3

RESULTS AND ANALYSIS

3.1 Background

As of now, and for some considerable time in the foreseeable future, Si material is and will be the workhorse of semiconductor manufacturing industry. This is mostly due to its mature fabrication technology coupled with is good properties. Not to mention the cheap cost and almost universal, omnipresent availability. Therefore, Si-based Cylindrical gate all around MESFET(Metal Silicon Field Effect Transistor) or GAA-MESFETs should be studied first.

MESFET is a form of semiconductor technology which is very similar to a junction FET or JFET. As the name of the MESFET indicates, it has a metal contact directly onto the silicon, and this forms a Schottky barrier diode junction.Figure 1(a) shows the landscape of an n-type GAA-MESFET Figure 1(b) presents the corresponding cross-sectional schematic diagram along channel direction and coordinates.Most devices are required for high speed operation, and therefore an n-channel is used because electrons have a much greater mobility than holes that would be present in a p-channel.

The gate contacts can be made from a variety of materials including Aluminium, a Titanium-Platinum-Gold layered structure, Platinum itself, or Tungsten. These provide a high barrier height and this in turn reduces the leakage current. This is particularly important for enhancement mode devices which require a forward biased junction.

The gate length to depth ratio is an important as this determines a number of the performance parameters. Typically it is kept at around four as there is a trade-off between parasitics, speed, and short channel effects.

- **Depletion mode MESFET*:*** If the depletion region does not extend all the way to the p-type substrate, the MESFET is a depletion-mode MESFET. A depletion-mode MESFET is conductive or "ON" when no gate-to-source voltage is applied and is turned "OFF" upon the application of a negative

gate-to-source voltage, which increases the width of the depletion region such that it "pinches off" the channel.

- **Enhancement mode MESFET*:*** In an enhancement-mode MESFET, the depletion region is wide enough to pinch off the channel without applied voltage. Therefore the enhancement-mode MESFET is naturally "OFF". When a positive voltage is applied between the gate and source, the depletion region shrinks, and the channel becomes conductive. Unfortunately, a positive gate-to-source voltage puts the Schottky diode in forward bias, where a large current can flow.

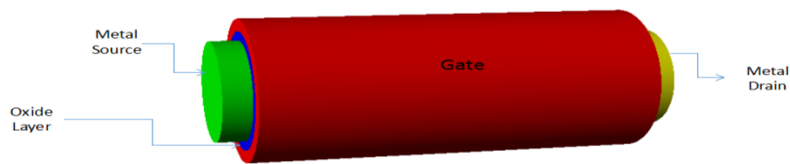


Fig 3.1: (a) The landscape of an n-type Si GAA-MESFET

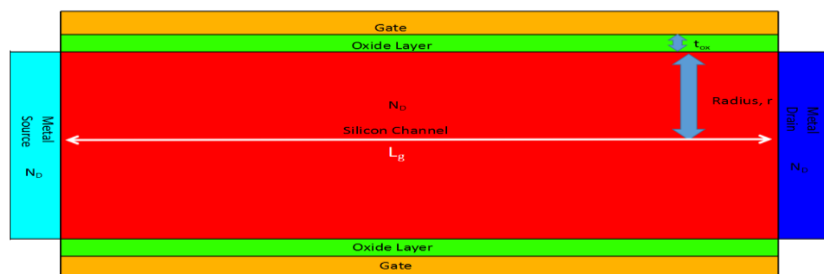


Fig.3.1:(b) cross-sectional schematic diagram along channel direction and coordinates of the device.

The long-channel threshold voltage for the n-type GAA-MESFET transistor is

$$V_{TH} = V_{FB} - \frac{qN_dR^2}{4\varepsilon_{si}} - \frac{qN_dR}{2C_{ox}} \quad (1)$$

and

$$V_{FB} = (\varphi_m - \chi - \frac{E_g}{2})/q + v_t \ln(\frac{N_d}{n_i}) \quad (2)$$

where VFB is the flat band voltage; q is the electronic charge; Nd is the doping concentration of the channel; R is the radius of the channel; Cox is the capacitance per unit area of the gate dielectric, εox is the permittivity of the oxide layer; φm is the workfunction of the gate metal. K is the electron affinity of Si. Eg is the band gap of Si. ni is the intrinsic carrier concentration of Si. vt is the thermal voltage, defined as kT/q.If the drain voltage is small the width of the depletion zone can be obtained from the Schottky diode theory:

$$x_{depl} = \sqrt{\frac{2\varepsilon_{sc}}{qN_d}(V_i - V_G)}$$

where V_i is the Schottky diode potential barrier on the semiconductor side and $\acute{\imath}\AA_{SC}$ is the permittivity of the semiconductor. The threshold voltage is the gate voltage for which $x_{depl}=a$. Using the expressions above we find the threshold voltage:

$$V_{TH} = V_i - \frac{qN_d\, a^2}{2\varepsilon_{sc}}$$

The threshold voltage can be either positive or negative, depending on the thickness of the N-type layer, the doping concentration N_d and the metal used to form the Schottky gate. If the threshold voltage is negative the MESFET is a depletion-mode device; if it is positive, it is an enhancement mode MESFET.

The current in the MESFET can be calculated as a function of gate and drain voltage using a technique similar to that which was used for the JFET. Since the channel basically behaves as a resistor the current flow from source to drain gives rise to a

progressive potential drop along the channel. The potential in the channel, noted *V(y),* varies from $V(y=0)=V_S=0$ at the source to $V(y=L)=V_D$ at the drain. In each vertical section located at a position y the reverse bias across the Schottky junction is, therefore, equal to $V_G-V(y)$.As a consequence the width of the depletion zone varies as a function of y in such a way that:

$$x_{depl}(y) = \sqrt{\frac{2\varepsilon_{sc}}{qN_d}(V_i - V_G + V(y))}$$

The expression for the current is obtained by integrating Ohm's law from source to drain:

$$dV = I_D\, dR = \frac{I_D\, dy}{q\,\mu\, N_d\, W\,(a - x_{depl}(y))}$$

where W is the device width.

Replacing $x_{depl}(y)$ by its value we obtain:

$$dV = \frac{I_D\, dy}{q\,\mu\, N_d\, W\left(a - \sqrt{\frac{2\varepsilon_{sc}}{qN_d}(V(y) + V_i - V_G)}\right)}$$

which can be re-written as:

$$q\,\mu\, N_d\, W \int_0^{V_D}\left(a - \sqrt{\frac{2\varepsilon_{sc}}{qN_d}(V(y) + V_i - V_G)}\right) dV = I_D \int_0^{L} dy$$

Performing the integration we obtain the Drain Current:

$$I_D = g_o\left(V_D - \frac{2\left((V_D + V_i - V_G)^{3/2} - (V_i - V_G)^{3/2}\right)}{3\sqrt{V_p}}\right)$$

where $$g_o = \frac{q\,\mu\,N_d\,W\,a}{L} \quad \text{and} \quad V_p = \frac{q\,N_d\,a^2}{2\,\varepsilon_{sc}}$$

These equations are valid if the channel is not pinched-off, i. e. if the device is not in saturation. Pinch-off occurs when $x_{depl}(L)=a$, at which point $V_D=V_{Dsat}=V_P-V_i+V_G$.

Saturation Drain Voltage: $V_{Dsat}=V_P-V_i+V_G=V_G-V_{TH}$.

The drain saturation current is obtained by replacing V_D by the saturation drain voltage V_{Dsat}, in Expression above, which yields the saturation drain current:

$$I_{Dsat} = g_o\left(\frac{V_p}{3} + \frac{2\,(V_i - V_G)^{3/2}}{3\sqrt{V_p}} - V_i + V_G\right)$$

The transconductance in saturation is given by:

$$g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D=constant} = g_o\left(1 - \sqrt{\frac{V_i - V_G}{V_p}}\right)$$

The n-type GAA-MESFET device was simulated in Atlas 3D. Device physical and biasing parameters are provided in Table 3.1:

Table 3.1 Device Parameters

Channel length,Lg	Radius	tox	Nd (cm^{-3})	V_{DS} (V)	V_{GS} (V)
25nm	6 nm	1.1 nm	$1*10^{19}$ cm^{-3}	0.5 V	-0.2 V - 1 V

3.2 Band Diagram

Here, the energy band diagram for different gate and drain biases has been shown.

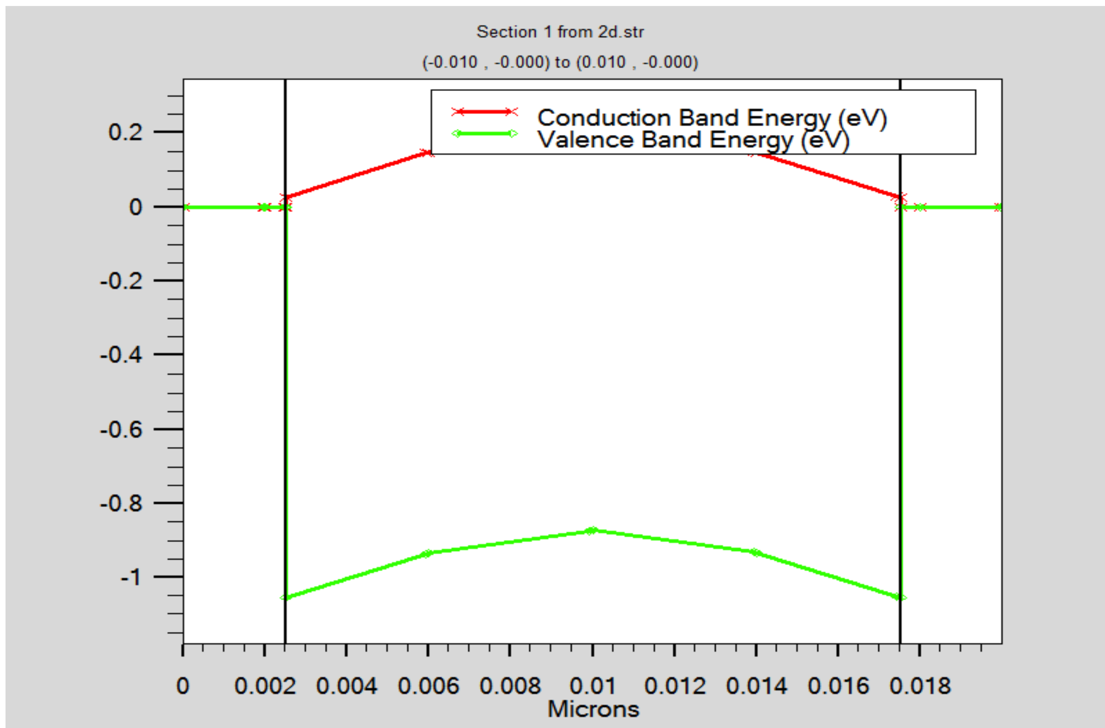


Fig 3.2: Energy band diagram when V_{GS}=0 V and V_{DS}= 0 V

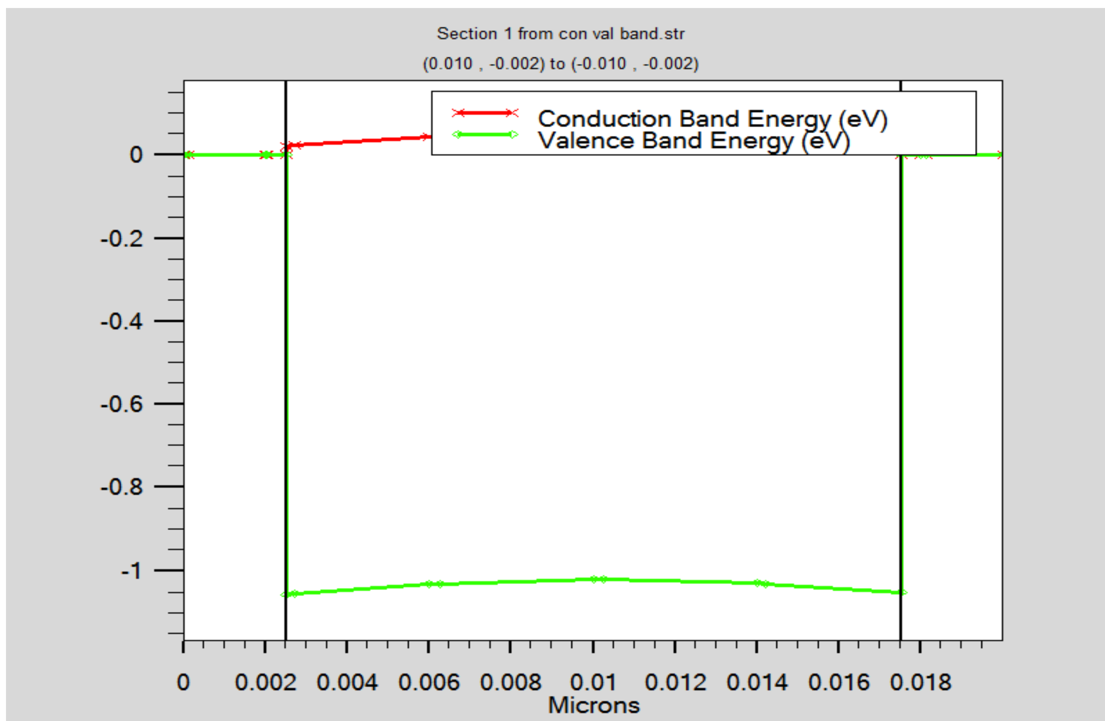


Fig 3.3: Energy band diagram when V_{GS}=0.3 V and V_{DS}= 0.005 V

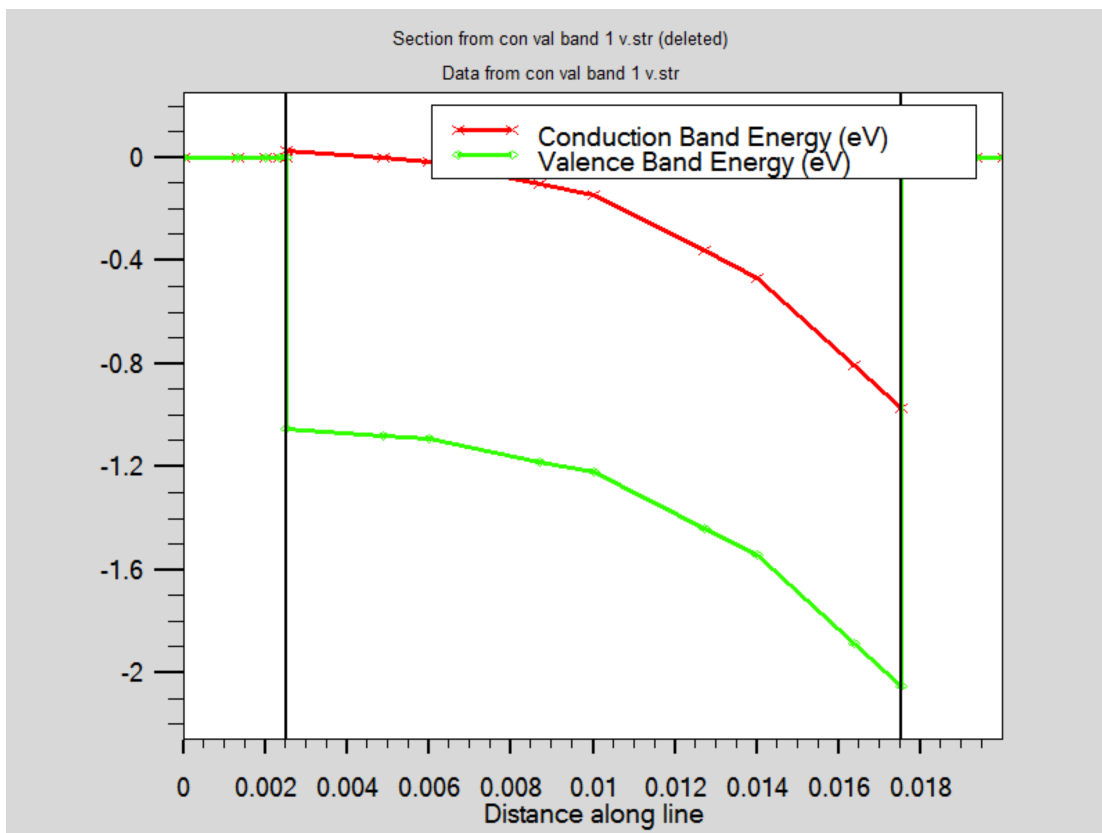


Fig 3.4: Energy band diagram when V_{GS}=0.3 V and V_{DS}= 1 V

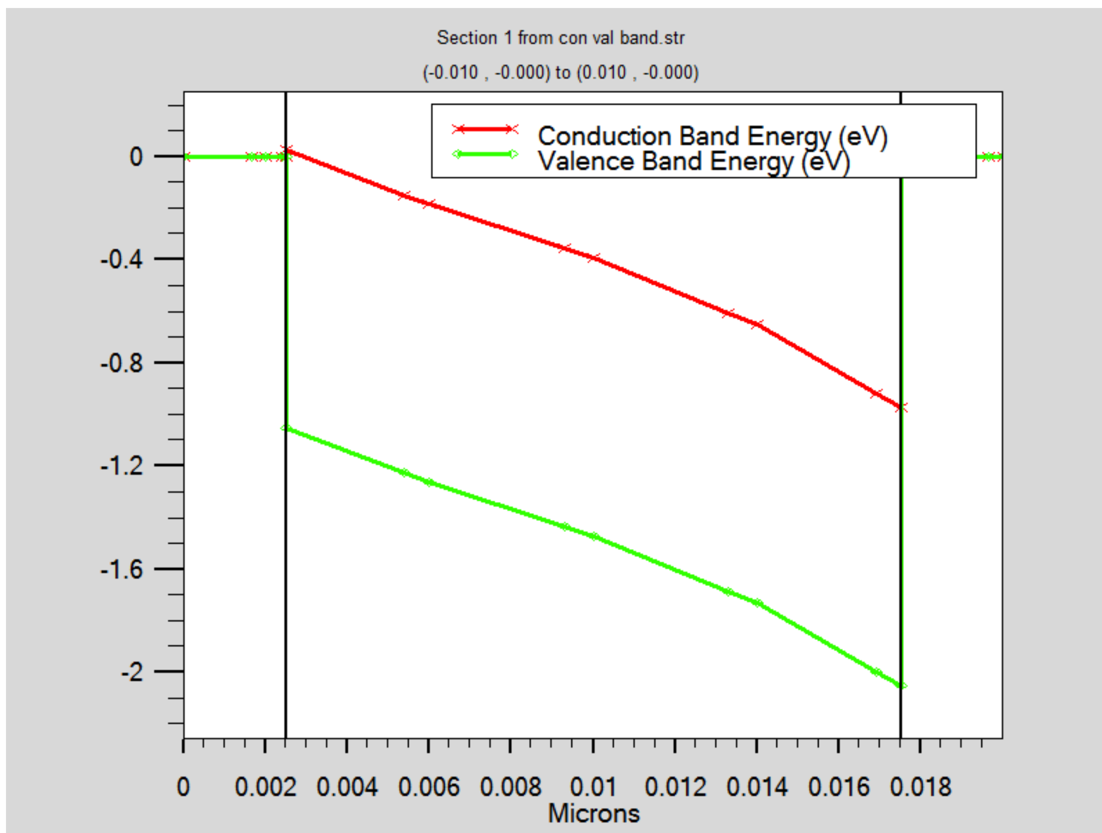


Fig 3.5: Energy band diagram when V_{GS}=1 V and V_{DS}= 1 V

In figure 3.2, the band diagram when all biases are set to zero has been drawn.Figure 3.3 and 3.4 represents the band diagram for a fixed V_{GS} (that is 0.3 V) while V_{DS} is varied(that is 0.005 V and 1 V respectively). It is seen that even for a fixed gate voltage the barrier between source and drain lowers when drain voltage is significantly increased. This is a kind of Short Channel Effect(SCE) called Drain Induced barrier Lowering(DIBL) which will be discussed in more detail in section 3.9.

In Figure 3.5, both V_{GS} and V_{DS} is increased significantly(that is 1 V) and it is seen that, this time, the barrier was lowered a great deal taking an almost linear shape proving just how great an effect both gate and drain voltage have on energy band.

3.3 Electrostatic Potential

Figure 3.6 illustrates the central electrostatic potential along channel direction for different gate lengths. And It can be seen that as the gate length decreases, the position of the minimum central potential is pulled up, leading to a lower threshold voltage. For example for a gate length 20 nm, potential is approximately 0.4 V at channel direction of around .012 μm while for 15 nm channel length it is about 0.5 V. This phenomenon is known as the threshold voltage roll-off and degrades the device subthreshold performances.

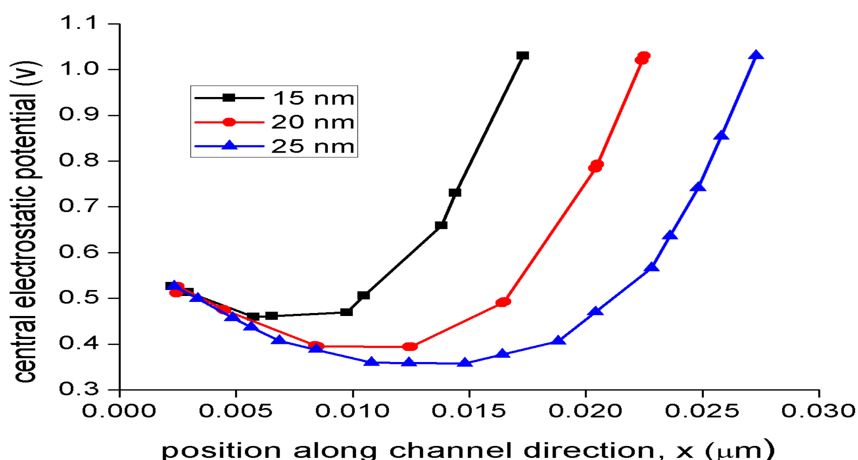


Fig 3.6: Central electrostatic potential along channel direction for different gate lengths. The simulated device parameters are Vgs = 0.2 V, R = 6 nm, Vds = 0.5 V, Nd = 1×10^{19} cm^{-3} and tox = 0.5 nm.

Figure 3.7 presents the electrostatic potential distribution in the channel center as a function of channel radius. It is observed that, as the channel radius increases, the minimum central potential along the channel direction rises up that is for radius= 7 nm, potential is 0.5V while for 8 nm it is around 0.55 v which suggests that the gate gradually loses control over the channel. This fact leads to a smaller threshold voltage for a larger channel radius, degrading the subthreshold characteristics. Hence, a smaller channel radius is desired to reduce the leakage current.

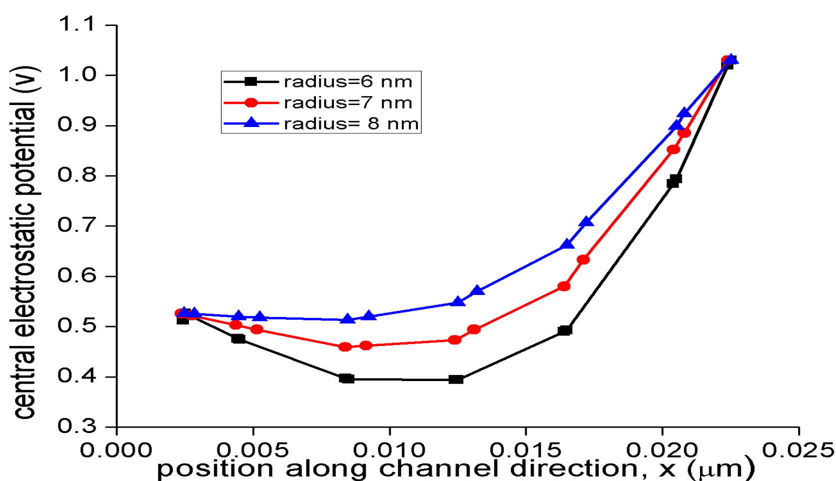


Fig 3.7: Central electrostatic potential along channel direction for different radiuses. The simulated device parameters are Lg = 20 nm, Vgs = 0.2 V, Vds = 0.5 V, tox = 0.5 nm, and Nd = 1×10^{19} cm^{-3}.

Figure 3.8 shows that the central electrostatic potential distribution for different equivalent oxide layer thicknesses, tox. It is clear that, as the equivalent oxide layer thicknesses steadily increases, potential also increases. For example when tox= 0.8 nm, potential is 0.45V while for 0.5 nm it is around 0.5 V, which shows that the gate electrode gradually loses control of the channel. This is because a thicker equivalent oxide layer will resist the vertical electric field from the metal gate penetrating into the channel, resulting in the degradation of threshold behaviors. Therefore, to suppress the SCEs, thin equivalent oxide thickness is preferred.

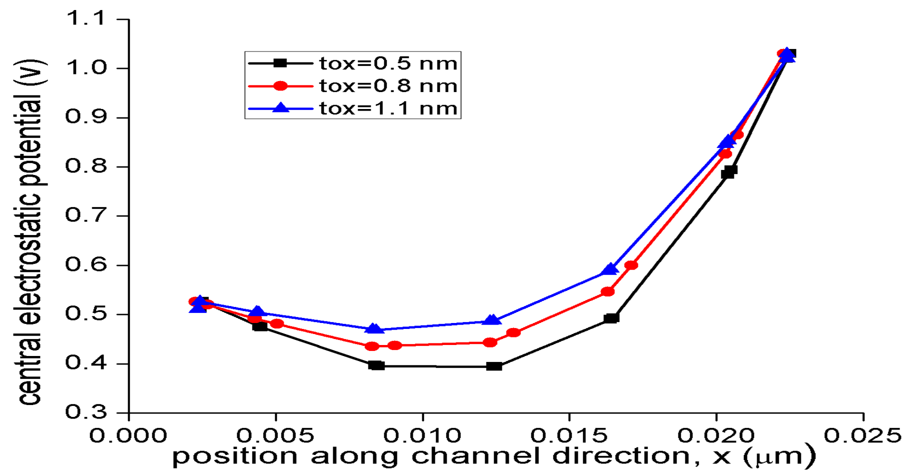


Fig 3.8: Central electrostatic potential distribution along channel direction for different equivalent oxide layer thicknesses. The simulated device parameters are Lg = 20 nm,Vgs = 0.2 V, Vds = 0.5 V,R= 6 nm, and Nd = 1×10^{19} cm^{-3}.

The central electrostatic potential distribution for different drain voltages is observed in Figure 3.9, It is obvious that, as Vds steadily increases, the position of the minimum central potential is raised which illustrates that the channel can be turned on more easily. The phenomenon is called drain inducing barrier lowering (DIBL) effect. This is a kind of important SCEs.

Figure 3.10 shows the electrostatic potential channel direction for different gate voltages. The center electrostatic potential is proportional to Vgs because of the capacitive coupling effect between the gate dielectric-layer capacitance and channel capacitance.

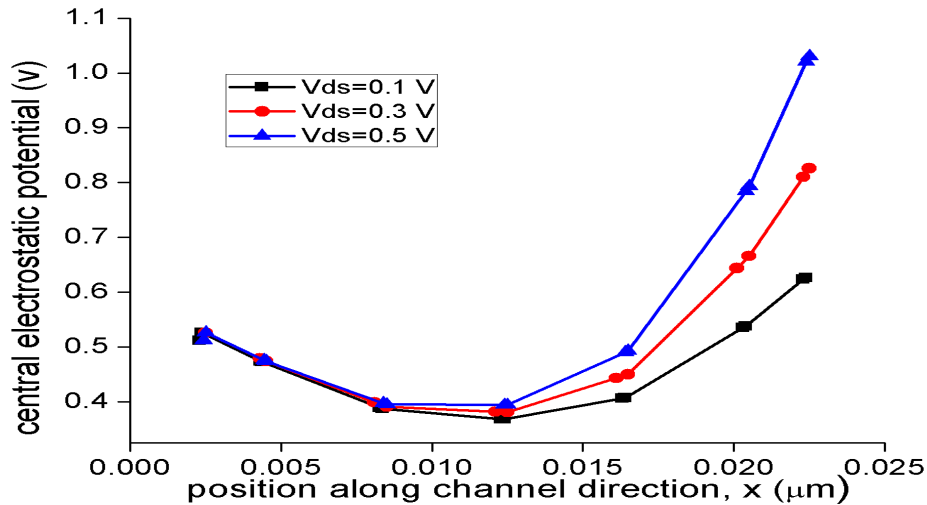


Fig 3.9: Central electrostatic potential distribution along channel direction for different drain voltages. The simulated device parameters are Lg = 20 nm, Vgs = 0.2 V, tox=0.5 nm, R= 6 nm, and Nd = 1×10^{19} $cm^{-3.}$

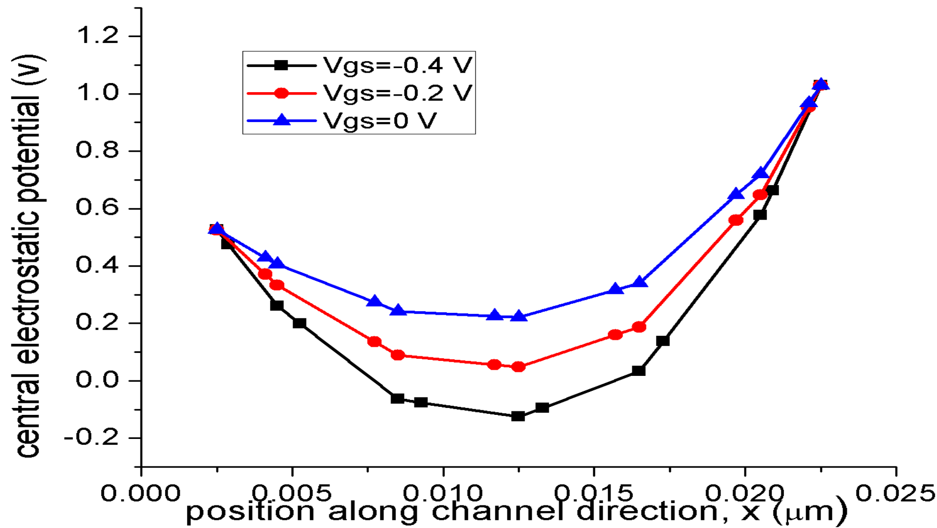


Fig 3.10: Central electrostatic potential distribution along channel direction for different gate voltages. The simulated device parameters are Lg = 20 nm, Vds = 0.5 V, tox=0.5 nm, R= 6 nm, and Nd = 1×10^{19} cm^{-3}

3.4 Electric Field

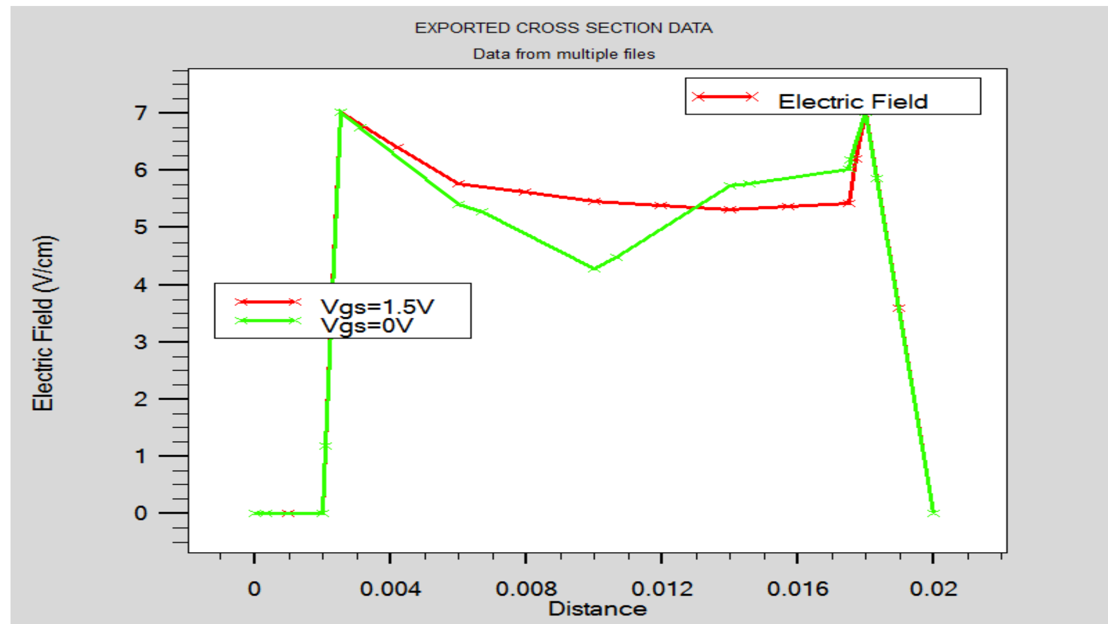


Fig 3.11: Electric field along channel direction for different gate voltages. The simulated device parameters are Lg = 15 nm, Vds = 0.5 V, tox=1.1 nm, R= 6 nm, and Nd = 1×10^{19} cm^{-3}

Fig 3.11 shows the electric field for different gate biases. It can seen that at the source body and drain body junction the electric field is very high which is about 11MV/cm.

3.5 Electron Concentration

Electron concentration in the Si body has been observed by taking 2-D cross sectional view of the device.

Figure 3.12 shows concentration profile for V_{GS}=0V and V_{DS}=0V while figure 3.13 shows the concentration profile for V_{GS}=0V and V_{DS}=0.5V. The device is in subthreshold regime in these two conditions. It can be seen that the carrier concentration level in the body is below the doping level which means that the body is fully depleted. Same can be said for figure 3.14 where V_{GS}=0.2V and V_{DS}=0.5V.

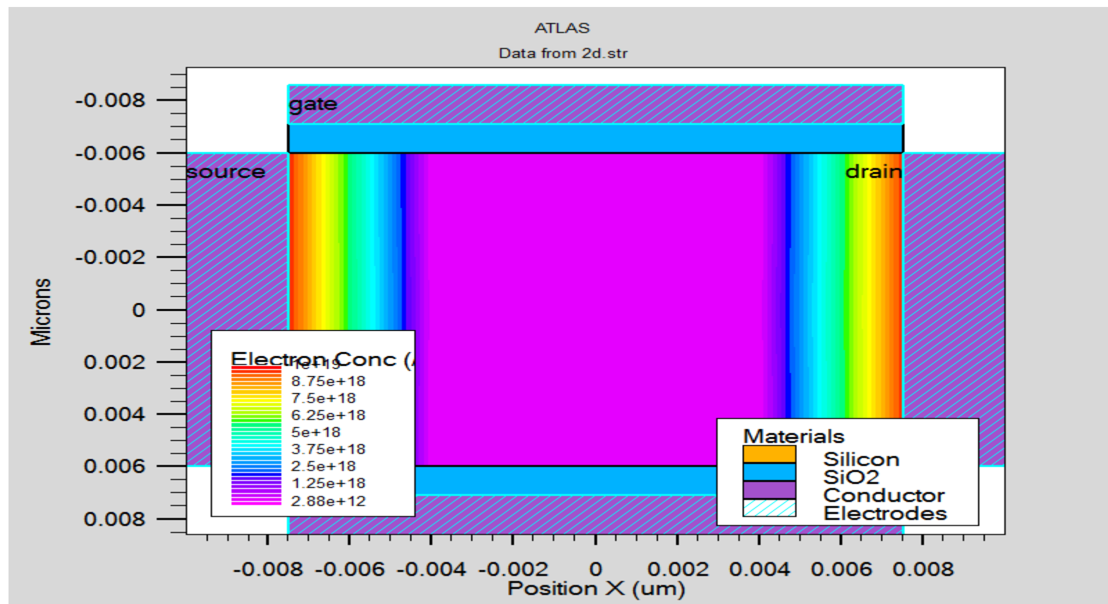


Fig 3.12(a): Electron concentration along channel direction for V_{GS}=0 V while Lg = 15 nm, V_{DS} = 0 V, tox=1.1 nm, R= 6 nm, and Nd = 1×10^{19} cm^{-3}

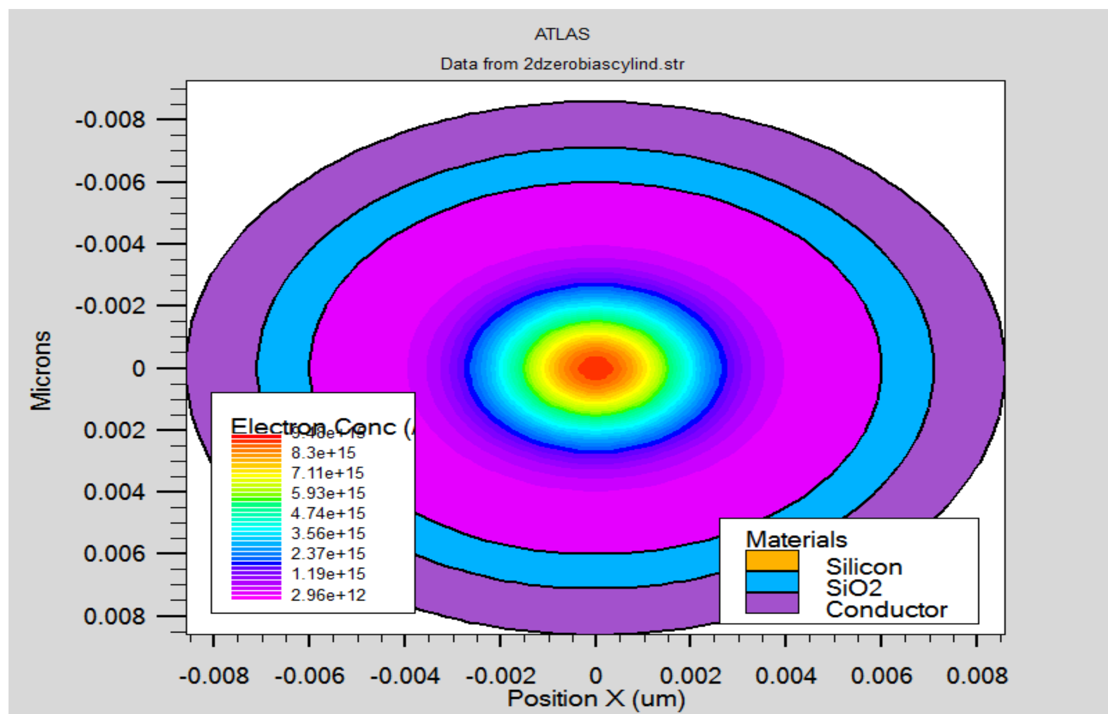


Fig 3.12(b): Electron concentration along channel direction for V_{GS}=0 V while Lg = 15 nm, V_{DS} = 0 V, tox=1.1 nm, R= 6 nm, and Nd = 1×10^{19} cm^{-3}

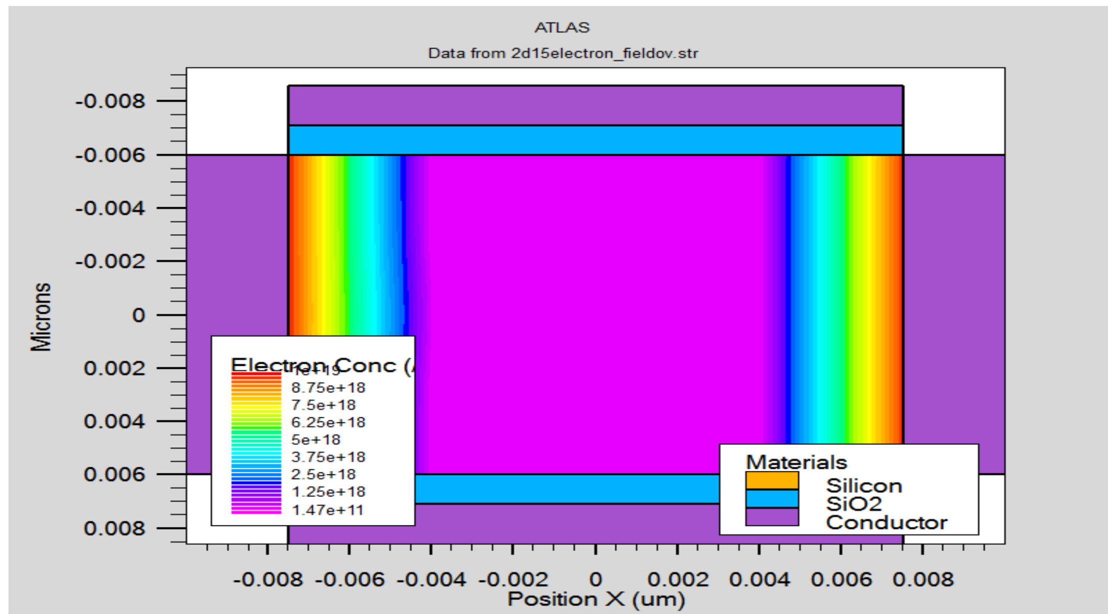


Fig 3.13: Electron concentration along channel direction for V_{GS}=0 V while Lg = 15 nm, V_{DS} = 0.5 V, tox=1.1 nm, R= 6 nm, and Nd = 1×10^{19} cm^{-3}

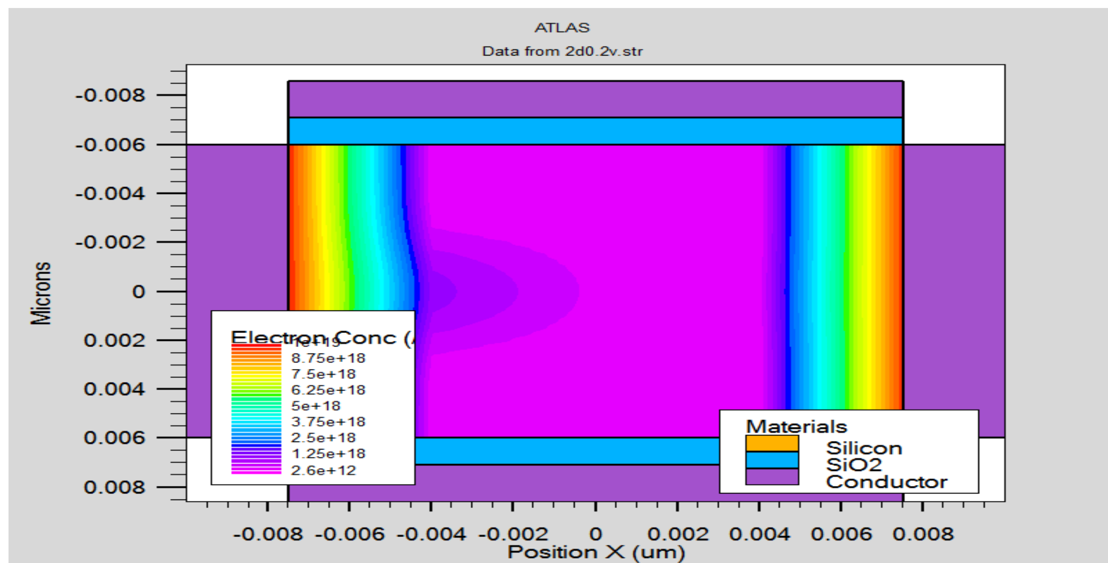


Fig 3.14: Electron concentration along channel direction for V_{GS}=0.2 V while Lg = 15 nm, V_{DS} = 0.5 V, tox=1.1 nm, R= 6 nm, and Nd = 1×10^{19} cm^{-3}

Figure 3.15 shows the electron concentration profile for V_{GS}=1.5 V respectively. It can be seen that electron concentration at top and bottom oxide has increased beyond doping level. At high gate bias carrier accumulates at the oxide-Si interface. It is also seen that the carrier concentration level in the whole body is also high which means that

current not only flows through the top and bottom surface, but also through the whole body.

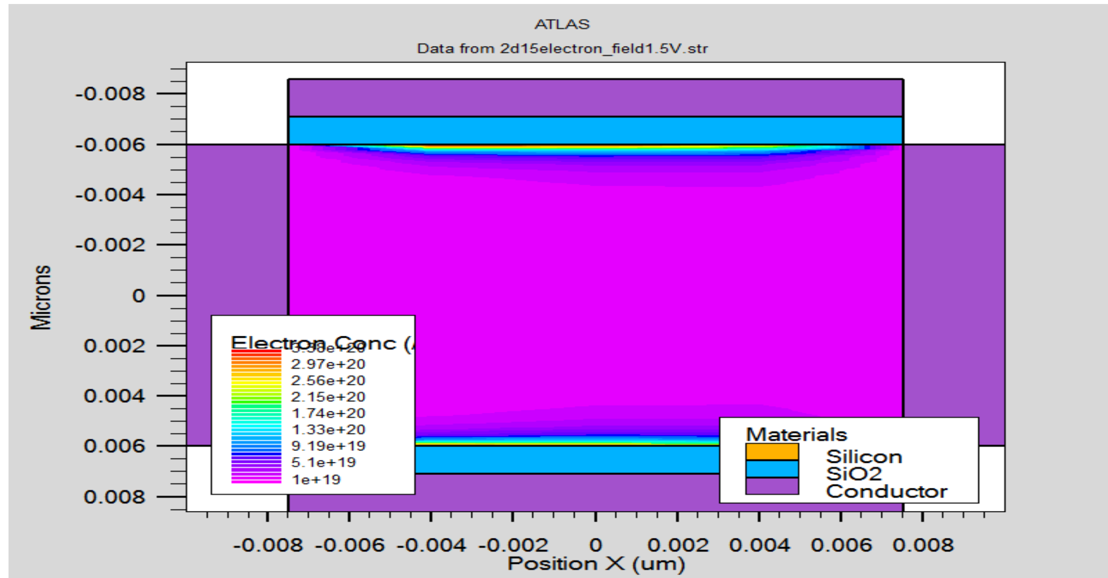


Fig 3.15(a): Electron concentration along channel direction for V_{GS}=1.5 V while Lg = 15 nm, V_{DS} = 0.5 V, tox=1.1 nm, R= 6 nm, and Nd = 1×10^{19} cm–3

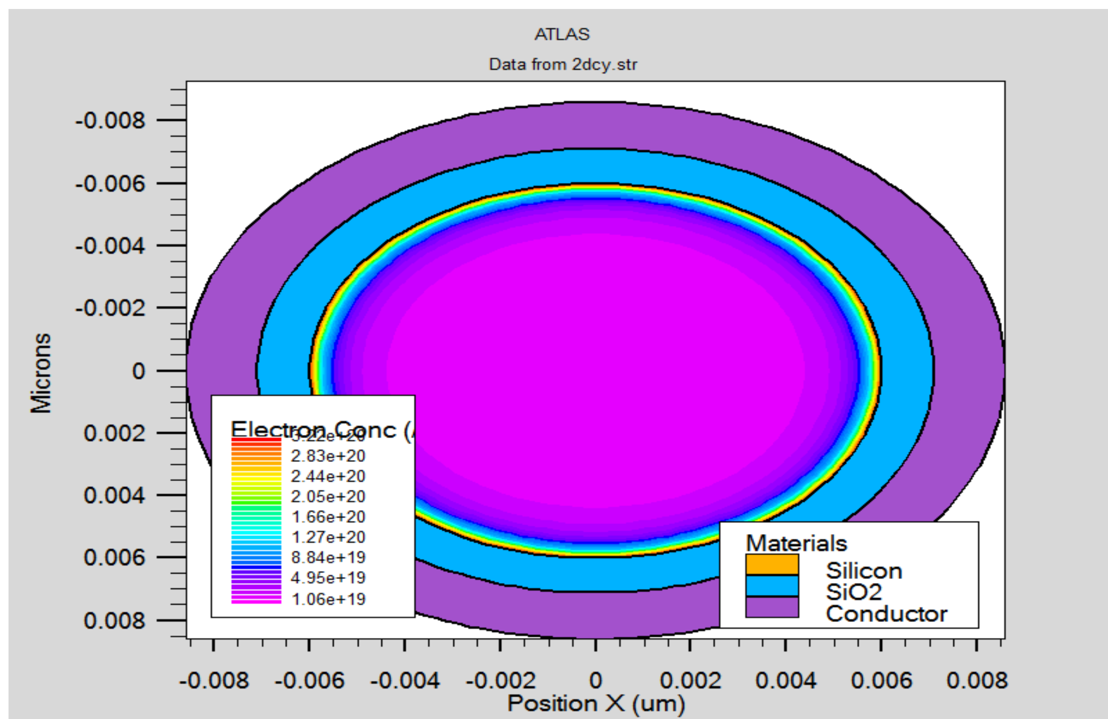


Fig 3.15(b): Electron concentration in cylindrical cutplane for V_{GS}=1.5 V while Lg = 15 nm, V_{DS} = 0.5 V, tox=1.1 nm, R= 6 nm, and Nd = 1×10^{19} cm–3

3.6 I_{DS}-V_{GS} Characteristics Curve

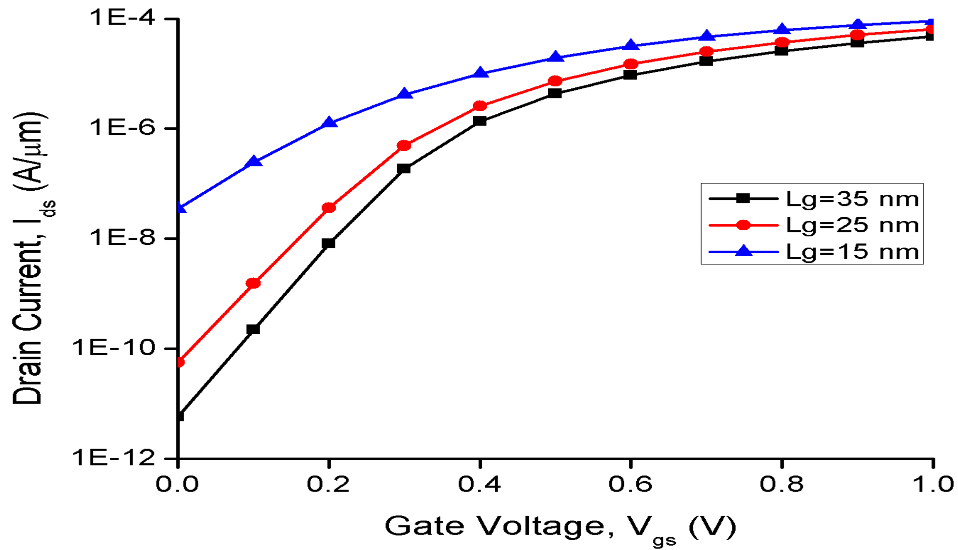


Fig 3.16: Drain current versus gate voltage for different gate lengths. The simulated device parameters are R = 6 nm, tox = 1.1 nm, Vds = 0.5 V, and Nd = 1×10^{19} cm^{-3}.

In figure 3.16, an Id -Vgs characteristic curve can be seen. It is observed that when the gate length decreases. Subthreshold leakage current increases while the on current increases. For example, for Lg=15 nm, drain current is about 10^{-5} while for 25 nm it is slightly higher at V_{GS} =0.4 v.

Table 3.2: Comparisons of different performance parameters from Fig:3.16

Length	Vt (V)	Subthreshold slope(mv/dec)	I_{on} (A)	I_{off} (A)	$I_{on/off}$
15nm	0.14	118.27	$10^{-4.168}$	$10^{-7.329}$	1448.77
25nm	0.28	69.76	$10^{-5.038}$	$10^{-10.120}$	120781.38
35nm	0.32	63.01	$10^{-5.249}$	$10^{-11.185}$	862978.54

In table 3.2, it is seen that with increasing length, threshold voltage is increasing while sub-threshold slope is decreasing. Also we observed that on current and off current is decreasing with increasing length.

Figure 3.17 shows another Id -Vgs curve which illustrates that the leakage current increases dramatically when the doping concentration slightly enlarges.For example, if Nd=0.6*10^{19} cm^{-3} then the drain current is $10^{-14.8}$ A/µm. If we increase the doping concentration then the current will be 10^{-13} A/µm.As the dopant concentration increases, the number of electrons offered by the dopant atoms also increase. Higher doping concentration makes the depletion of carriers more difficult, thereby degrading the subthreshold behaviors.One way to improve the on-state to off-state drain current ratio can be improved by controlling doping concentration of the channel, such as using the nonuniform doping technique.

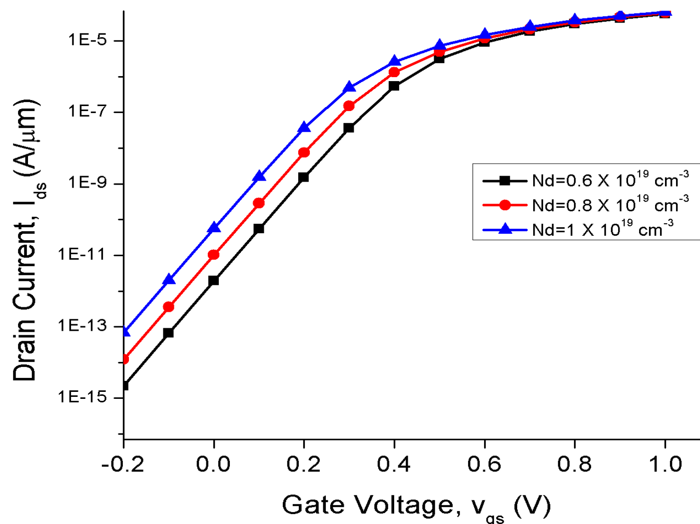


Fig 3.17: Comparison of Ids–Vgs curves with different doping concentrations. The simulated device parameters are tox = 1.1 nm, V_{DS} = 0.5 V, Lg = 25 nm, and R = 6 nm.

Table 3.3: Comparisons of different performance parameters from Fig:3.17

Doping concentration(cm^{-3})	Vt(V)	Subthreshold slope(mv/dec)	I_{on} (A)	I_{off} (A)	$I_{on/off}$
$1 * 10^{19}$	0.28	69.7554	$10^{-5.038}$	$10^{-10.120}$	120781.38
$0.8 * 10^{19}$	0.30	69.1342	$10^{-5.257}$	$10^{-10.943}$	485288.50
$0.6 * 10^{19}$	0.32	68.6739	$10^{-5.518}$	$10^{-11.594}$	1191242.01

From table 3.3. it is observed that if the doping concentration is increased then the threshold voltage also increases while sub-threshold slope decreases. As for on current and off current, they decrease with decreasing doping concentration.

In figure 3.18, it is seen that as the channel radius increases linearly, the leakage current is dramatically enlarged because the gate controllability over the channel decreases. For example at Vgs=0.2 V, the drain current for radius=7 nm is much higher than that radius= 6 nm. Although at higher gate voltage they remain rather unchanged. Therefore, the off-state current could be suppressed using an adequately small channel radius for a given gate length.

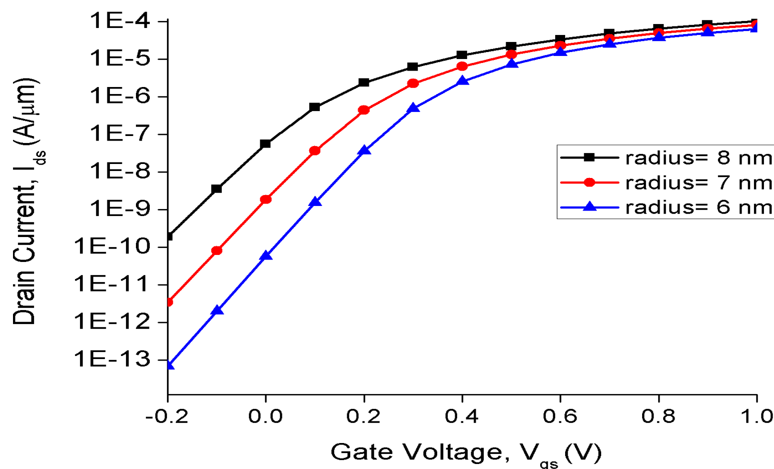


Fig 3.18: Drain current versus gate voltage for different radiuses. The simulated device parameters are Lg = 25 nm, tox = 1.1 nm, V_{DS} = 0.5 V, and Nd = 1×10^{19} cm^{-3}.

Table 3.4: Comparisons of different performance parameters from Fig:3.18

Radius (nm)	Vt (V)	Subthreshold Slope (mv/dec)	I_{on} (A)	I_{off} (A)	$I_{on/off}$
6	0.28	69.7509	$10^{-5.038}$	$10^{-10.120}$	120781.38
7	0.24	77.0462	$10^{-4.778}$	$10^{-8.651}$	7464.49
8	0.20	102.212	$10^{-4.564}$	$10^{-7.155}$	389.94

In table 3.4, it is observed that if the radius is increased from 6nm to 8nm then the threshold voltage decreases from 0.28 to 0.20 and sub-threshold slope increases from 69.7509 to 102.212. Also the on current and the off current is increasing gradually.

3.7 Threshold voltage

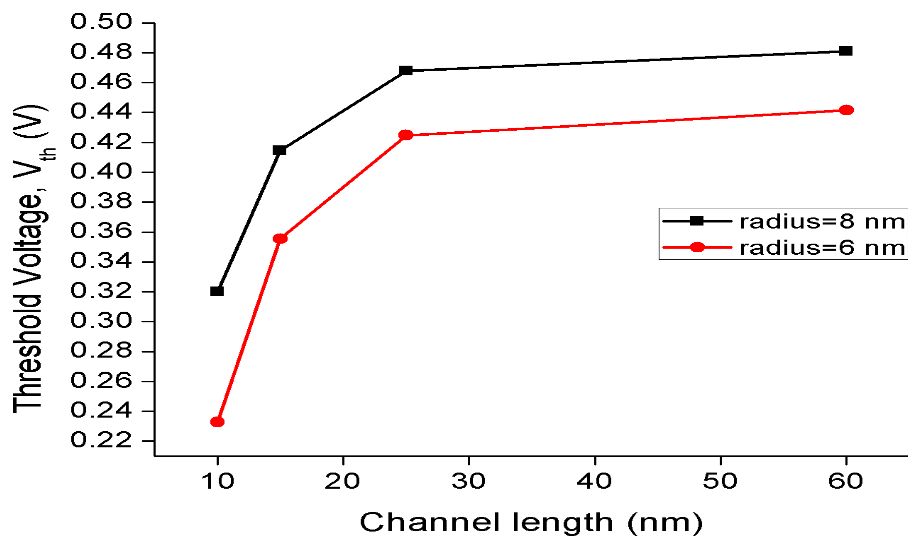


Fig 3.19: Comparison of Vth versus channel length between the different radiuses. The simulated device parameters are tox = 0.5 nm, V_{DS} = 0.05 V, and Nd = 1×10^{19} cm^{-3}.

In Figure 3.15, it can be observed that the threshold voltage is very sensitive to the channel radius because the leaky path is inside the bulk instead of at the silicon/gate dielectric layer inter-face. This is inherently different from the conventional inversion mode MOSFETs. Moreover, the threshold voltage is reduced as the gate length

decreases. This effect is known as the threshold voltage roll-off, which is a kind of typical SCEs. To effectively suppress this effect, the channel diameter should be much smaller than the gate length.

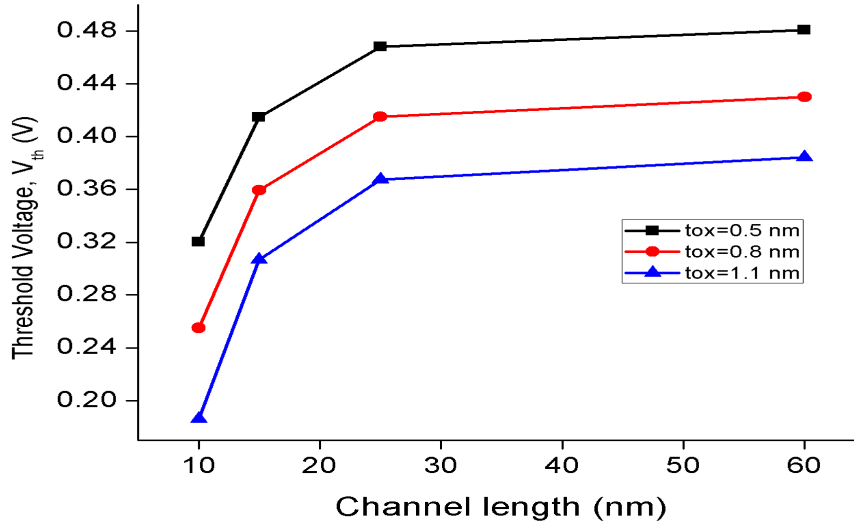


Fig 3.20: Comparison of Vth versus channel length between different equivalent oxide layer thicknesses. The simulated device parameters are R = 6 nm, V_{DS} = 0.05 V, and

Nd = 1×10^{19} cm^{-3}.

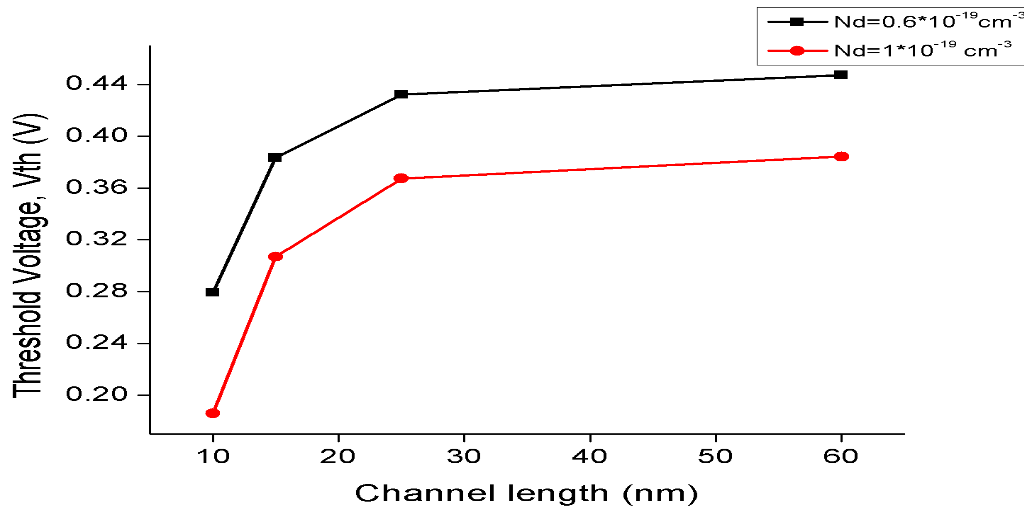


Fig 3.21: Comparison of Vth versus channel length between different doping concentration . The simulated device parameters are R = 6 nm, V_{DS} = 0.05 V, and Nd = 1×10^{19} cm^{-3}.

Figure 3.20 shows that as tox increases, Vth decreases. This is because as tox increases, the gate’s controllabilty over the channel decreases.

In Fig 3.21 shows the variation of threshold voltage with varying channel length and doping concentration. It can be observed that as the doping concentration increases, threshold voltage decreases.

3.8 I_{DS}-V_{DS} Curve

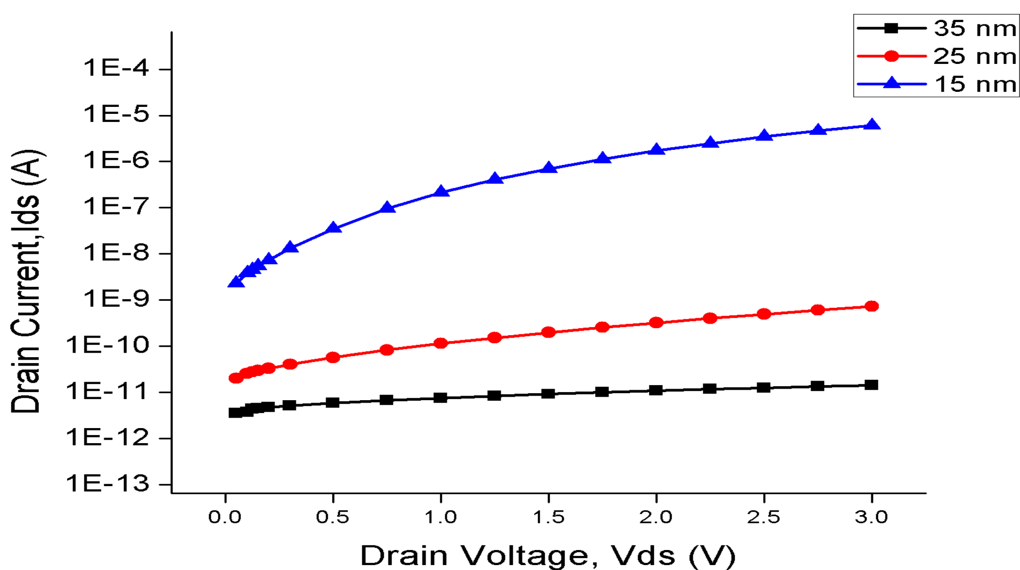


Fig 3.22: Drain current versus Drain voltage for different gate lengths. The simulated device parameters are R = 6 nm, tox = 1.1 nm, V_{DS} = 0.5 V, and Nd = 1×10^{19} cm^{-3}

Fig 3.22 shows that increase in drain voltage does not have much of an effect on drain current as the channel length increases.

Fig 3.23 illustrates that an increase in drain voltage increases the drain current almost linearly.

Fig 3.24 shows that with increase in drain voltage, the drain current almost linearly increases.

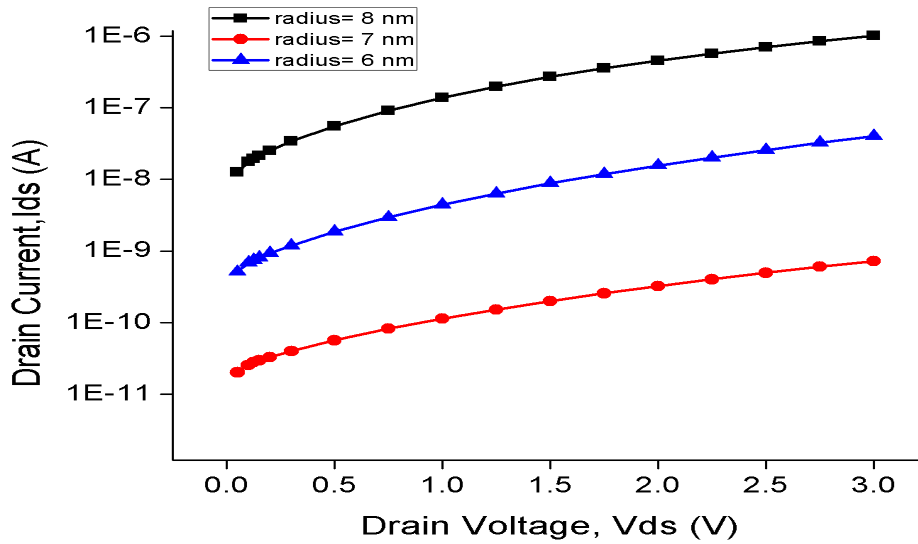


Fig 3.23: Drain current versus Drain voltage for different radius. The simulated device parameters are Lg=25 nm, tox = 1.1 nm, V_{DS} = 0.5 V, and Nd = 1×10^{19} cm^{-3}

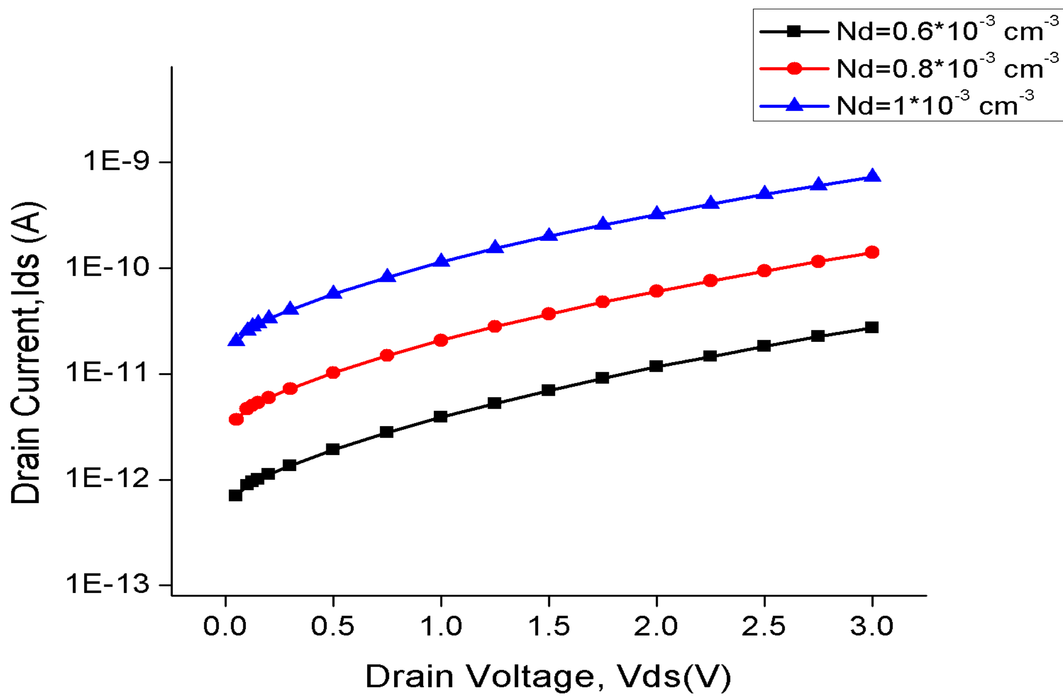


Fig 3.24: Drain current versus Drain voltage for different doping concentration. The simulated device parameters are Lg=25 nm, tox = 1.1 nm, V_{DS} = 0.5 V and radius= 6nm

3.9 Drain induced barrier lowering (DIBL)

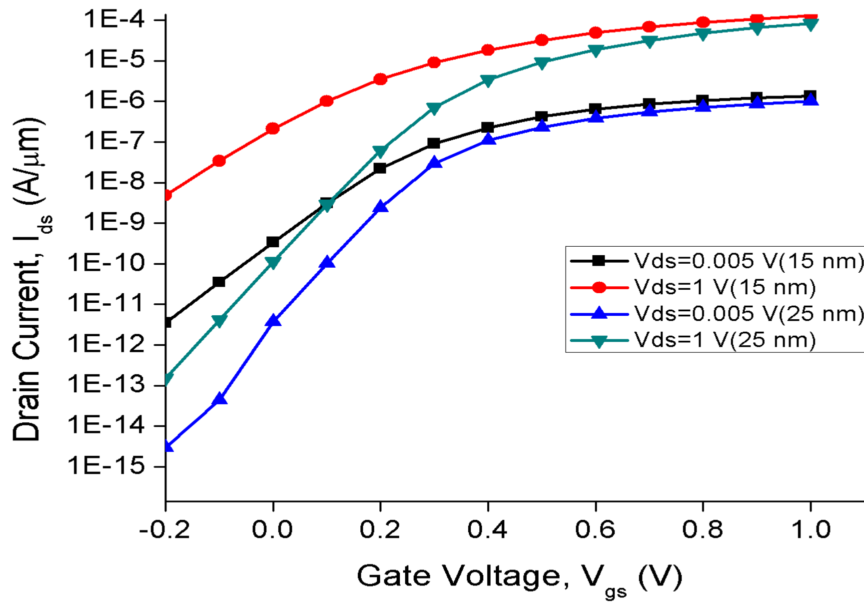


Fig 3.25: Comparison of Ids–Vgs curves between different gate lengths and drain voltages. The simulated device parameters are tox = 1.1 nm, R= 6 nm and Nd = 1×10^{19} $cm^{-3.}$

In this figure 3.25, if we increase drain voltage at 15nm length we will get higher drain current compare to at 25nm length and if we decrease the drain voltage from 1V to 0.005V and increase the length then we get lowest drain current, 10^{-15} A/µm. It can be deduced that for a fixed gate length, a large drain voltage can increase the on-state current, but it also degrades the sub-threshold behaviors because of the DIBL effect. The DIBL coefficient could be defined as the difference in the threshold voltage when the drain voltage is increased from 0.005 to 1.0 V. There is a potential barrier between the source and the channel region. The height of this barrier is a result of the balance between drift and diffusion current between these two regions. If a high drain voltage is applied, the barrier height can decrease, leading to an increased drain current. Thus the drain current is controlled not only by the gate voltage, but also by the drain voltage. For device modeling purposes this parasitic effect can be accounted for by a threshold voltage reduction depending on the drain voltage.

Table 3.5: Comparisons of different performance parameters from Fig:3.25

Channel length	V_{DS} (V)	Vt (V)	Subthreshold Slope(mv/dec)	DIBL(mV/V)
15 nm	0.005	0.30	104.36	182.60
	1	0.13	146.57	
25 nm	0.005	0.37	64.15	70.00
	1	0.20	71.03	

From table 3.5 it can be seen that for a fixed gate length as V_{DS} is increased, Vth is simultaneously decreased.

3.10 Application of High-K Dielectric and Gate Stack

It has been seen from the aforementioned figure that as the oxide(SiO2) becomes thicker, the gate gradually loses control of the channel. Hence, a thin equivalent oxide is preferred to suppress the SCEs. However, as thin oxide(SiO2) results in gate tunnelling current they will not be much of an aid here. Therefore, in order to have small tox and to suppress the gate tunneling current, high-k dielectric materials can be used. This provides us with both stronger insulation and better gate controllability.

Three different types of insulator are used here namely HfO2 and stack of Oxide-HfO2. All the resultants structure a structures are simulated and the obtained data is compared in order to evaluate the performance of each individual transistor.

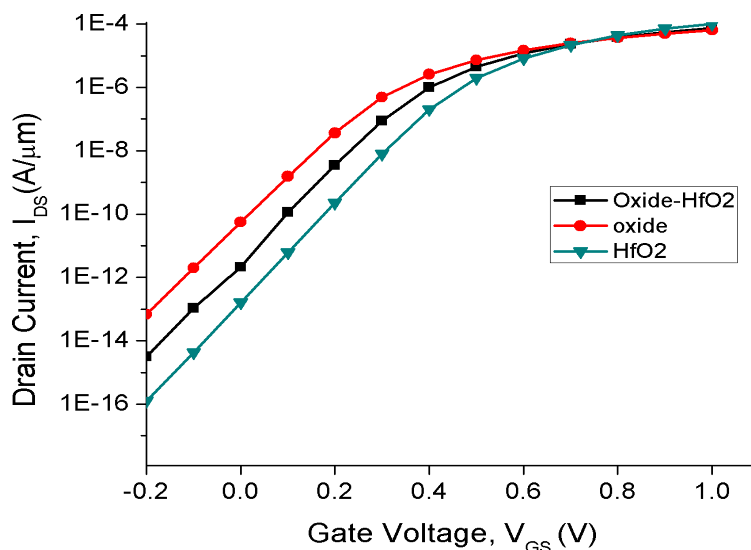


Fig 3.26: Drain current versus gate voltage for different insulators keeping the channel length and other parameters constant. The simulated device parameters are Lg=25nm R = 6 nm, tox = 1.1 nm, V_{DS} = 0.5 V, and Nd=1 × 10^{19} cm^{-3}

Figure 3.26 shows some rather interesting results. It is observed that all the new insulator used mark a significant improvement in device performance. HfO2 shows the best performance with the lowest amount of leakage current followed by the stack insulator.Another interesting phenomena is that both the stack insulator showed almost identical performance. A better evaluation of their influence can be further derived by check few others parameter which has been tabulated below.

Figure 3.27 and 3.28 reiterates our findings from figure 3.26. It is seen here, the threshold voltage roll off effect has been reduced significantly after the use of High K dielectric material, HfO2, and conjunction of High K-Low K stack, oxide-HfO2. This is due to increased gate controllability and lower gate tunneling current.

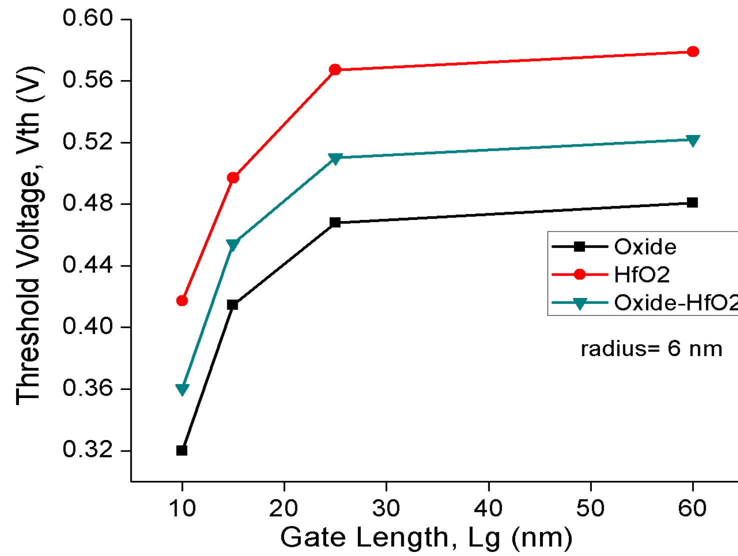


Fig 3.27: Comparison of Vth versus channel length between the different insulators. The simulated device parameters are tox = 0.5 nm, V_{DS} = 0.05 V, and Nd = 1×10^{19} cm–3.

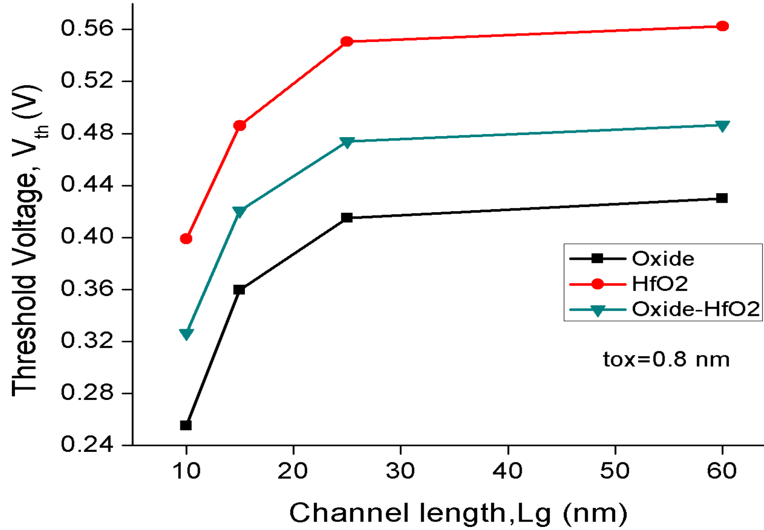


Fig 3.28: Comparison of Vth versus channel length between different insulator. The simulated device parameters are R = 6 nm, V_{DS} = 0.05 V, and Nd = 1×10^{19} cm^{-3}.

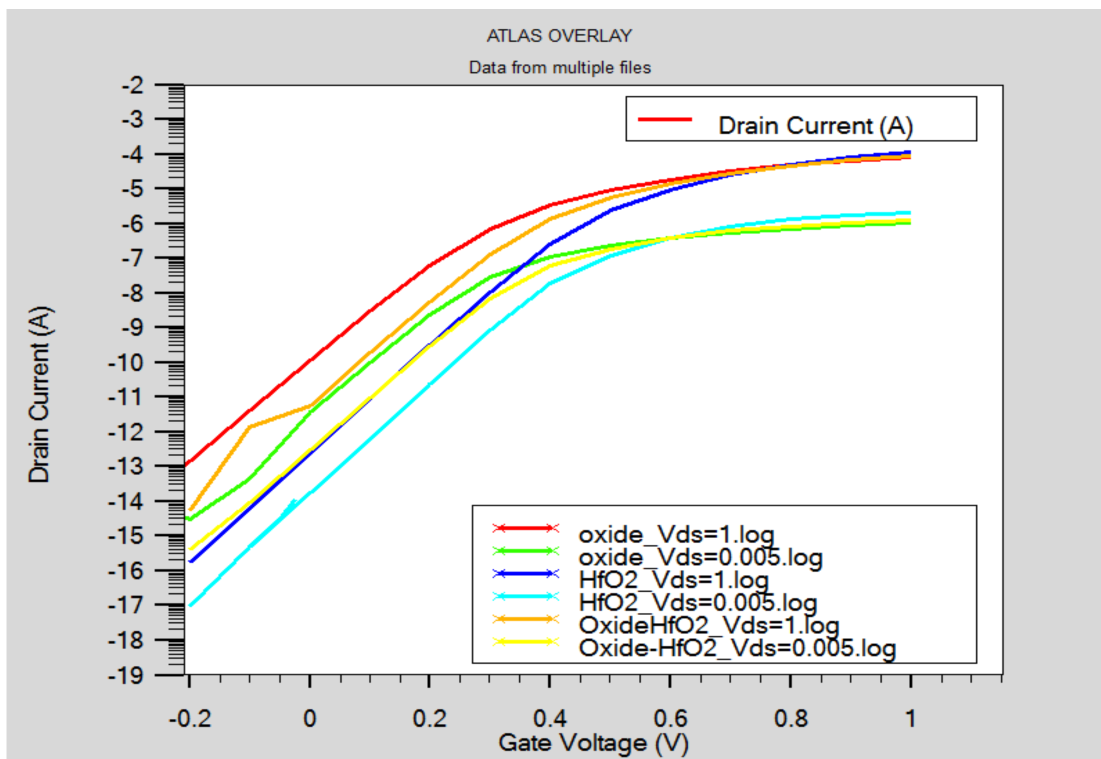


Fig 3.29: Comparison of I_{DS}–V_{GS} curves with gate length=25 nm and drain voltages of 0.005 V and 1V respectively. The simulated device parameters are tox = 1.1 nm, R= 6 nm and Nd = 1×10^{19} cm^{-3}.

Table 3.6: Comparison of data of different material as insulator, Lg=25 nm, radius=6 nm and Nd=1 * 10^{19} cm^{-3}

	Oxide	HfO2	Oxide-HfO2
Vt (V)	0.28	0.41	0.35
Subthreshold slope(mv/dec)	69.76	63.47	57.79
I_{on} (A)	$10^{-5.038}$	$10^{-5.633}$	$10^{-5.259}$
I_{off} (A)	$10^{-10.120}$	$10^{-12.684}$	$10^{-11.616}$
$I_{on/off}$	120781.38	11246049.74	2275097.43

Table 3.7: Comparison of DIBL of different material as insulator for Lg= 25 nm

	V_{DS} (V)	Oxide	HfO2	Oxide-HfO2
Vt (V)	0.005	0.37	0.54	0.44
	1	0.20	0.39	0.27
Subthreshold slope (mv/dec)	0.005	64.15	62.27	66.24
	1	71.03	63.68	65.89
DIBL(mV/V)		70.00	150.75	170.85

Table 3.6 and 3.7 summarizes device performance for different insulators.

Chapter 4

CONCLUSION

For the GAA-MESFET under consideration when we used SiO_2 as insulator, the following device performance variation have been observed:

- As gate length, Lg is increased, subthreshold slope decreases while Vt and $I_{on/off}$ ratio increases.
- When doping level in body is increased Vt and $I_{on/off}$ ratio decreases, while subthreshold slope increases slightly.
- When Si body radius is increased, Vt and and $I_{on/off}$ ratio decreases while subthreshold slope increases.

The device performance is compared for 3 different insulator combinations: High-k oxide (HfO2), Low-k oxide (SiO2), and stack of high and low-k oxides. The following observations have been made for the three device structures:

- Use of High K decreases the leakage current while increasing the on current of the device. This means that, high K provides largest $I_{on/off}$ ratio.
- High k offers the highest threshold voltage compared to its Low K oxide and stack counterpart.
- For High-K oxide, DIBL is the highest.
- Stacking of high and low-k oxides provides the lowest subthreshold slope.

The work can be extended for varying channel materials. Besides, the GAA-MESFET structure can be compared with other GAA structures. Besides, since radius below 5 nm is not used here, we did not incorporate quantum effects. Quantum models can be included to see how device characteristics alter for shorter channel radius and channel length.

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